Dual Gate Metal-Insulator Tunneling Transistors

by

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Abstract

This thesis introduces and investigates new class of metal insulator tunneling transistor (MITT) devices. MITT devices with sub 5nm features, having a geometry that represents a realistic implementation, are studied using a simulation model developed for this thesis. The effect of changing the dimensions of the device is studied, and the performance of devices having different geometries is compared. Two different fabrication processes are developed and preliminary results for one of these processes are is presented.

Preface

Portions of Chapters 1-4 of this thesis has been published as A. J. McDermott and A. Y. Elezzabi "Deep Gate Field Penetration Au:ZrO_2 Metal-Insulator Tunneling Transistor" *IEEE Transactions on Electron Devices*, vol. 67, no. 6, 2627-2632. A. Y. Elezzabi is the supervisory author and was involved with concept formation and manuscript composition.

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Chapter 1

Introduction

1.1 Motivation

The rate at which transistors have been reduced in size to meet the demand for higher microprocessor performance was predicted by Moore's law, and to date, that prediction has largely proven to be valid[1]. In recent years, the introduction of fin field-effect transistors (finFETs) facilitated a drastic reduction in the minimum feature size of complementary metaloxidesemiconductor (CMOS) transistors and has fueled the increase in device integration density. The finFETs nanoscale channel width has been the primary reason for the increased device density; however, with the recent realization of sub-10nm nodes, the mass-produced transistors are fast approaching a limit where further reductions in channel width will be challenging. Further decreases in size will require a reduction in the channel length which introduces new complications as the distance between source and drain shrinks below 10nm. In such a short channel, quantum effects — particularly electron quantum tunneling — results in leakage current that dissipates power when the transistor is not switching. Direct electron tunneling through the gate oxide and between the source and drain contacts increases exponentially as the channel length is decreased.

As the distance between device contacts is reduced, the tunneling current can become comparable in magnitude to the transport current. Consequently, transistor devices operating at the quantum scale need to take advantage of tunneling of charge carriers and integrate the effects of tunneling into the operation of the device. Studies of various tunneling devices, including Si-based tunneling FETs[2], graphene based tunneling transistors[3], and metal-insulator tunneling transistors (MITT)[4, 5], have demonstrated that transistors based on quantum tunneling are highly promising. In particular, MITT devices are interesting due to the simplicity of design and ease of fabrication, being made of potentially only two materials.

1.2 Thesis Objectives

The thesis investigates the operation and performance of sub 10nm MITT devices from a practical perspective.

1.3 Theoretical Framework

This thesis investigates the steady-state operation of two-dimensional metal-insulator-metal electron tunneling devices. In order to assist the reader with understanding the theoretical model used, the relevant background theory in quantum mechanics and electrostatic will be presented in this section. Should the reader be interested in exploring this theory further, Griffiths' Introduction to Quantum Mechanics[6] and Introduction to Electrodynamics[7] provide thorough coverage of the topics.

1.3.1 Electron Tunneling

The behavior of a quantum particle is described by the Schodinger's equation, from which the wavefunctions, $\Psi(\mathbf{r}, t)$ and corresponding energy for a particle can be ob-

tained:

$$-\frac{\hbar^2}{2m}\nabla^2\Psi(\mathbf{r},t)+U(\mathbf{r},t)\Psi(\mathbf{r},t)=i\hbar\frac{\partial\Psi(\mathbf{r},t)}{\partial t} \tag{1.3.1}$$

where $\hbar$ is Planck's constant, m is the mass of the particle, $U(r,t)$ is the potential with respect to the particle, and i is $\sqrt{-1}$. Ultimately, we will be using 1.3.1 to obtain the tunneling probability for a single electron through a one dimensional potential $U(z)$, so we can use a simplified version of Schrodinger's equation, assuming that the potential $U(r,t)$ is independent of time and depends only on the z-direction, (i.e. $U(r,t)=U(z)$). Next, assuming a product of single variable function for the wavefunction $\Psi=\psi(z)\phi(t)$ a simple separation of variables can be used to obtain the time independent Schrodinger's equation:

$$-\frac{\hbar^2}{2m}\frac{\mathrm{d}^2\psi(z)}{\mathrm{d}z^2}+U(z)\psi(z)=E\psi(z) \tag{1.3.2}$$

where $\Psi(z,t)=\psi(z)e^{-i\frac{Et}{\hbar}}$.

1.3.1.1 Tunneling Through a Finite Constant Potential Barrier

To provide a basic derivation of tunneling probability we can turn our attention to the finite constant potential barrier, shown in FIG. 1.1, which has the following rectangular potential $U(z)$:

$$U(z)=\begin{cases}0, & z<a, & \text{Region I}\\ U_0, & a\le z\le b, & \text{Region II}\\ 0, & z>b, & \text{Region III}\end{cases} \tag{1.3.3}$$

For the potential shown in Fig. 1.1, a particle having an energy between 0 and U_0 can propagate freely in regions I and III, but cannot in region II. However, as will be described below, the wavefunction $\psi(z)$ still exists in region II, leading to

the possibility of an particle propagating toward the barrier to tunnel through the barrier. The solution to Schrodinger's equation for the finite constant potential barrier describes the tunneling phenomena.

In regions I and III, 1.3.2 becomes:

$$\frac{\mathrm{d}^2\psi_{I,III}(z)}{\mathrm{d}z^2} = -k^2\psi(z) \tag{1.3.4}$$

where $k = \sqrt{2mE}/\hbar$, which, when solved, results in a plane wave solution with the general form consisting of a linear superposition of plane waves traveling to the right and left:

$$\psi_I(z) = C_0 e^{ikz} + C_1 e^{-ikz} \tag{1.3.5a}$$

$$\psi_{III}(z) = C_4 e^{ikz} + C_5 e^{-ikz} \tag{1.3.5b}$$

where C_0, C_1, C_4, and C_5 are constants.

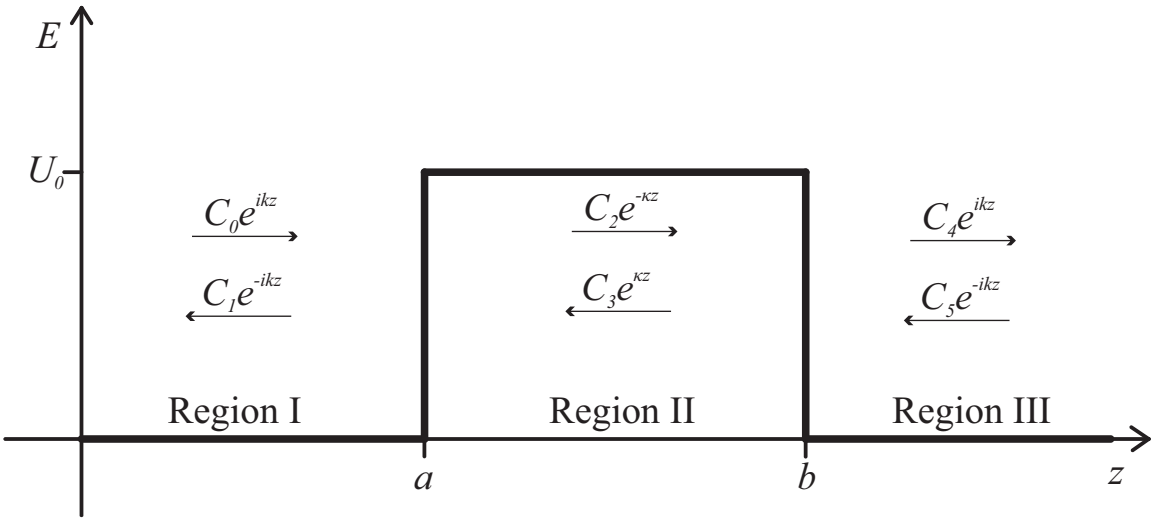

Figure 1.1: A finite constant potential barrier showing the solution to Schrodinger's equation in the three different regions.

It should be noted that the wavefunction in 1.3.5 does not represent a physical particle, as it cannot be normalized. However, that does not mean it is not useful, as it can be used to obtain the relative probability density of two different regions for a

propagating particle with energy E. In region II, we have an equation that is very similar to the equations obtained for regions I and III:

$$\frac{\mathrm{d}^2\psi_{II}(z)}{\mathrm{d}z^2} = -\kappa^2\psi(z) \tag{1.3.6}$$

where $\kappa = \sqrt{2m(E-U_0)}/\hbar$. If $E > U_0$, the resulting wavefunction has the same form as 1.3.5. When $E < U_0$, region II would be a classically inadmissible region (i.e. a classical particle would have to gain energy in order to exist in region II). Due to the wave properties of quantum particles, there is a greater than zero probability that the particle exists in region II. Since $E < U_0$, we can rewrite $\kappa = i\sqrt{2m(U_0-E)}/\hbar$, which results in the following solution for $\psi(z)$:

$$\psi_{II}(z) = C_2e^{\kappa z} + C_3e^{-\kappa z} \tag{1.3.7}$$

where C_2 and C_3 are constants.

The wave function can be said to be attenuating in region II and propagating in regions I and III. Since the wavefunction $\Psi(z,t)$ describes the probability density of a particle we can use the results from 1.3.5 and 1.3.7 to determine the probability of a particle passing through the barrier. Fig. 2 presents a qualitative representation of the tunneling process.

If a particle is represented by a right traveling wavefunction in region I with an amplitude of C_0, and we assume that the amplitude of the left traveling wavefunction in region III (i.e. C_5) is zero, then the amplitude of wavefunction that has passed through the potential barrier, C_4, represents the probability of the particle tunneling through the potential barrier. As the wavefunctions used cannot be normalized, the amplitude C4 does not provide information on its own, however the tunneling probability $D(E) = |C_4/C_0|^2$ is obtained by squaring the absolute value of the ratio of the right traveling wave in region III and the right traveling wave in region I.

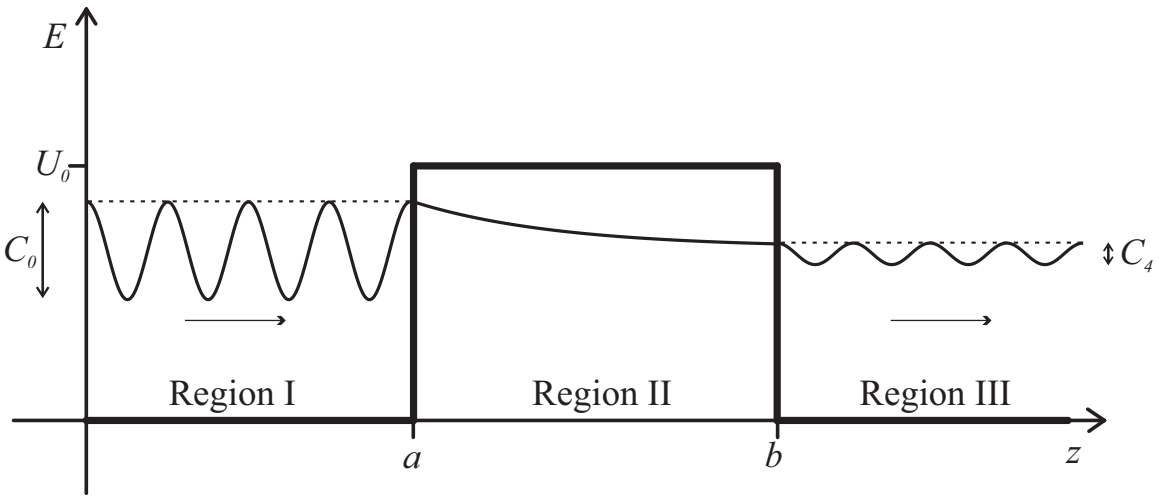

Figure 1.2: An illustration of a plane wave particle with a wavefunction amplitude C_0 attenuating through Region II.

To solve for $D(E)$, the following boundary conditions are imposed on $\psi(z)$ at the boundaries between regions I, II, and III: $\psi(z)$ is continuous across the boundaries and $d\psi(z)/dz$ is continuous at the boundaries.[1] The four boundary conditions are used to eliminate the coefficients C_1, C_2, C_3, and C_5 and solve for $D(E) = |C_4/C_0|^2$. For the finite constant potential barrier $D(E)$ is as follows for $E < U_0$:

$$D(E) = \frac{1}{1 + \frac{U_0^2 \sinh^2(\kappa_1(b-a))}{4E(U_0-E)}} \tag{1.3.8}$$

where $\kappa_1 = i\kappa$.

1.3.1.2 Transfer Matrices and the Transfer Matrix Method

The concept of solving boundary conditions to obtain tunneling probabilities can be extended to a general form which describes the transmission probability of a particle of energy E through any arbitrary potential, as illustrated in Fig. 1.3. Here, the scenario in regions I and III is identical to the corresponding regions for the finite constant barrier, and the solution to eq. 1.3.2 remains the same. However, in region II, because the potential is arbitrary, a general solution is needed. The general solution

[1] $d\psi/dz$ must be continuous except where $E = \pm\infty$

to a single variable, second order differential equation, such as eq. 1.3.2 has the following form:

$$\psi_{II}(z) = C_2 f(z) + C_3 g(z) \tag{1.3.9}$$

where $f(z)$ and $g(z)$ are two linear solutions to eq. 1.3.2. Applying the aforementioned boundary conditions at $z = a$ and $z = b$ allows for the amplitudes in region III to be written in terms of C_0 and C_1 as follows:

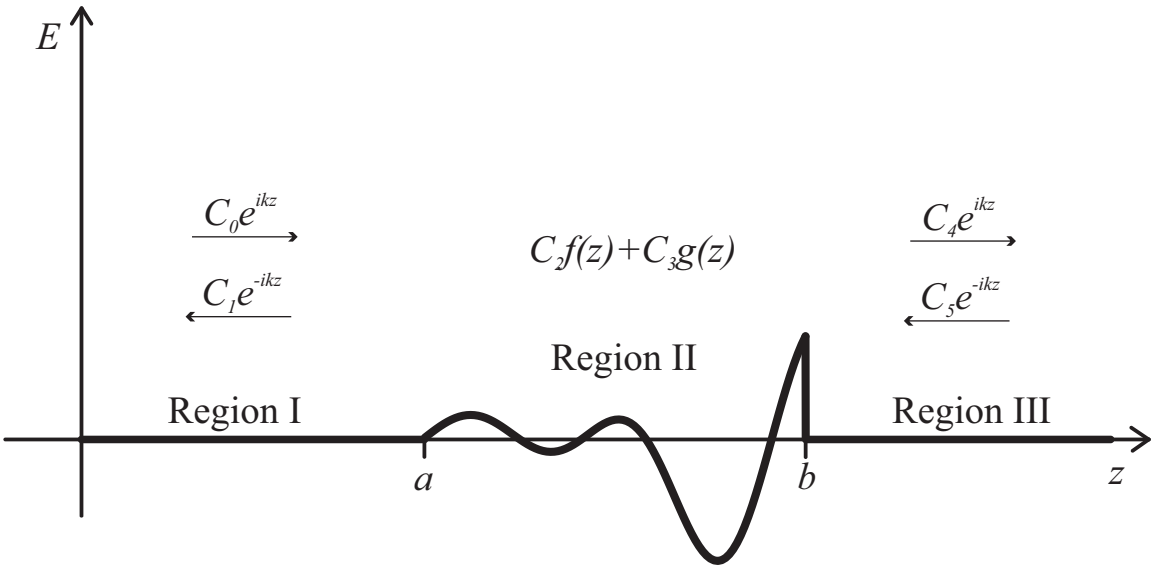

Figure 1.3: Arbitrary finite potential barrier.

$$C_4 = M_{11} C_0 + M_{12} C_1 \tag{1.3.10a}$$

$$C_5 = M_{21} C_0 + M_{22} C_1 \tag{1.3.10b}$$

where $\mathbf{M}_{11}$, $\mathbf{M}_{12}$, $\mathbf{M}_{21}$, and $\mathbf{M}_{22}$ depend on k, a, b, $f(z)$, and $g(z)$ and define the transfer matrix $\mathbf{M}$, which can be rewritten as:

$$\begin{pmatrix} C_4 \\ C_5 \end{pmatrix} = \begin{pmatrix} M_{11} & M_{12} \\ M_{21} & M_{22} \end{pmatrix} \begin{pmatrix} C_0 \\ C_1 \end{pmatrix} = \mathbf{M} \begin{pmatrix} C_0 \\ C_1 \end{pmatrix} \tag{1.3.11}$$

If an exact solution can be found in each region, the transfer matrix $\mathbf{M}$ describes the scattering states of a particle with energy E in a potential $U(z)$.

As above, to determine the tunneling probability $D(E)$, C_0 is set to equal 1, C_5 is set to equal zero and $D(E) = |C_4|^2$ is solved which results in:

$$D(E) = |C_4|^2 = \frac{1}{|M_{22}|^2} \tag{1.3.12}$$

If a potential barrier $U(z)$ has 2 regions in which an exact solution exists, a transfer matrix exists for a plane wavefunction crossing the barrier between the two regions, as the two equations that make up the transfer matrix correspond to the two boundary conditions. For example, for the finite constant potential barrier transfer matrices $\mathbf{M}_{1\to2}$ and $\mathbf{M}_{2\to3}$ for the at the boundaries of Regions I and II and Regions II and III as follows:

$$\begin{pmatrix} C_2 \\ C_3 \end{pmatrix} = \mathbf{M}_{1\to2} \begin{pmatrix} C_0 \\ C_1 \end{pmatrix} \tag{1.3.13a}$$

$$\begin{pmatrix} C_4 \\ C_5 \end{pmatrix} = \mathbf{M}_{2\to3} \begin{pmatrix} C_2 \\ C_3 \end{pmatrix} \tag{1.3.13b}$$

can be calculated and, eq. 1.3.13a can be substituted into eq. 1.3.13b to obtain an overall transfer matrix $\mathbf{M}_{1\to3} = \mathbf{M}_{2\to3}\mathbf{M}_{1\to2}$:

$$\begin{pmatrix} C_4 \\ C_5 \end{pmatrix} = \mathbf{M}_{2\to3}\mathbf{M}_{1\to2} \begin{pmatrix} C_0 \\ C_1 \end{pmatrix} \tag{1.3.14}$$

Multiplying transfer matrices can be extended to N number regions in which an exact solution for the wavefunction exist by multiplying transfer functions for each boundary:

$$\mathbf{M} = \mathbf{M}_N \mathbf{M}_{N-1} \cdots \mathbf{M}_1 \mathbf{M}_0 \tag{1.3.15}$$

The Transfer Matrix Method (TMM) involves obtaining $\mathbf{M}_0$ through $\mathbf{M}_N$ and using equations 1.3.15 and 1.3.12 to obtain a solution for a complex potential that is approximated as piecewise $\psi(z)$ functions of constant potential. This approximation is illustrated in Figure 1.4. Obtaining the overall transfer function $\mathbf{M}$ provides an overall tunneling rate $D(E)$ for an arbitrary potential that is split into a piecewise function of constant potentials.

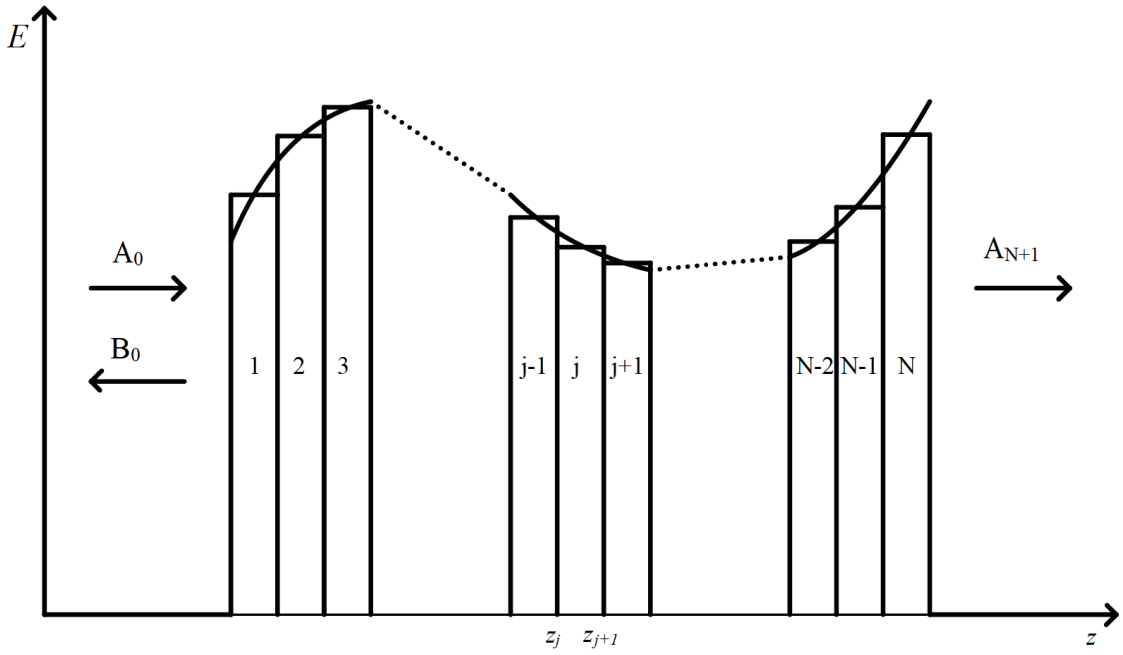

Figure 1.4: Piecewise arbitrary potential split into N section, where A_0 is the amplitude of the incident wave, B_0 is the amplitude of the reflected wave, and A_{N+1} is the amplitude of the transmitted wave.

Referring to Fig. 1.4, each piece j is centered at a location z_j, and has an potential value, U_j, which are used to find the solution to $\psi_j(z)$ within that section as follows:

$$\psi_j(z) = A_j e^{k_j z} + B_j e^{-k_j z} \tag{1.3.16}$$

where $k_j = \sqrt{2m(E - U_j)}/\hbar$, A_j is the amplitude of the forward traveling particle,

and B_j is the amplitude of the backward traveling particle. By applying the boundary conditions discussed above, each transfer matrix $\mathbf{M}_{j\to j+1}$ can be calculated as follows [8]:

$$\mathbf{M}_{j\to j+1} = \frac{1}{2}\begin{pmatrix} (1+S_j)e^{-i(k_{j+1}-k_1)z_j} & (1-S_j)e^{-i(k_{j+1}+k_1)z_j} \\ (1-S_j)e^{i(k_{j+1}+k_1)z_j} & (1+S_j)e^{i(k_{j+1}-k_1)z_j} \end{pmatrix} \tag{1.3.17}$$

where

$$S_j = \frac{m_{j+1}k_j}{m_j k_{j+1}} \tag{1.3.18}$$

To determine transmission probability, the incident amplitude A_0 is set to $A_0 = 1$, and the transmission amplitude A_{N+1}, can be calculated as:

$$A_{N+1} = \frac{m_{N+1}k_0}{m_0 k_{N+1} M_{22}} \tag{1.3.19}$$

and used to find D(E):

$$D(E) = \frac{m_0 k_{N+1}}{m_{N+1}k_0}|A_{N+1}|^2 \tag{1.3.20}$$

1.3.2 Tunneling Current Density

The method for calculating $D(E)$ shown above will now be used to calculate the tunneling current, J, of electrons in one-dimensional metal-insulator-metal tunnel junction, where regions I and III above correspond to a first and second metal layers ($Metal_1$ and $Metal_2$), respectively, and Region II corresponds to an insulating material with a non-constant potential $U(z)$. The number of electrons tunneling through the barrier, $N_{1\to 2}$, can be calculated as follows[9]:

$$N_{1\to 2} = \int_0^\infty D(E_z) v_z n(v_z) dv_z = \frac{1}{m} \int_0^\infty D(E_z) n(v_z) dE_z \tag{1.3.21}$$

where $E_z = mv_z^2/2$ is the energy of the electron along the z-direction, v_z is the velocity of the electron in the z-direction, and $n(v_z)$ is the number density of electrons per unit volume with velocity v_z.

We now need to solve for $n(v_z)$. Two assumptions are needed here to continue. First, as this is a one dimensional potential, only the component of electron motion in the z-direction is required to determine the tunneling rate. Second, an isotropic distribution of electrons is assumed for both $Metal_1$ and $Metal_2$. As such, in k-space, the elemental number density, dn, of electrons is:

$$dn = f_1(E) \frac{1}{4\pi^3} dk_x dk_y dk_z \tag{1.3.22}$$

where $f_1(E)$ is the Fermi-Dirac distribution function of $Metal_1$. Using $k = mv/\hbar$, eq. 1.3.22 can be rewritten as:

$$dn = f(E) \frac{m^3}{4\pi^3 \hbar^3} dv_x dv_y dv_z = n(v_z) dv_z \tag{1.3.23}$$

where v_x, v_y, and v_z are the velocities of the electron in the x-, y-, and z-directions, respectively. From 1.3.23 we can solve for $n(v_z)$:

$$n(v_z) = \int \int f(E) \frac{m^3}{4\pi^3 \hbar^3} dv_x dv_y \tag{1.3.24}$$

Transforming the above equation into cylindrical coordinates with ${v_r}^2 = {v_x}^2 + {v_y}^2$, $E_r = (v_x^2 + v_y^2)m/2$, $E_z = v_z^2 m/2$, and $E = E_r + E_z$ we obtain:

$$n(v_z) = \frac{m^2}{2\pi^2 \hbar^3} \int_0^\infty f(E) dE_r \tag{1.3.25}$$

and inserting into eq. 1.3.21 and applying $E = E_r + E_z$ we get

$$N_{1\to 2} = \frac{m}{2\pi^2\hbar^3}\int_0^\infty D(E_z)\int_{E_z}^\infty f(E)dEdE_z \tag{1.3.26}$$

The current density J can be calculated by subtracting the number of electrons tunneling from $Metal_2$ to $Metal_1$, $N_{2\to 1}$ from $N_{1\to 2}$:

$$J = e(N_{1\to 2} - N_{2\to 1}) \tag{1.3.27}$$

As $D(E)$ is the same in both directions[10], $N_{2\to 1}$ can be calculated the same as $N_{1\to 2}$ above, with the exception that the Fermi-Dirac distribution of $Metal_2$, $f_2(E)$ is used:

$$N_{2\to 1} = \frac{m}{2\pi^2\hbar^3}\int_0^\infty D(E_z)\int_{E_z}^\infty f_2(E)dEdE_z \tag{1.3.28}$$

The Fermi-Dirac distribution functions $f_1(E)$ and $f_2(E)$ are defined as follows:

$$f_1(E) = \frac{1}{1+e^{(E-E_{F1}+eV_1)/k_BT}}, f_2(E) = \frac{1}{1+e^{(E-E_{F2}+eV_2)/k_BT}} \tag{1.3.29}$$

where E_{F1} and E_{F2} are the fermi energies of $Metal_1$ and $Metal_2$, and V_1 and V_2 are voltages applied to $Metal_1$ and $Metal_2$, respectively.

Equation 1.3.27 now becomes:

$$J = \frac{em}{2\pi^2\hbar^3}\int_0^\infty D(E_z)\int_{E_z}^\infty (f_1(E) - f_2(E))dEdE_z \tag{1.3.30}$$

and the integral with respect to E can be solved exactly to obtain:

$$J = \frac{em^*k_BT}{2\pi^2\hbar^3}\int_0^\infty D(E_z)ln\left(\frac{1+e^{\left(\frac{E_{F1}-E_z-V_1}{k_BT}\right)}}{1+e^{\left(\frac{E_{F2}-E_z-V_2}{k_BT}\right)}}\right)dE_z \tag{1.3.31}$$

Equation 1.3.31 describes a current density for a one dimensional potential where E is the energy of the source electron, E_F is the fermi energy of the metal, $D(E)$ is the tunneling transmission probability for an electron having energy E, e is the electron

charge, m^* is the effective mass of the electron, k_B is the Boltzmann constant, $\hbar$ is the reduced Planck's constant, and T is temperature.

1.3.3 Electric Potential of an MIM Junction

This section outlines the theory behind the electric potential $V(z)$, used to calculate the potential $U(z)$ and $D(E)$ in MIM tunnel junctions. More precisely, the electric potential within the insulator layer is determined using the following theory, with the electric potential within the metal layers of the MIM assumed to be a constant potential that it determined by an applied voltage.

1.3.3.1 Poisson's Equation

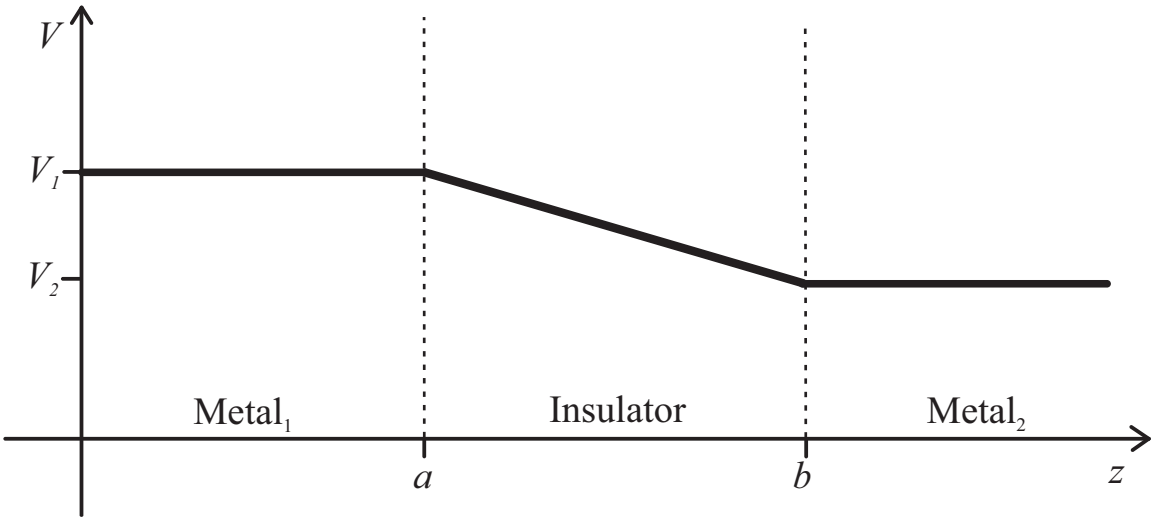

Figure 1.5: Electric potential $V(z)$ of an MIM junction with an applied voltage.

Poisson's equation, shown below, is used to determine an electric potential V given a charge density ρ and necessary boundary conditions.

$$\nabla^2 V = \frac{\rho}{\epsilon_0} \tag{1.3.32}$$

In the case of a 1D potential in the z-direction, such as the potential of an MIM tunnel junction, $\rho = 0$ and eq. 1.3.32 becomes

$$\frac{d^2V}{dz^2} = 0 \tag{1.3.33}$$

which has a general solution of $V(z) = cz + d$. Given the boundary conditions of the voltages V_1 and V_2 applied to either side the MIM junction, the resulting electric potential has a constant slope within the insulator layer, as shown in FIG. 1.5

Poisson's equation is extended to two dimensional MIM structures in this work, however as exact solutions are not possible, the finite element method is used to solve for the electric potential in 2D, and 1D potential is interpolated from the solved 2D potentials to obtain $V(z)$.

1.3.3.2 Band Structure

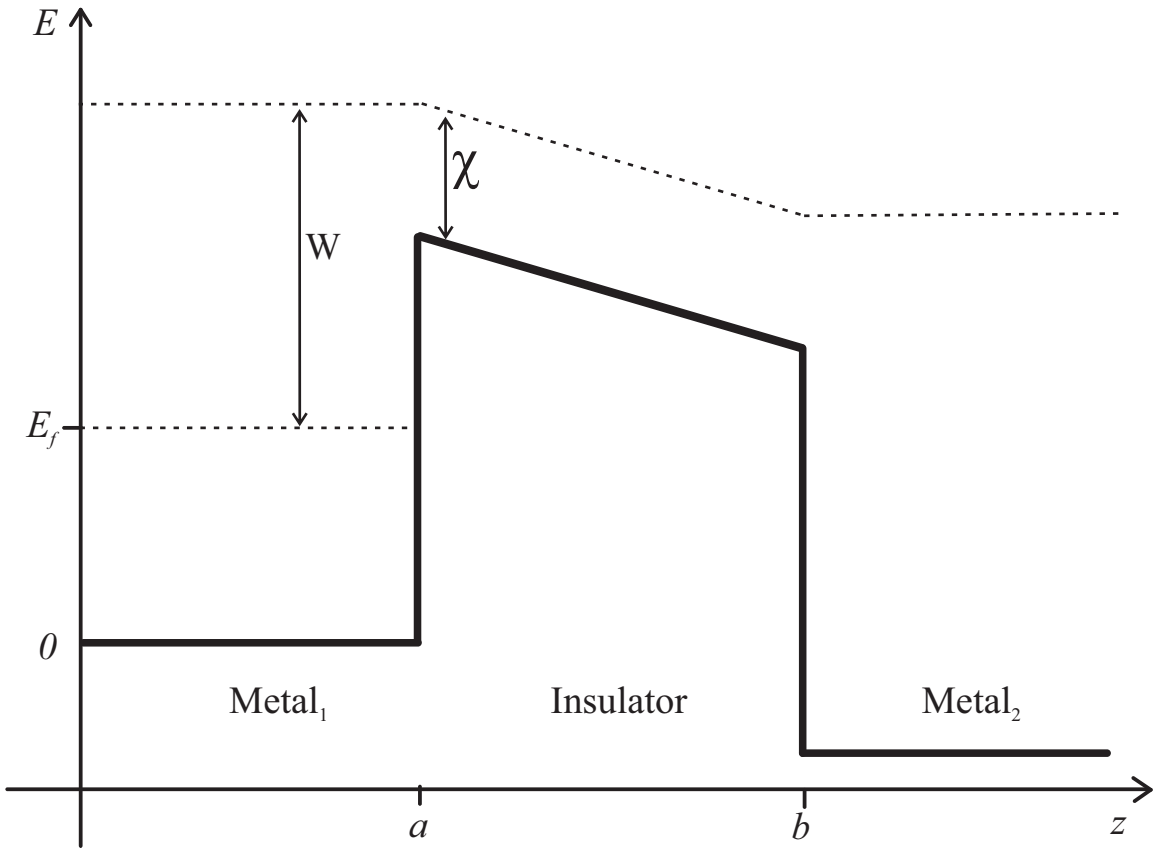

Figure 1.6: Band structure and potential $U(z)$ of an MIM junction with an applied voltage.

The electric potential $V(z)$ is distinct from the potential barrier $U(z)$ of the MIM

junction with respect to an electron in the metal layer incident on the MIM junction. $V(z)$ determines the general shape within the insulator and the "height" of the potential barrier is determined by the band structure of the MIM junction.

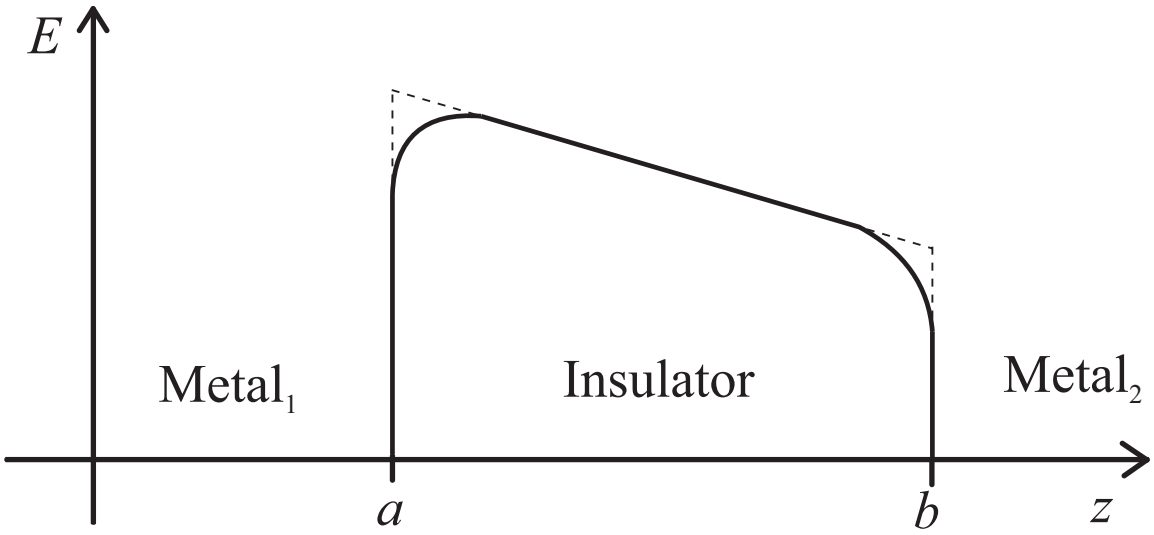

Figure 1.7: Illustration of the image charge effect contribution to the potential $U(z)$.

The height of the potential barrier seen by an electron in the metal with energy equal to the Fermi energy E_f of the metal is determined by the offset of the conductance band of the insulator and E_f. This offset is easily calculated by the difference in the work function W of the metal and the electron affinity of the insulator χ. Fig 1.6 shows the band structure of an MIM tunnel junction under an applied voltage difference between the two metal layers.

The potential barrier is also altered by the effects of image charges along the interfaces between the metal layers and insulator[10].An electron with charge $-e$ located within the insulator region at a distance d from the interface produces an electric field that is equivalent to the field produced by a particle with charge $+e$ located a distance d from the interface. This particle is referred to as an image charge and occurs at both the $Metal_1$-$Insulator$ interface and the $Insulator$-$Metal_2$ interface. These image charges with charge $+e$ the produce further image charges with the opposite interface. For example, the $+e$ image charge at distance d from

the metal1-insulator interface produces an image charge with charge $-e$ from the $Insulator\text{-}Metal_2$ interface at a distance of $2(b-a)+d$, which produces another image charge and so on, with the effect on the electric potential due to the recursive image charges decreasing with distance from the MIM junction. The image charge contribution is given by [11]:

$$U_{image}(z) = \frac{e^2}{16\pi\epsilon}\sum_{k=0}^{\infty}\left(\frac{2}{(k+1)z} - \frac{1}{kl_{Ch}+z} - \frac{1}{(k+1)l_{Ch}-z}\right) \tag{1.3.34}$$

where $l_{Ch} = b - a$ is the width of the insulator (also referred to as the length of the channel). The image charge effect reduces the height of the barrier near to the metal layers due to the inverse dependence of $U_{image}(z)$. Figure 1.7 shows an example of the top of a barrier with the image charge effect included.

The overall energy potential $U(z)$ within the insulator layer to be used when calculating $D(E)$ is given by:

$$U(z) = eV(z) + E_F + W - \chi + U_{image}(z) \tag{1.3.35}$$

1.4 Review of Electron Tunneling Devices

Various metal and insulator-based tunneling devices have been investigated and implemented. This section contains a brief overview of such devices, from those that are found in consumer electronics to others that are the topic of recent research.

1.4.1 MIM Junctions

A metal-insulator-metal tri-layer structure is the simplest physical implementation of a solid state device that has a finite potential barrier through which electrons

can tunnel. MIM junctions exhibit diode-like behaviour, as electron tunneling is a non-linear process, allowing for rectification of electric current. When compared to a semiconductor diode, MIM diodes are advantageous due to their ultrafast response time, which can be as fast as 1 femtosecond [12]. In addition to being used as rectifying diodes, MIM junctions have been developed for use as antenna-coupled infrared detectors, high-frequency mixers, optical rectennas, and switching memories [13–18]. The progress of MIM junction device development is in part thanks to innovations in atomic layer deposition and physical vapour deposition, which allows for the fabrication of high quality thin films of oxide that are required for reliable MIM devices.

Asymmetric MIM diodes, exhibit asymmetry in their current-voltage (I-V) response for reversed voltage polarity. A MIM junction may have dissimilar metal electrodes, resulting in a trapezoidal-shaped potential barrier at zero bias voltage.[19] Alternatively, metal-insulator-insulator-metal (MIIM) and metal-insulator-insulator-insulator-metal (MIIIM) devices, have been shown to have an asymmetric I-V response for reversed voltage polarity due to differing direct tunneling rates and resonant tunneling current rates depending on the polarity of the applied voltage. [20, 21] The development of asymmetric MIM junctions have demonstrated how engineering the structure of the potential barrier between the metal contacts can be used to greatly affect the I-V response of metal-insulator devices.

1.4.2 Variations of Tunneling Transistors

Various transistor devices have been developed that make use of the non-linearity of tunneling current.

The hot electron transistor, based on a metal-insulator-metal-insulator-metal or metal - insulator - metal - semiconductor structures, modulates the tunneling current through the device by altering the voltage of the middle metallic layer [22].

In recent years, variations on the hot electron transistor based on a semiconductor - metal - semiconductor, with tunneling current through Shottky barriers at the metal-semiconductor interfaces have arisen. The graphene based hot electron transistor, where a graphene layer replaces the middle metal layer, has received much attention[23].

Semiconductor based tunneling field effect transistors (TFETs) have a CMOS-style geometry and a p-type/intrinsic/n-type semiconductor tunnel junction. Operating in an analogous manner to the metal-insulator-tunneling transistor, an adjacent gate contact modulates the electric potential between the p-type source and n-type drain to permit or disallow direct band-to-band tunneling between the valence band of the p-type source and the conduction band of the n-type drain[24].

Single electron transistors operate based on tunneling current between source and drain contacts through a structure with discrete energy states.[25] The position within the potential of the discrete energy levels is controlled by a gate contact thereby allowing precise control of tunneling current.

1.4.3 Field Effect MITTs

The MITT was first theorized in 1996 by Fujimaru and Matsumura[26], based on a CMOS-style device with a planar tunnel junction and gate contact separated from a gate contact by a separate gate oxide layer. The same group later presented a functioning device based on a Ti-TiO_x-Ti tunnel junction having a channel length of 16nm. These devices were fabricated based on a conventional photolithography fabrication process. Fabrication of Ti-TiO_x-Ti devices by atomic force microscopy oxidation was also demonstrated [4]. Since then, other devices, both fabricated and proposed, have demonstrated the potential of MITTs. [27–29].

In recent years, significant attention has been given to air gap tunneling transistors (or vacuum field effect transistors), which have an analogous structure to the MITT,

only with an air (or vacuum in non-ambient conditions) replaces the insulating layer in the MIM tunnel junction channel[30]. Electron transport in these devices is ballistic in nature, however the method of controlling the current based on gate-modulation of the electric potential is similar. Typically, air gap tunneling transistors typically have channel lengths of 30nm or more [31, 32]. However, the operation of different variations of air gap transistors provide insight into how analogous changes may affect the operation of MITTs. These variations include different device geometries, such as CMOS shaped, planar, vertical, or dual gate, and different device component geometries, such as changes in ballistic electron emitter radius.

1.5 Summary and Thesis Scope

In this chapter, the theoretical framework for this thesis is introduced. The theory behind electron tunneling is discussed and a transfer matrix method solution to electron tunneling through arbitrary potential barriers is applied to calculate tunneling rates. The solution of static electric potentials and the band structure of materials are discussed. A review of metal-insulator based electronic devices is given.

Chapter 2 presents the implementation of a simulation model that applies the various theoretical concepts of chapter 1 to MITT devices having arbitrary 2D geometries. The model is implemented using MATLAB to calculate the steady state current of MITT devices. The main functions of the MATLAB program are described and brief discussion of the limitations of the model is presented.

Chapter 3 introduces the butterfly junction MITT (referred to as BJMITT) device which has a novel geometry that includes a dual gate structure. The operation of a BJMITT device that represents a feasible physical implementation is discussed in detail using the model introduced in chapter 2. The impact of varying the geometry and material on the key operating characteristics of the BJMITT is investigated.

Finally, introductory efforts into the fabrication of the BJMITT, and the results of those efforts are shown.

Chapter 4 compares the operation of the BJMITT device to a T-shaped, single gate MITT, and further demonstrates how transistor performance can be improved based on device geometry. The performance characteristics of a BJMITT and T-shaped MITT with similar dimensions are compared. A fabrication process for the T-shaped MITT is proposed.

Chapter 2

Simulation of Two-Dimensional MITT Devices

2.1 Overview

Simulations in MATLAB are used to evaluate the equations derived in Chapter one to obtain currents for the two dimensional devices shown in Figure 2.1. Generally, the program operates as follows:

1. Various parameters are set up by the user to determine material properties, and geometry of the device, along with the range of operating voltages to be solved
2. The drain and gate voltages are looped over
3. At each drain and gate voltage, a finite element method calculation is performed to obtain a two dimensional electric potential of the device
4. Along a set width of the drain and source contacts, one dimension potentials are approximated from the two dimensional potential
5. For each of the one dimensional potentials, a current density is calculated according to the equations in Chapter 1, which includes the TMM calculations

6. The calculated current densities are numerically integrated along the x-axis to obtain a current in A/m

Appendix A.1 contains the top-level function in which the user defines the scope of and begins the simulation in MATLAB. Appendix A.2 contains the program that loops over voltages and calls the other functions when necessary.

2.2 Meshing and FEM solving of Poisson's Equation

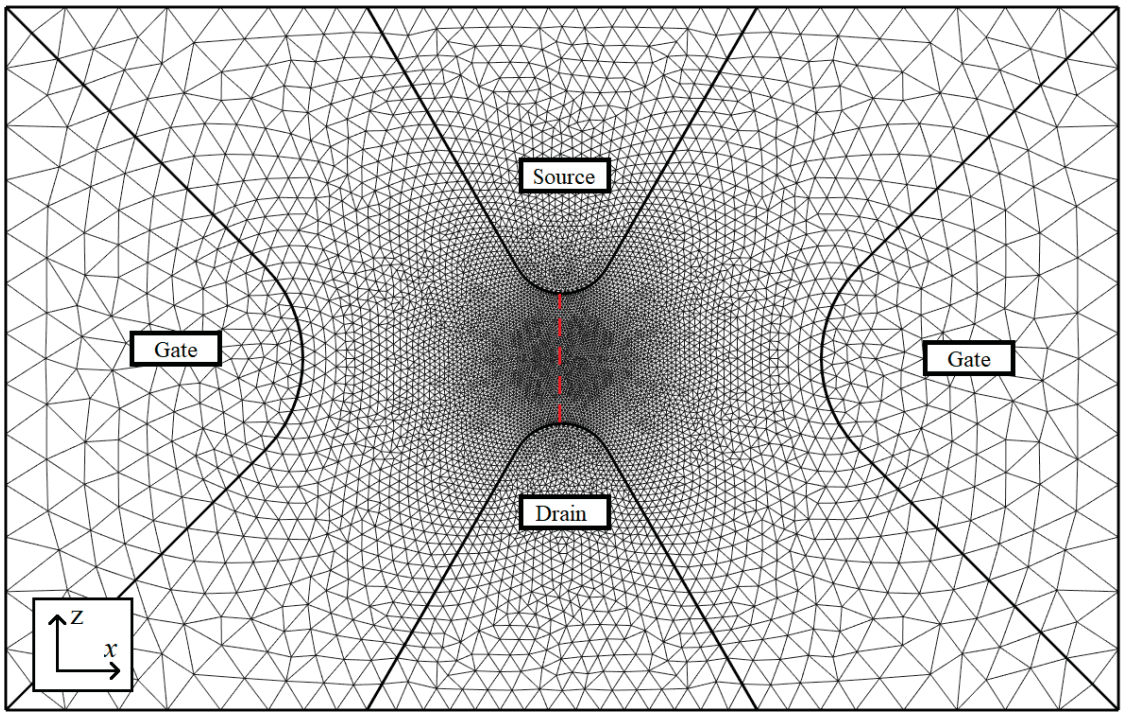

Figure 2.1: A typical FEM mesh showing higher mesh density near the active region of the device. The dotted red line shows an example of a line along which U(z) is interpolated.

The two dimensional Poisson's Equation is solved using FEM, which begins with the creation of the mesh for the structure being simulated. Referring to Figure 2.1, parameters are chosen to define the source, drain, and gate contacts of the device with the chosen geometry. Using a meshing program developed by D. Engwirda[33],

the boundaries that make up this geometry is locked, and the mesh is generated with a specified density.

Appendix A.3 contains the function which "draws" the source, gate, and drain based on the input values, and prepares the necessary variables used by the meshing program to create the mesh.

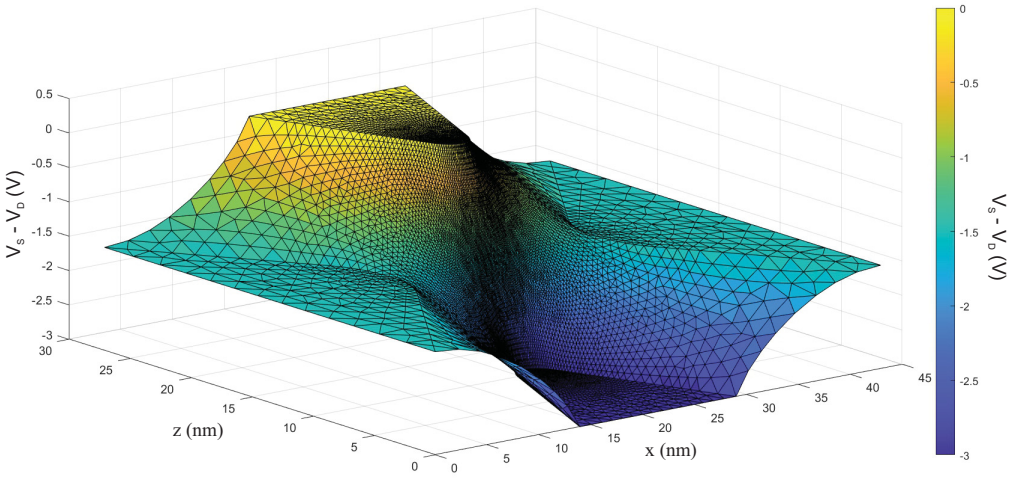

Figure 2.2: An example of the FEM solution showing the device potential. The colourbar indicates the voltage relative to the source contact.

Referring to FIG. 2.1, the density of the mesh is increased in the area between the source and drain, as that is the active region of the device, and requires a higher degree of accuracy to provide results. Typically, the side lengths of the triangles are up to about 2.5nm in length near the boundaries, and as small as about 0.1nm between the source and drain. The width and height of the simulated device is chosen to minimize any effects of the boundaries on the active region, with the density of the mesh further away from the active region being increased to reduce computation time.

Open boundary conditions are set along the edges of the simulation area and the source, drain, and gate contact voltages are pinned to the chosen values. An example output of the FEM solution of the program is shown in Figure 2.2, with the source

set to 0V, the drain set to -3V and the gate contacts set to 1.5V.

From the obtained solution of the potential in the active area, a plurality of one-dimensional potentials are interpolated. The one dimensional potentials are gathered along straight lines between the source and drain (in the z-direction) along set intervals (along the x-direction), as shown in red in Fig. 2.2.

Appendix A.4 contains the function that evaluates Poisson's equation.

2.3 Calculation of the Tunneling Current

The program calculates currents based on eq. 2.3.1 below [8], which gives the drain current per unit height, I_D, (i.e. tunnel electron flow from source to drain) at a particular drain voltage, V_D, and gate voltage, V_G, over the voltage range between $0V$ and $3V$ using:

$$I_D = \frac{em^* k_B T}{2\pi^2 \hbar^3} \int_{x_1}^{x_2} \int_{E_{min}}^{E_{max}} D(E,x) \cdots \cdots ln \left(\frac{1 + e^{\left(\frac{E_F - E - V_S}{k_B T}\right)}}{1 + e^{\left(\frac{E_F - E - V_D}{k_B T}\right)}} \right) dEdx \tag{2.3.1}$$

where E is the energy of the source electron, E_F is the fermi energy of the metal used for the source and drain, $D(E)$ is the tunneling transmission probability for an electron having energy E, x_1 and x_2 are the edges of the channel width, E_{min} and E_{max} are the minimum and maximum energies of the tunneling electron, respectively, e is the electron charge, k_B is the Boltzmann constant, $\hbar$ is the reduced Plancks constant, temperature $T = 300K$, and V_S and V_D is the voltage applied to the source and the drain, respectively. In the example shown in this chapter, the metal used in the source, drain, and gate is Au, and the insulator is ZrO_2, $w_{Ch} = x_2 - x_1 =$ 3.46nm and $E_{min} = E_F - 1.5$eV and $E_{max} = E_F + 0.5$eV. It should be noted that $T = 300$K, the contribution to the tunneling current from electrons with energy above

$E_{max} = E_F + 0.5\text{eV}$ or below $E_{min} = E_F - 1.5\text{eV}$ is negligible and the drain current is dominated by current tunneling near the Fermi energy. For the tunneling current shown in FIG. 2.3, the current density per unit energy at the peak around $E = E_F$ is more than $10^3\times$ larger than at E_{min}, and more than $10^5\times$ larger than at E_{max}. Both E and x are divided into a linear space of data points.

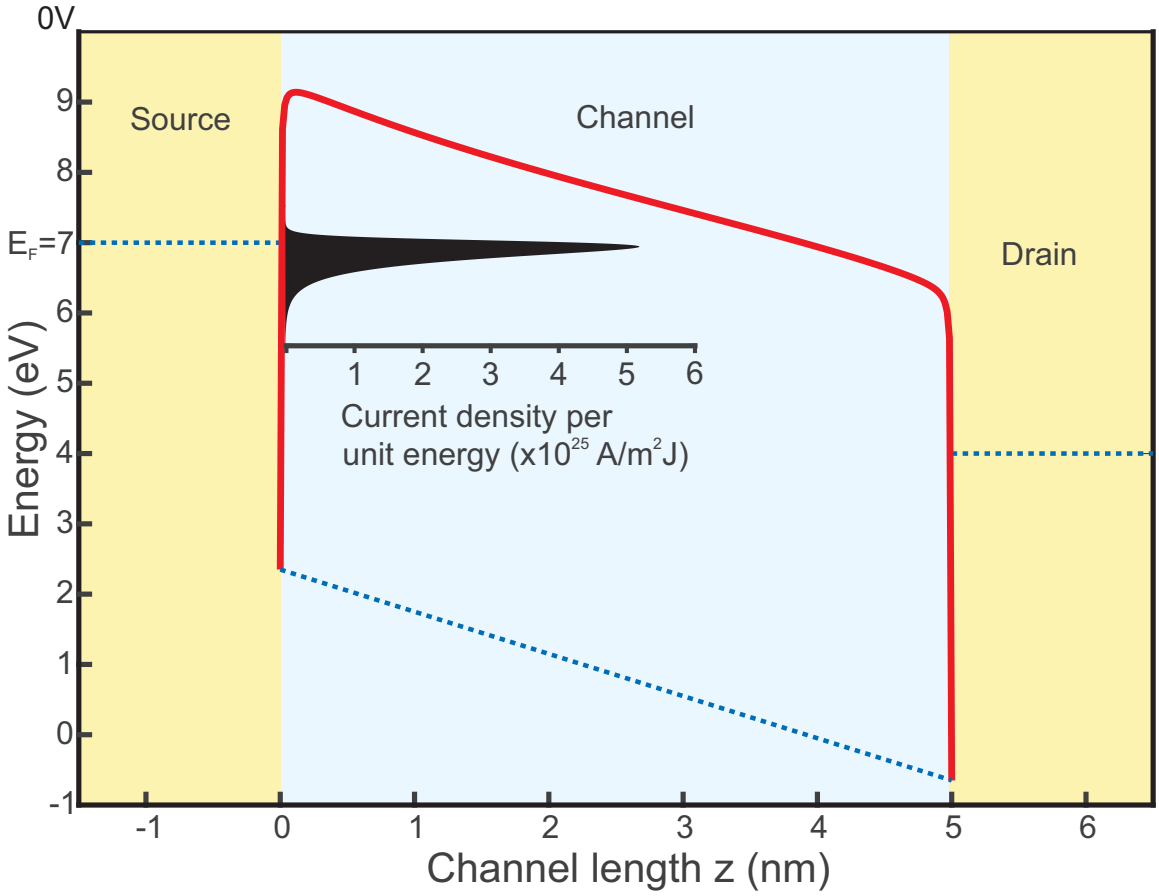

Figure 2.3: Calculated current contribution per unit energy shown with the 1D potential for which the current was calculated.

Eq. 2.3.1 is not solved as one, rather it is broken down step by step as the program loops through the simulated values. To start, for each value of x, the 1D electric potential along z is interpolated from the 2D electric potential, converted to the potential barrier $U(z)$, and the image charge effect (using eq. 1.3.34) and the band structure (using eq. 1.3.35) are applied. The resulting 1D potential barrier, shown in red in Fig. 2.3, is used to calculate the current contribution at each energy

value E.

At each energy level E in the approximation, $D(E)$ is calculated using TMM calculations detailed in section 1.3.13 and multiplied by the log factor in the integral to obtain a vector of "current density per energy" values J_E:

$$J_E = D(E,x) ln \left(\frac{1 + e^{\left(\frac{E_F - E - V_S}{k_B T}\right)}}{1 + e^{\left(\frac{E_F - E - V_D}{k_B T}\right)}} \right) \tag{2.3.2}$$

At each voltage state of the device, the program loops over energy levels from E_{min} to E_{max}. In reality, the energy integral should be calculated from zero to infinity, however this procedure is impractical and wasteful, as the contributions to the current from electrons at energy levels both significantly above and below the fermi level of the metal are negligible, as discussed above. In theory, the maximum energy of an electron within the metal layers would be $E = E_F + W$, with any electrons having an energy higher than that being ejected from the metal. However, using this maximum would be wasteful in calculations due to negligible contribution to the current.

Fig. 2.3 depicts an example of the current contribution (per energy level) superimposed on the corresponding potential barrier for which is it calculated. The area, shaded in black, of the current contribution is a current density $J(x)$ in A/m^2. As expected, the current contribution increases slowly as the energy of electrons increases, and then decreases rapidly after the fermi energy of the metal is passed. The values of J_E are used to obtain a value for the current density $J(x)$ using a trapezoidal approximation of the following integral:

$$J(x) = \frac{e m^* k_B T}{2\pi^2 \hbar^3} \int_{E_{min}}^{E_{max}} D(E,x) ln \left(\frac{1 + e^{\left(\frac{E_F - E - V_S}{k_B T}\right)}}{1 + e^{\left(\frac{E_F - E - V_D}{k_B T}\right)}} \right) dE \tag{2.3.3}$$

Fig. 2.4 depicts a typical current density plot along the z-direction for the devices in this work, superimposed over the approximate location of the active region of the devices. To obtain the final value of current I_D the following integral is solved using

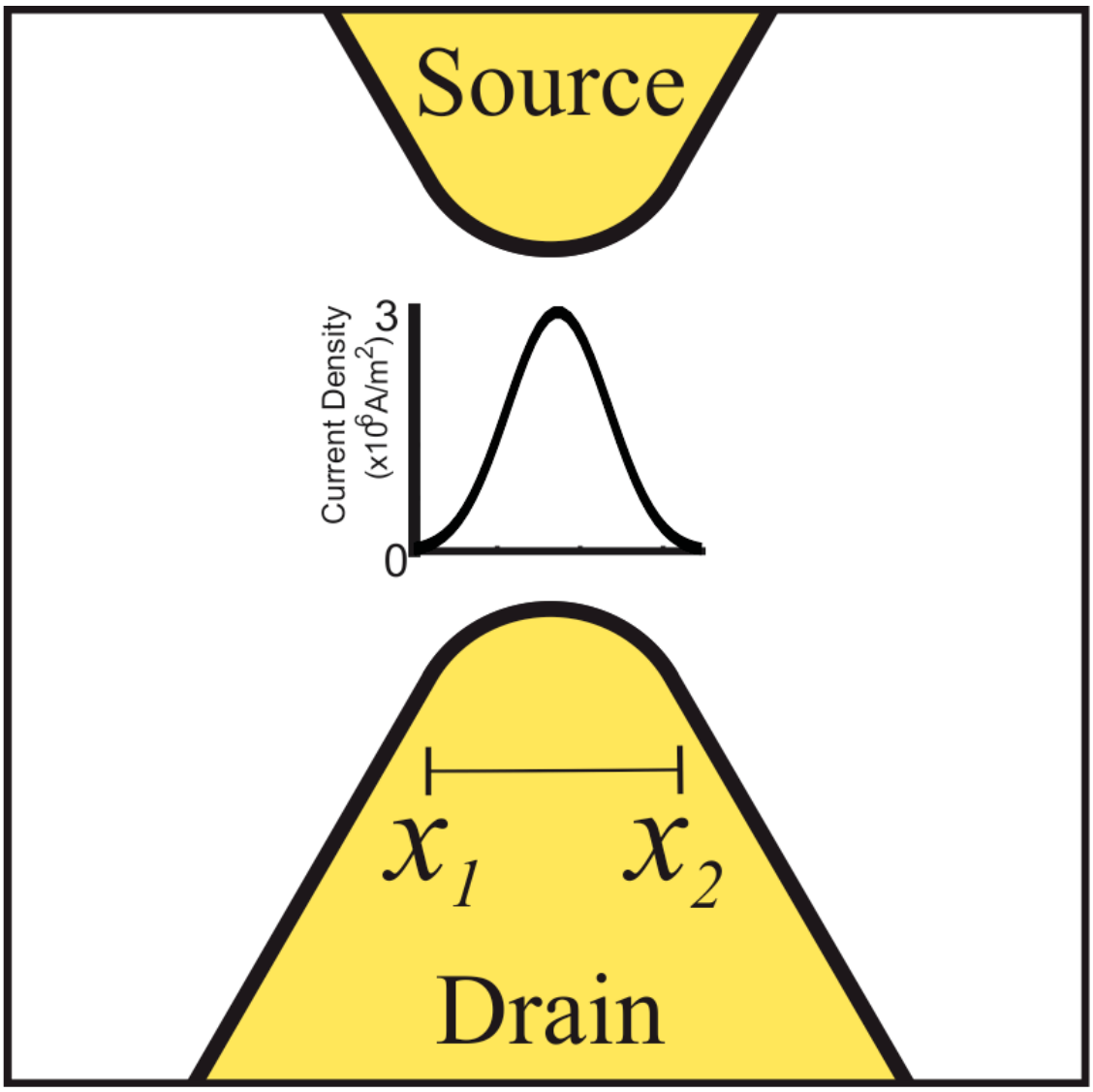

Figure 2.4: Calculated current density at the approximate location in the x-direction where the current travels.

a trapezoidal approximation:

$$I_D = \int_{x_1}^{x_2} J(x)dx \tag{2.3.4}$$

Similar caveats apply to the values of x_1 and x_2 as with E_{min} and E_{max}, which are chosen keeping computation time and practicality in mind, with the knowledge that negligible amounts of current contribution is missing. For the example shown, the current density at $x = (x_1 + x_2)/2$ is more than 70× greater than the current

density at $x = x_1$.

Appendix A.5 presents the function that evaluates the values of $D(E)$

2.4 Comparison with Fowler-Nordheim Equation

To verify the accuracy of the model, the $I_D - V_D$ curve at $V_G = 1.5V$ is compared to a current-voltage curve obtained by solving the Fowler-Nordheim (FN) equation[34] in the field emission regime ($V_D > (W_{Au} - \chi) = 2.35$V) for a 5nm long linear gradient potential barrier.

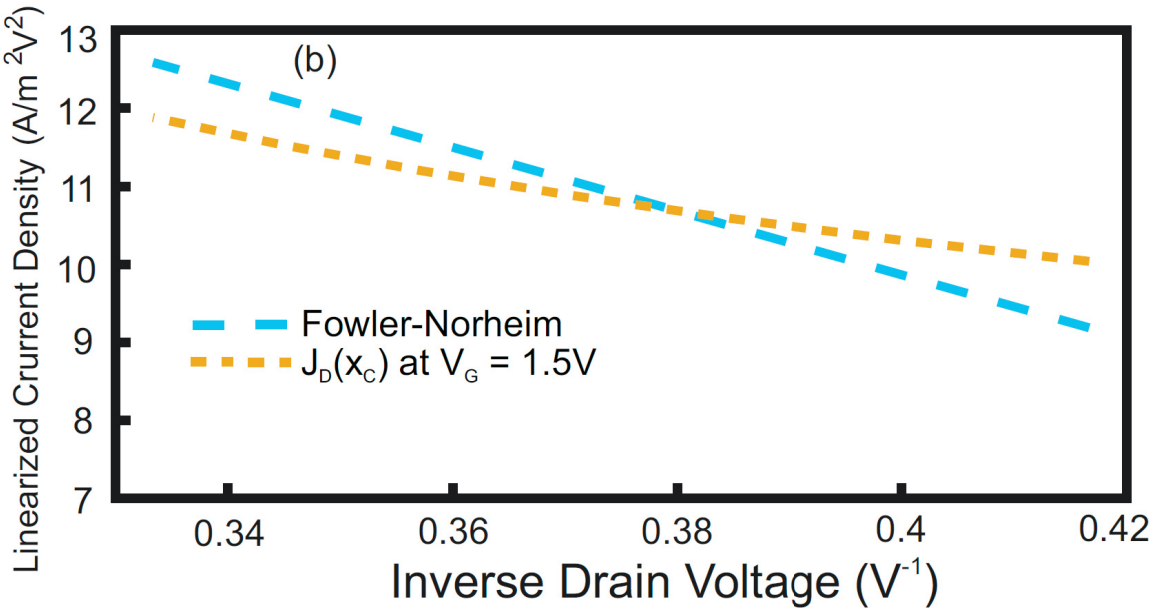

Figure 2.5: Comparison of the current calculated using the simulated model and the claculated Fowler-Nordheim current for a triangular barrier of similar shape.

The linearized plot (i.e. $ln(J/V^2)$ vs. V_D^{-1}), presented in Fig. 2.5, shows similar values are obtained through both of the FN equation, and the simulation results. The clear difference in slope of the linearized current densities between the BJMITT and the FN equation further reinforces the accuracy of the model, as these differences are expected and predictable. At the onset of field emission ($V_D = 2.35$V), the greater current density from the simulation is attributed to the inclusion of image charge effects in eq. 1.3.3.4 shortening the effective barrier length by $\sim$ 0.2nm (at E_F)

when compared to the linear barrier used in the FN equation. At higher voltages, where $1/V_D < 0.38\text{V}^{-1}$, the lower current density of the simulation is attributed to the geometry-induced field enhancement lengthening the effective barrier when compared to the linear barrier. The Fowler-Nordheim equation alone does not account for these factors.

2.5 Limitations of the Model

It needs to be acknowledged that the model introduced in chapter 1 and chapter 2 is not without its limitations which will be discussed herein. As a result, some of the simulated results presented in chapters 3 and 4 are likely to be unphysical, in the sense that this model does not account for certain phenomena, which are discussed below. Wherever applicable, it is noted where the data presented is likely to be unphysical.

2.5.1 Band Structure

In chapter 1, it is assumed the band structure of the material in the active region equivalent to the band structure of the bulk material. For a realized device, the nanostructured nature of the active region of the simulated devices likely introduces localized aberrations in the band structure of both the metal contacts and the insulator within the channel. For example, it is assumed that the transition between materials as shown in the band structure is explicit and non-gradual. It has been shown that the band structure of an MIM junction may take on the behaviour of a gradual shift the barrier between a metal and an insulator. Such an effect would undoubtedly affect the electronic performance of a MITT device.[35]

2.5.2 Idealized Geometry

While care was taken to ensure the simulated device is feasible in term of dimensions and material, achieving the perfectly circular geometry used in the simulations using conventional fabrication techniques is not possible. The program, as used, requires specific set-up to simulate device with a specific geometry. In this thesis, idealized geometries are investigated; however, the functionality exists to expand to other geometries. In particular, should a real device be constructed, the program has the flexibility to simulate a geometry to match such a real device.

The atomic structure of the materials is also not included in the model. With feature sizes that approach 1nm or less, the geometry of a physical device would be affected by the crystal structure of the various materials, or even the placement of individual atoms.

2.5.3 Other Mechanisms of Electron Transport

The model could be improved by including other mechanisms of electron transport.

Non-homogeneous crystal structure may give rise to defects in the active region; such defects are likely to occur due to the complex geometry. For example, thin films of dielectric material grown via ALD on high-aspect ratio structures are unlikely to form a perfect crystal at a region between two vertical faces, where the two planes of growth meet[36]. These defects may provide localized available energy levels within the dielectric layer, below the conduction band, through which electrons could tunnel. This so called trap-assisted tunneling, well described by the Poole-Frenkel effect, would likely affect transistor performance.[37]

While tunneling current due to trap-assisted tunneling may be considered detrimental leakage current in the context of the devices studied herein, the potential for engineering the defects to enhance transistor performance is of interest. This is discussed in more detail in a later section of this thesis.

2.6 Summary

In this chapter, a simulation model for MITTs is introduced. The simulation model uses various theoretical conclusions introduced in chapter 1 to simulate 2D MITT devices. The model is able to be adapted for any 2D structure.

Chapter 3

Butterfly Junction Metal Insulator Tunneling Transistor

3.1 Introduction

Previous studies of MITT devices focused on large-scale (∼15-30nm) tunnel junction, and did not address the challenges realized in sub-10nm tunnel junctions[27–29]. Large channel length acts as a proof of principle for MITT operation; however, they do not provide accurate current-voltage characteristics. In a MITT device, it is critical to have the gate contact as close to the junction area as possible. However, for small channels (<10nm), the main challenge has been the shallow penetration of the gate electric field into the channel region when the channel length is narrowed[38]. While enhancing the penetration depth can be achieved by having the gate very close to the source and drain, gate to source/drain leakage current becomes inevitable. If the distance between the gate and source/drain is less than the channel width, the leakage current can exceed the tunneling current by orders of magnitude and thus rendering the device to be ineffective[39]. Furthermore, unlike a typical metal-oxide-semiconductor field-effect transistor (MOSFET) device where the channel is formed

by attracting carriers to the gate and conductance occurs only in a small portion of the source-to-drain junction surface area, in a MITT device, the channel is the entire area of the source-to-drain junction. As such, to modulate the potential barrier between the source and the drain, the induced electric field from the gate must penetrate the entire area of the channel. For optimal the modulation of current, the depth of the channel cannot exceed the width of the channel.

While it is necessary to recognize and accept that previous planar MITT reports incorporate idealized geometries, it is important to realize that a MITT device having a channel length of ∼5nm cannot be constructed with material boundaries having sharp, 90° corners, short of being constructed atom by atom. These highly unrealistic features are located at the edges of the source and drain near to the gate where the potential barrier is modulated. Since this region is most critical area for MITTs[39], and determines the current-voltage (IV) characteristic of the MITT, small deviations can lead to unphysical results. Furthermore, image charge effect introduces significant potential barrier lowering for tunnel junctions of 5nm and must be included to obtain accurate IV characteristics.

Here, we present a new class of planar MITT devices. The butterfly junction metal insulator tunneling transistor (BJMITT) consists of a dual gate, a source, and a drain of thin film metallic contacts embedded in a thin insulating dielectric. The geometry of the BJMITT is a manifestation of a realistic representation of a feasible device. A proposed fabrication process for the device is discussed later in this chapter. The shape and material for the proposed device are chosen with both device performance and fabrication in mind. The BJMITT design allows for complete gate electric field penetration into the channel and low leakage current density.

3.2 Device Overview

3.2.1 Device Geometry

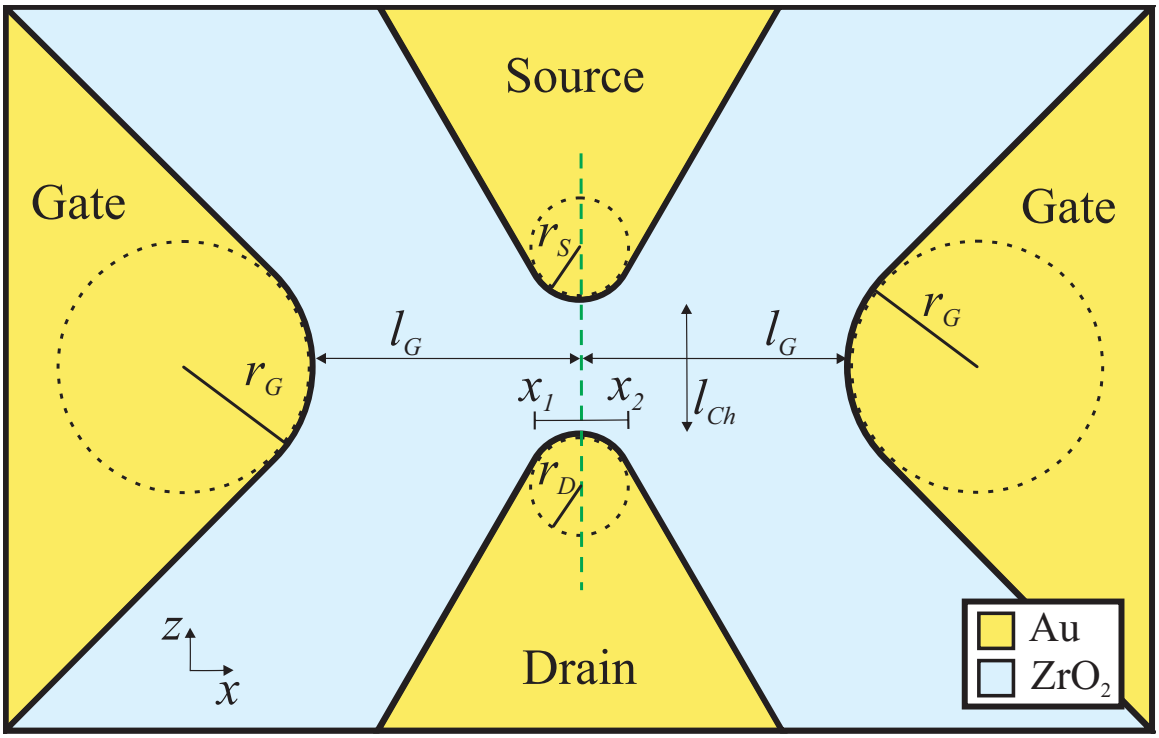

Figure 3.1: Basic two-dimensional geometry of the BJMITT.

Fig. 3.1 illustrates the two-dimensional geometry of the BJMITT device. Unlike previously reported devices, the butterfly junction is based on a tapered configuration to enable a complete gate electric field penetration into the entire channel, while also significantly reducing leakage current to either the source or to the drain. Here, both the source and drain contacts adiabatically taper to a radius $r_S = 2$nm to form a very narrow tunnel junction having a minimum length $l_{Ch} = 5$nm across which electrons tunnel in response to an applied source-drain voltage (V_D). Dual gate contacts on either side of the tunnel junction, tapered to a radius $r_G = 5$nm, are located a distance $l_G = 10$nm from the source and drain tips. The gate contacts are close enough to alter the electric potential along the whole length of the tunnel junction via the field effect, while at the same time far enough away to inhibit significant electron tunneling

to either the source or the drain. In this respect, the tunneling electrons originate from the source; therefore, when the source is held at ground (i.e. $V_S = 0$V), and the drain voltage V_D is raised, it allows a flow of tunneling electrons from the source. In the OFF state, when the gate voltage, V_G, is set to 0V, it raises the channel potential and increases the effective tunneling length experienced by an electron tunneling from the source to the drain. In the ON state, when V_G is set to be greater than V_S, the channel potential decreases which in turn decreases the effective tunneling length.

3.2.2 Device Material

To highlight and characterize the IV characteristics of the BJMITT, the source (S), drain (D) and gate (G) metallic contacts are made of gold, and the dielectric insulator is taken to be a high electron affinity ZrO_2. The following material parameters are used in the calculations: Au work function, $W_{Au} = 5.1$eV[40]; ZrO_2 electron affinity, $\chi = 2.75$[41]; electron effective mass in ZrO_2, $m^* = 0.1m_e$[42], where m_e is the electron mass; and ZrO_2 dielectric permittivity, $\epsilon = 25\epsilon_0$[39], where ϵ_0 is the permittivity of free space.

Gold is chosen for the gate contacts strictly because gold does not form a native oxide. This is required for the proposed fabrication method to work, as using a material that does form a native oxide introduces challenges that go beyond the scope of this work. At the scale required for this device to function, introducing an insulating layer of 3nm thickness at the active region of the device goes beyond fabrication feasibility within the University of Alberta NanoFab. In later sections of this chapter, variations on the material used are investigated; however, it is with the understanding that these variations do not fall under the scope of the fabrication process of section 3.7. There are obvious operational advantages to using metals other than gold for the contacts; primarily, using a metal with a lower work function than gold, will increase tunneling current.

ZrO_2 is chosen as the channel insulator for it's high electron affinity. It is preferable to use a material combination in which the potential barrier height $(W - \chi)$, in eV, is less than the breakdown voltage of the channel in V. If the source-to-drain breakdown voltage of the channel were to be reached before the tunneling current entered the field emission regime, there would be no ability to change the effective tunneling length of the channel by lowering the gate field.

3.3 Device Operation

Using the program introduced in chapter 2, Poisson's equation is solved for an Au-ZrO_2 BJMITT having $l_G = 10nm$, $l_{Ch} = 5$nm, $r_S = r_D = 2$nm and $r_G = 5$nm. The resulting 2D electric potentials in the ON and OFF states are depicted in Fig. 3.2a and Fig. 3.2b, respectively. Notably, it can be seen that the electric potential of the entire width of the channel is modulated as V_G is changed between the ON and the OFF states. In this configuration, the current characteristics of the BJMITT are independent of the penetration depth of the gate field.

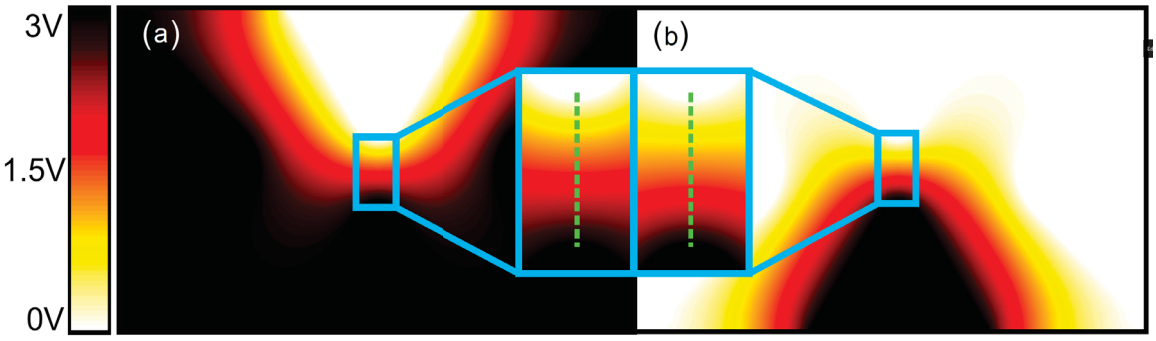

Figure 3.2: 2D device potential in the (a) ON and (b) OFF states.

The change in the potential energy $U(z)$ between the ON and OFF state determines I_D change. For a 5nm junction at $V_D = 3$V, shown in Fig. 3.3, the difference between V_G values of $0V$ (black) and $3V$ (red) is evident. To show that the geometry of the channel and the image charge strongly influence the potential barrier shape, a

simplistic triangular barrier without the image charge effects correction (dashed blue line) is plotted on the same figure. The geometry induced electric field enhancement at the sharp tips of the source and drain contacts modify the barrier shape close to their proximity. This is evident when comparing the ON state potential barrier and the triangular barrier at $z = 4.5$nm. Even though the ON state potential barrier is lowered by both the gate field and image charge effects, it remains 0.01eV higher than the triangular potential.

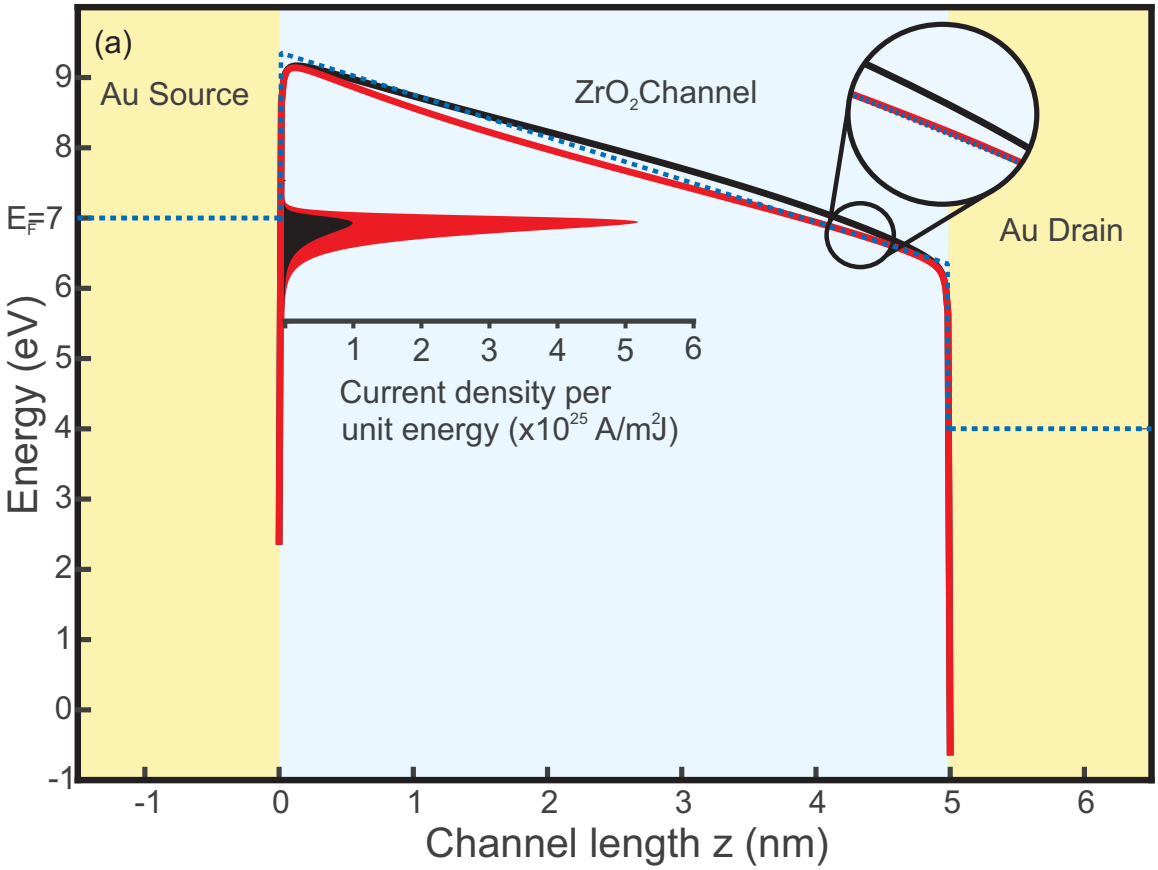

Figure 3.3: 1D device behaviour for the ON state and the OFF state. The current contribution per unit energy is shown superimposed on the potential at the energy level where the contribution takes place.

Switching the BJMITT from the OFF to the ON state results in a maximum barrier drop of 0.267eV at $z \sim 2.5$nm. The potential barrier near the source and drain is not significantly influenced by the gate field due to pinning of the electrostatic potential to the V_S and V_D voltages. Most importantly, however, is that the potential

barrier drop imparts a corresponding reduction in the effective tunneling length of 0.29nm ($\sim$ 6% of the l_{Ch}) at $E = E_F$ which in turn increases $D(E_F)$ by 302%. The influence of the enhanced transmission probability on the current density per unit energy is clearly illustrated in Fig. 3.3 between the ON state (5.2×10^{25}A/m^2·J) and OFF state (1.0×10^{25}A/m^2·J). While the energy potential shown in Fig. 3.3 occurs along the channel center x_C, the current density $J_D(x)$ across the entire width of the channel between x_1 and x_2 is being modulated by V_G, as indicated in Fig. 3.4. Notably, in this configuration, the current characteristics of the BJMITT are independent of the penetration depth of the gate field.

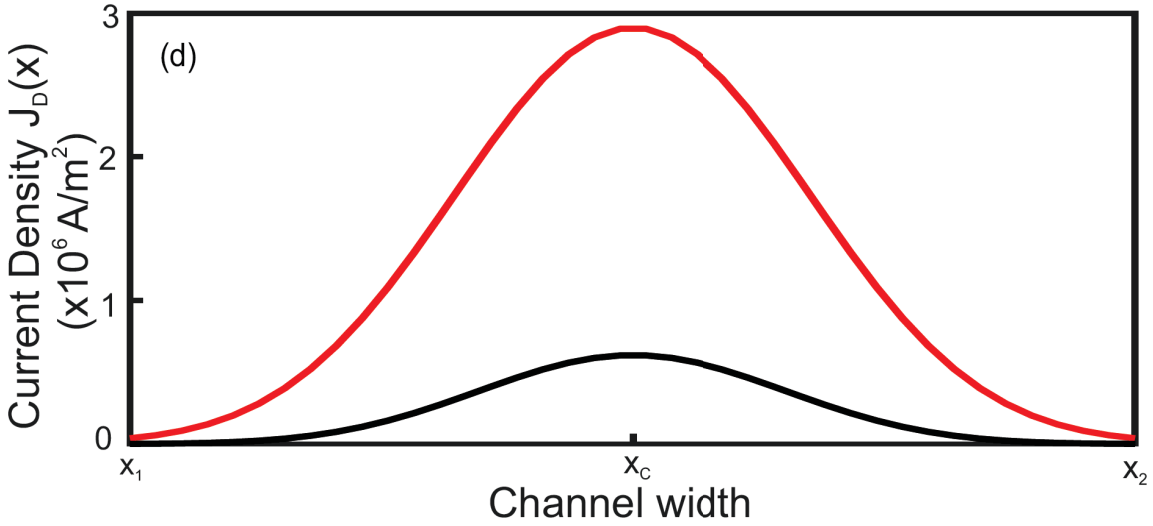

Figure 3.4: Tunneling current density along the width of the channel.

3.4 Device Characterization

3.4.1 Transistor Performance

The steady state performance of the BJMITT is evaluated primarily based on three characteristics. These characteristics are the ON/OFF ratio, which is the ratio of I_D at $V_G = 3V$ and $V_G = 0V$, the subthreshold swing (SS) at $V_D = 3V$, and the total current I_D. For discussions herein, when values of these characteristics are being

compared, a better performing device would have a larger ON/OFF ratio, and a smaller SS, with a larger current I_D being preferred, however with less importance than the ON/OFF ratio or SS.

A key parameter that determines the performance of a transistor is the $I_D - V_D$ behaviour as a function of V_G. The $I_D - V_D$ relationship of the BJMITT is depicted in Fig. 3 and clearly shows how the exponential $I_D - V_D$ response of the tunnel junction can be modified by the application of V_G. At $V_D = 3$V, the current density is $0.8{\times}10^{-6}$mA/μm at $V_G = 0$V and increases by 550% to $4.4{\times}10^{-6}$mA/μm at $V_G = 3$V for an ON/OFF ratio of 5.5. Notably, such a current increase is achieved with only a 10% decrease of effective tunneling length.

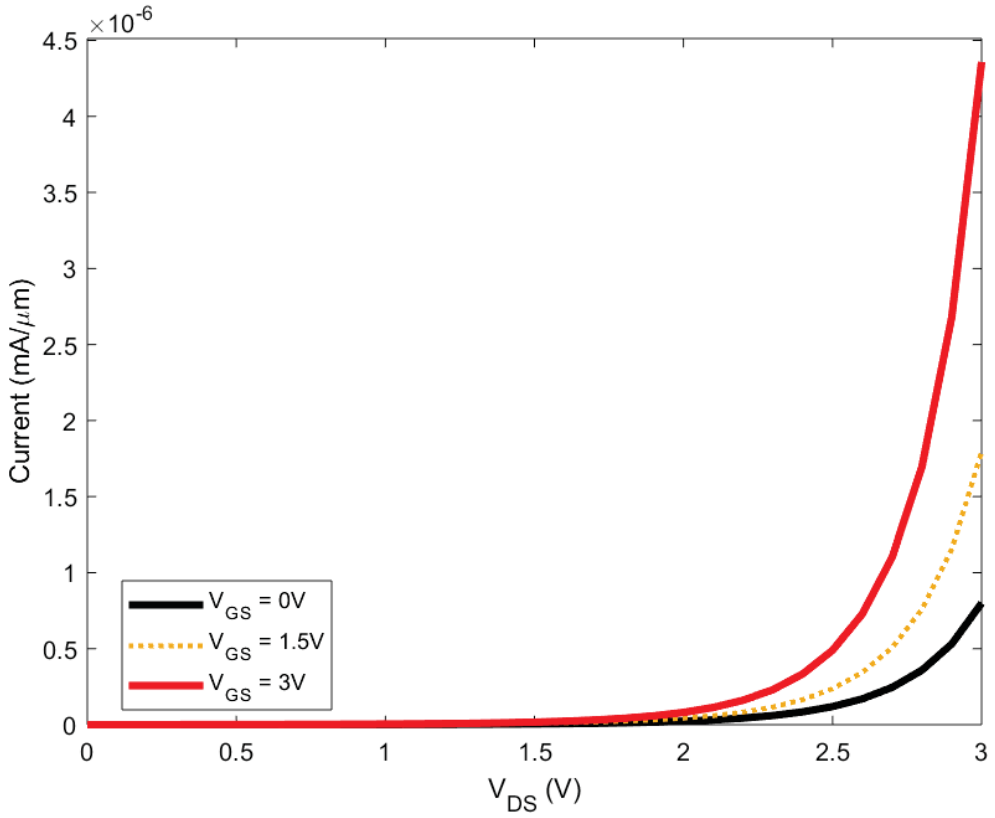

Figure 3.5: Channel current vs. source-drain voltage for different values of gate voltage.

Another parameter that need to be considered is the I_D-V_G behaviour while V_D is held constant. The I_D-V_G behaviour at $V_D = 3V$ is depicted in Fig. 4. The BJMITT

exhibits a minimum sub-threshold swing (SS) of 3.73V/dec, which is comparable to previously reported devices[5].

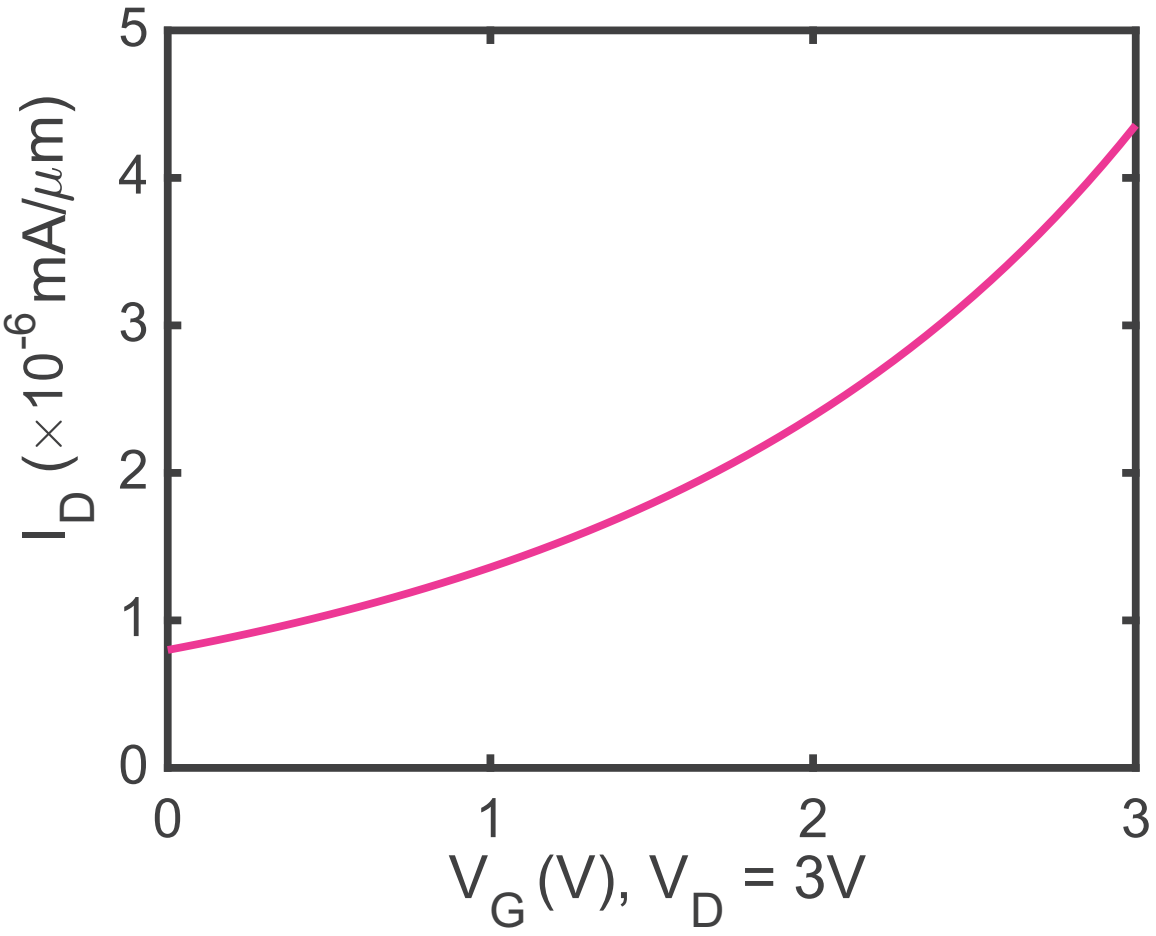

Figure 3.6: The I_D vs V_G behaviour of the BJMITT at $V_D = 3$V.

3.4.2 Leakage Current

As shown in Fig. 3.7, the maximum channel current density $J_D(x_C)$ is clearly greater than the maximum gate leakage current density $J_{leakage}$ between the source and the gate contacts. At $V_D = V_G = 3$V, the channel current density is more than $10^4\times$ greater than the leakage current density. Here, $J_{leakage}$ is calculated for the minimum distance between the gate and source contacts, and any contributions to the tunneling current density from other locations on the gate contacts will be lower than $J_{leakage}$.

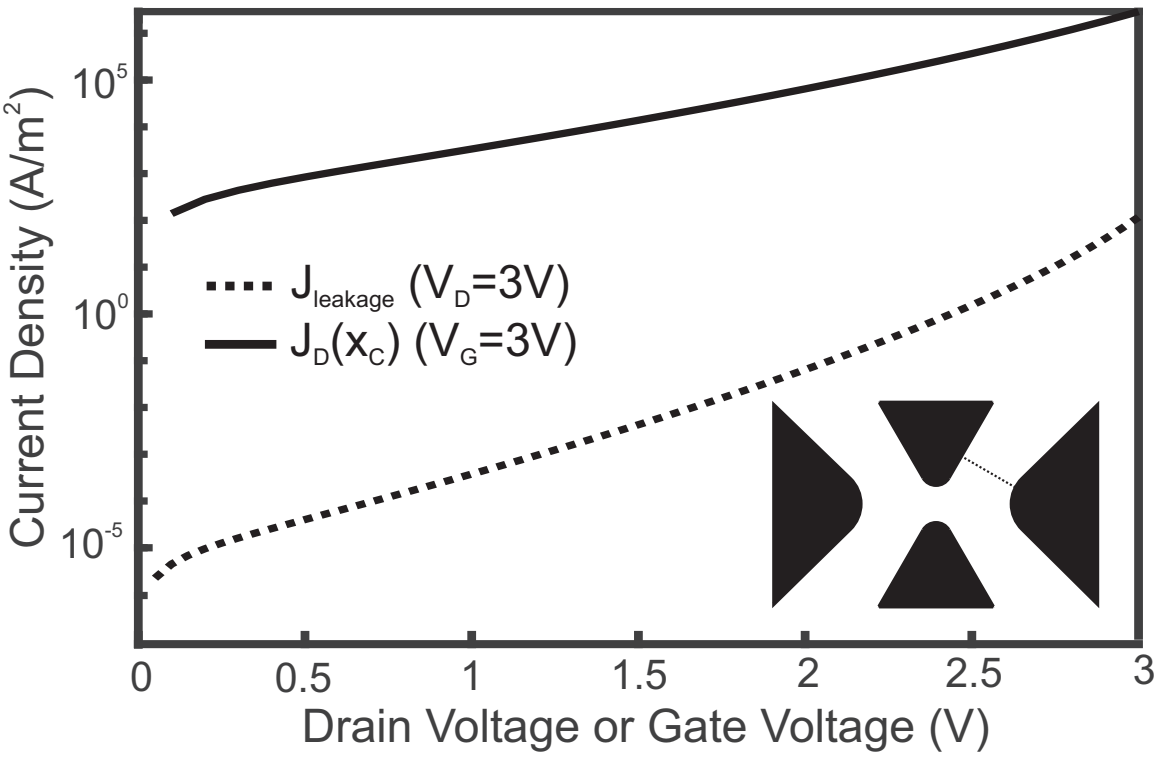

Figure 3.7: Leakage current density, $J_{leakage}$, compared to channel current, $J_D(x_C)$. Inset: device schematic indicating the line along which the leakage current density was calculated.

The main pathways for leakage current is dependent on the state of the device, as illustrated in Fig. 3.8. Here, the field distribution of the BJMITT is shown for the ON and OFF states. In the ON state, the leakage current occurs between the source and gate contacts, and is at a maximum at the two locations on the gate contacts that are closest the source contacts. Since the device is symmetric, the same leakage pathways exist for the OFF state, except the leakage current occurs from the gate contacts to the drain contact.

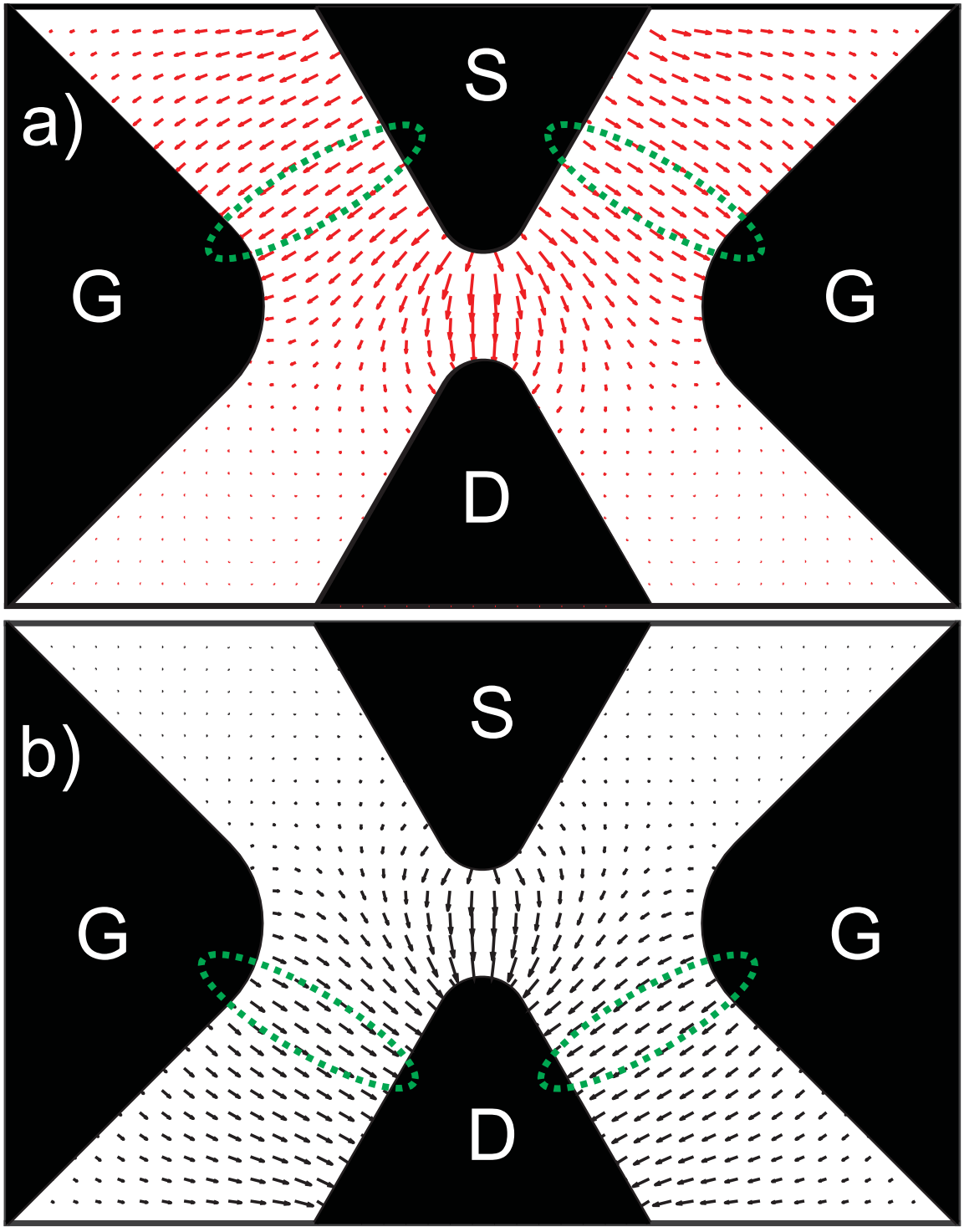

Figure 3.8: Electric field distribution. (a) ON and (b) OFF states. The paths of the main leakage currents are identified as the dotted regions.

3.4.3 Change in Operating Temperature

Referring to Fig. 3.9, the effect of the operating temperature on device performance is shown. In both the ON and OFF states, increasing temperature leads to a small increase in current magnitude, which is more pronounced in the ON state. This leads to a small improvement in performance characteristics at higher temperatures where, between 100K and 350K, the ON/OFF ratio increases from 5.3 to 5.5, and the SS decreases from 3.8V/dec to 3.6V/dec.

For the model used, the input temperature mainly affects the electron distribution around the fermi energy of the metal. Lower temperatures have a sharper drop off in energy state occupation above the fermi energy. As this change is the same in both the on state and the off state, the relatively minor change vs. temperature is expected.

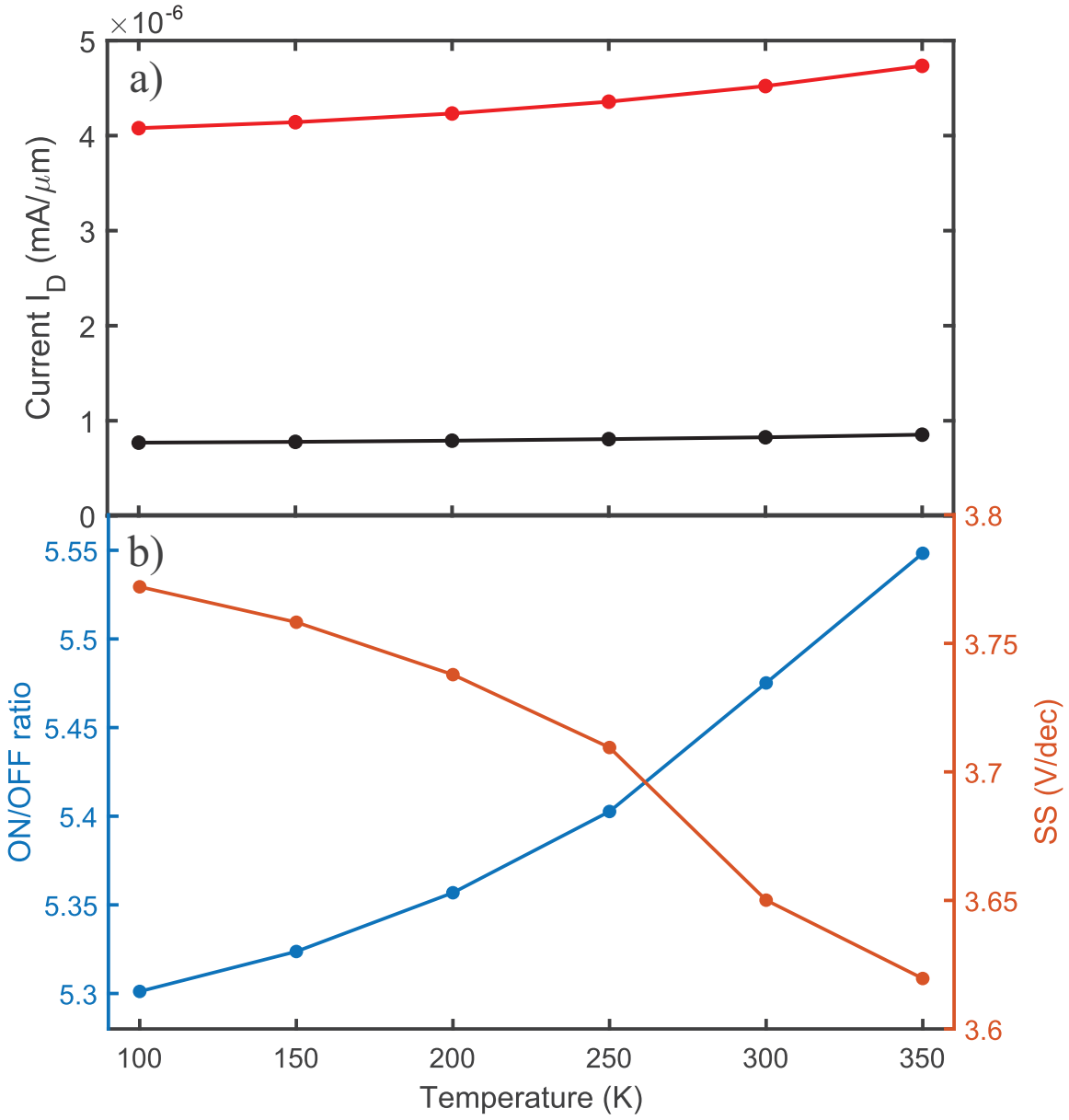

Figure 3.9: a) ON (red) and OFF (black) current vs. temperature. b) ON/OFF ratio and SS vs. temperature.

3.5 Geometry-Dependent Device Operation

In this section we study the dependence of the transistor performance of the BJMITT on the geometry of the active region. In particular, we will look at how altering various geometric parameters away from what is presented in section 3.2 affects the ON/OFF ratio and the sub-threshold swing at $V_D = 3V$.

3.5.1 Channel Length

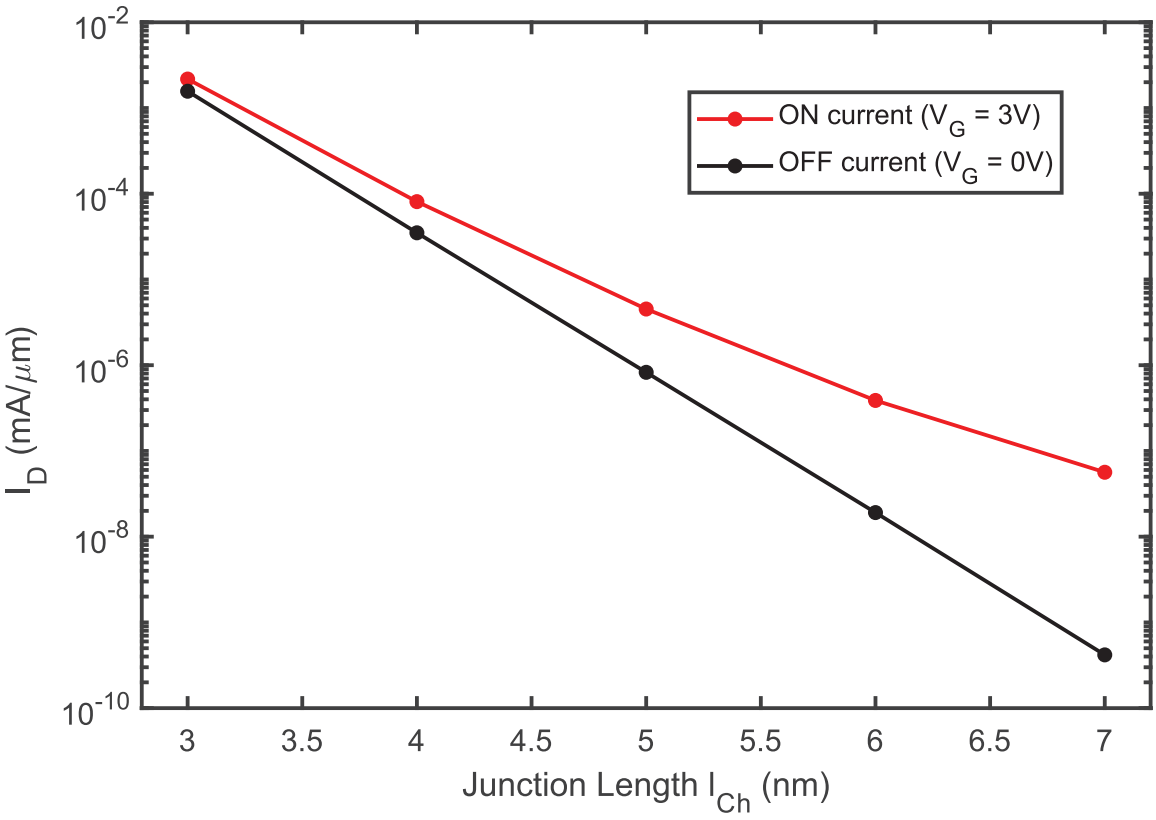

Figure 3.10: ON and OFF currents vs. junction length at $V_D = 3V$.

Altering the channel length l_{Ch} of the BJMITT predictably causes the greatest impact on the overall drain current due to the exponential relationship between tunneling length and tunneling current. Referring to Fig. 3.10, the ON and OFF currents at $V_D = 3V$ are shown. Notably, the increased degree of gate field penetration manifests as a deflection in the ON current away from a constant slope in the

logarithmic scale. The increase in field penetration comes at a cost of overall current value I_D which, in the ON state, is about 10^4 times larger at 3nm versus 7nm. The change in ON/OFF ratio, shown in Fig. 3.10, further demonstrates the increased field penetration.

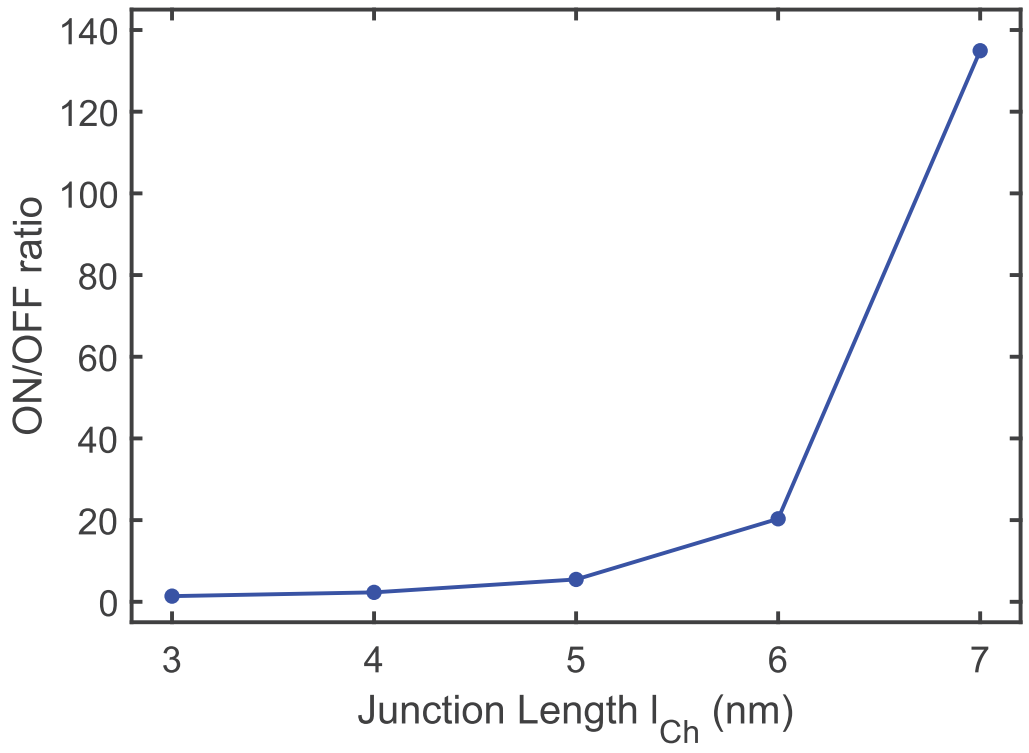

Figure 3.11: ON/OFF ratio vs. junction length at $V_D = 3V$.

The upper and lower limits of 3nm and 7mn junction length are chosen because any junction outside of these limits is deemed to be impossible to work, or unrealistic to operate. For the lower limit, any junction length that is lower than 3nm would have an electric field strength of at least 1V/nm, which is approaching the breakdown field for some materials[43]. Additionally, as will be shown, transistor performance is very poor at $l_{Ch} \leq 3nm$ due to low field penetration and pinning of the potential to the source and drain voltages. For the upper limit, tunneling current across an $l_{Ch} \geq 7nm$ is low enough to almost be negligible and would not produce enough current for a useful transistor. For example, taking the ON current at 7nm from Fig

3.10 and assuming the device has a thickness of 100nm, the total current would be 5.6×10^{-9}mA.

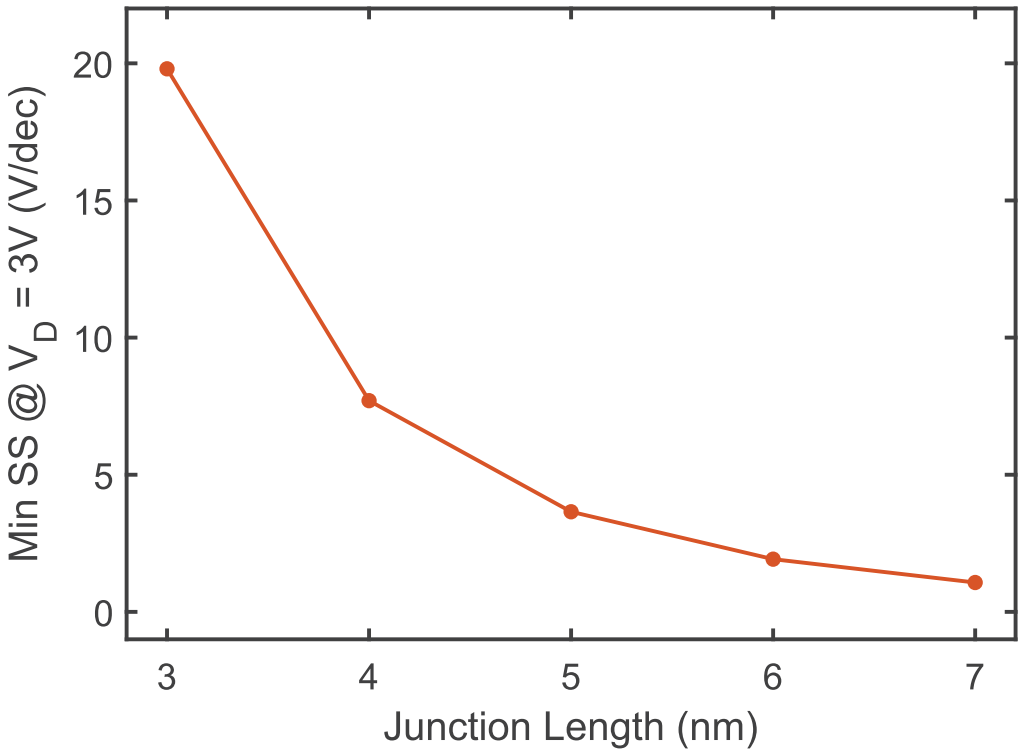

Figure 3.12: Sub-threshold swing vs. junction length at $V_D = 3V$.

Fig. 3.11 shows the exponential relationship between the ON/OFF ratio and l_{Ch} and Fig. 3.12 shows the inverse exponential relationship between SS and l_{Ch}. Of interest when comparing Fig. 3.11 and Fig. 3.12 is the difference in behaviour of the 5nm junction when compared to the edge cases of 3nm and 7nm. The 3nm junction and the 7nm junction both exhibit poor and excellent performance characteristics, respectively, however the $l_{Ch} = 5$nm device has an ON/OFF ratio close to that of the 3nm junction, and a SS closer to that of the 7nm junction.

Notably, this is not a surprising or unpredictable result, since the tunneling current has an exponential relationship with the junction length. Since the ON/OFF ratio is more important for a transistor operating as a switch, and SS is more important for a transistor operating as an amplifier, cases where one can be improved, even if the

other is not, are of interest.

In the following sections, the device geometry is altered around the junction length l_{Ch}, and the effect on the key characteristics is presented.

3.5.2 Gate Distance

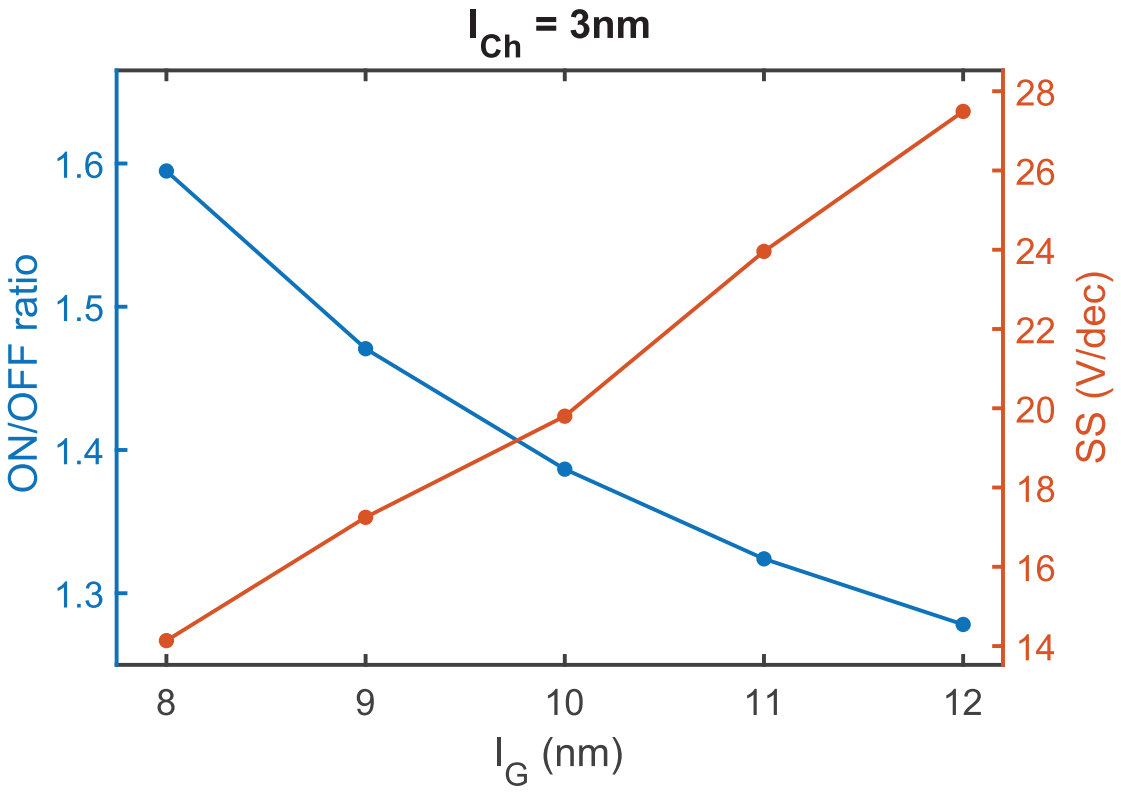

Figure 3.13: Effect of varied l_G on electronic characteristics of a 3nm junction length device.

Altering the distance of the gate contacts from the junction affects gate field penetration. In this section, the resulting ON/OFF ratio and SS as the gate distance is varied between 8nm and 12nm. Results are presented for devices with junction lengths of 3nm, 5nm, and 7nm. It should be noted that as the gate distance is decreased, the gate and source/drain contacts become proximate, thus increasing the source/drain-to-gate leakage current.

In this section, the change in ON/OFF ratio and SS are shown for each devices with junction lengths of 3nm, 5nm, and 7nm, respectively. In each configuration,

decreasing gate distance results in a non-linear improvement ON/OFF ratio, and a linear improvement in SS.

Referring first to the 3nm device, the ON/OFF ratio and the SS are shown in Fig. 3.13. The results are reflective of both the relative poor performance of the device due to the poor field penetration. The change in SS from 28V/dec to 14V/dec, while large in magnitude, is not a substantial increase in device efficacy. This lack of increased efficacy is further reinforced by the low increase in ON/OFF ratio.

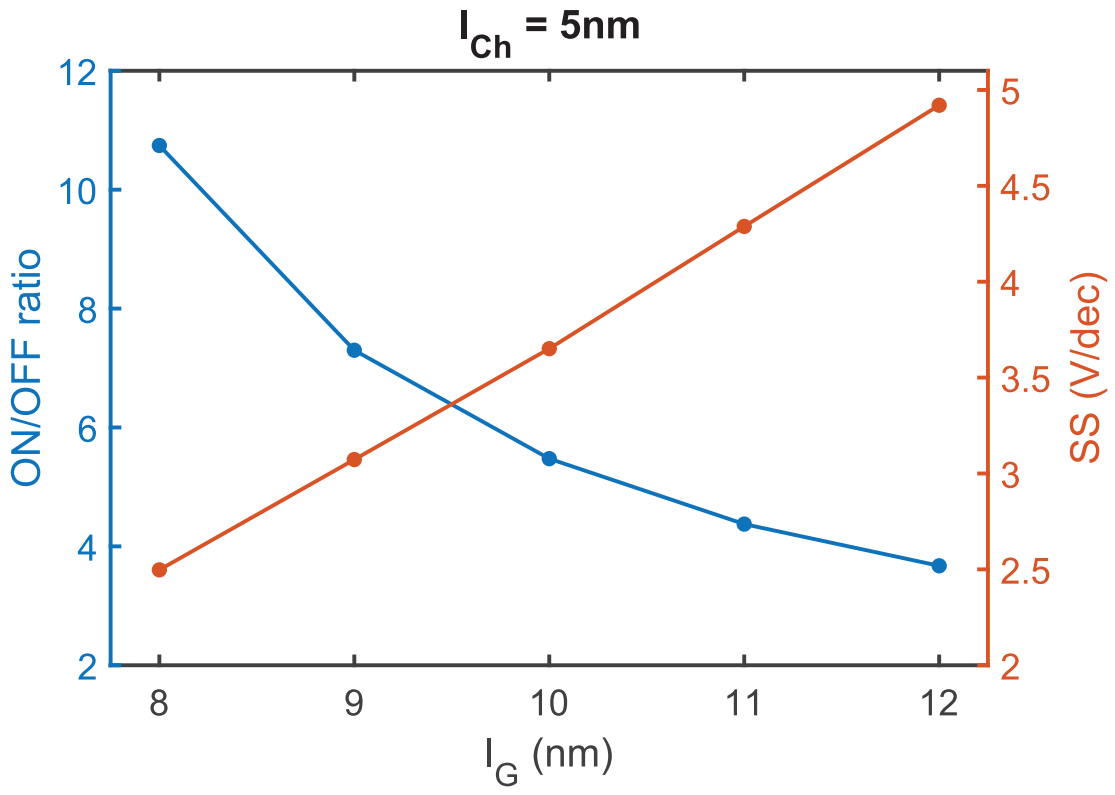

Figure 3.14: Effect of varied l_G on electronic characteristics of a 5nm junction length device.

As the channel length is increased to 5nm, shown in Fog. 3.14 and 7nm, shown in Fig. 3.15, the ability for the gate field to penetrate the channel shows up most clearly in the behaviour of the ON/OFF ratio at each junction length. As l_{Ch} is increased, the ON/OFF ratio vs. gate distance relationship becomes more non-linear. This demonstrates the importance of having high gate field penetration to allow for the gate field to have a highly non-linear effect on current, such as for the l_{Ch} = 7nm

device shown in Fig. 3.15.

For each of the different channel length devices, SS performance saw an approximately 50% decrease in maximum SS between 12nm and 8nm gate distance. The magnitude of the change in SS is greatest for the 3nm junction and lowest for the 7nm junction, however this is expected due to logarithmic calculation of SS. When the magnitude is lower, larger deflection of the field is required to improve the SS, as shown for the l_{Ch} = 7nm in Fig. 3.15 .

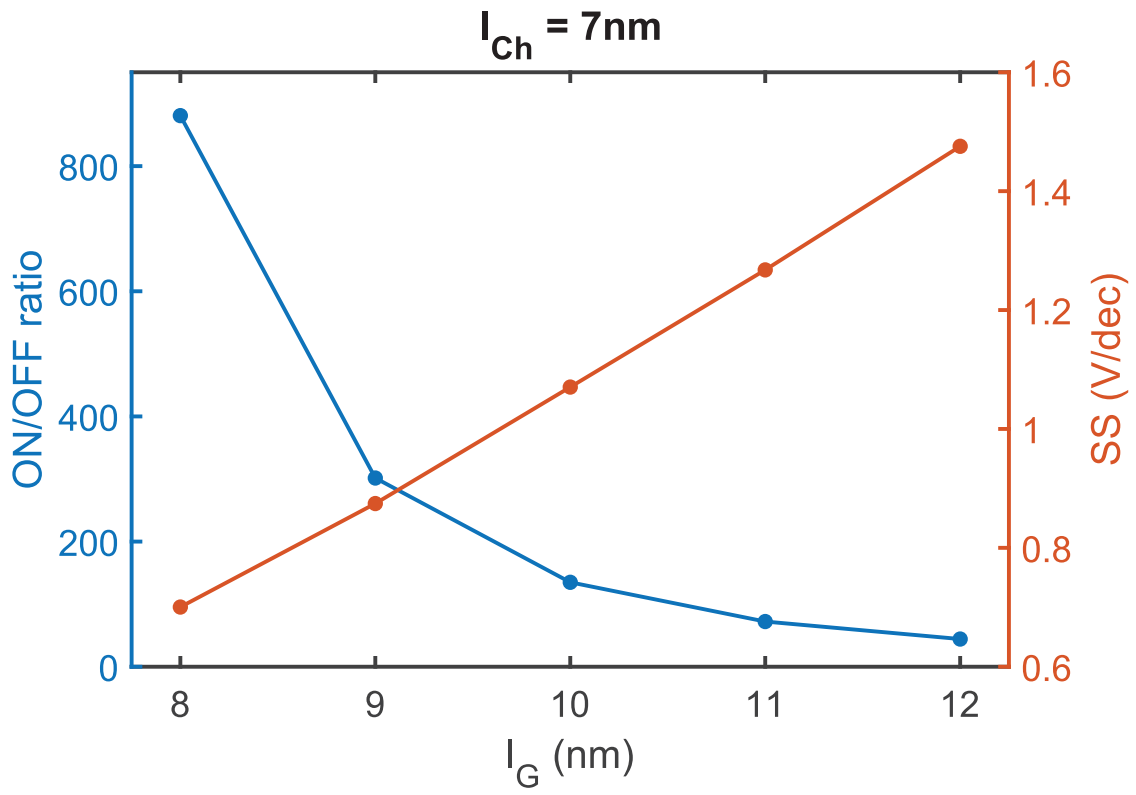

Figure 3.15: Effect of varied l_G on electronic characteristics of a 7nm junction length device.

Next to altering the junction length, changing the distance of the gate contacts from the channel has the largest effect on the key device characteristics due to the increased strength of the gate field at shorter distances of l_G. The improvement of characteristics is pronounced for devices with a greater l_{Ch} due to the combination of increased gate field strength and gate field penetration.

3.5.3 Tip Radius of the Source and Drain

Next, the effect of altering the sharpness of the source and drain contact geometry is investigated. The change in sharpness is simulated by varying the radii r_S and r_D between 1nm and 3nm.

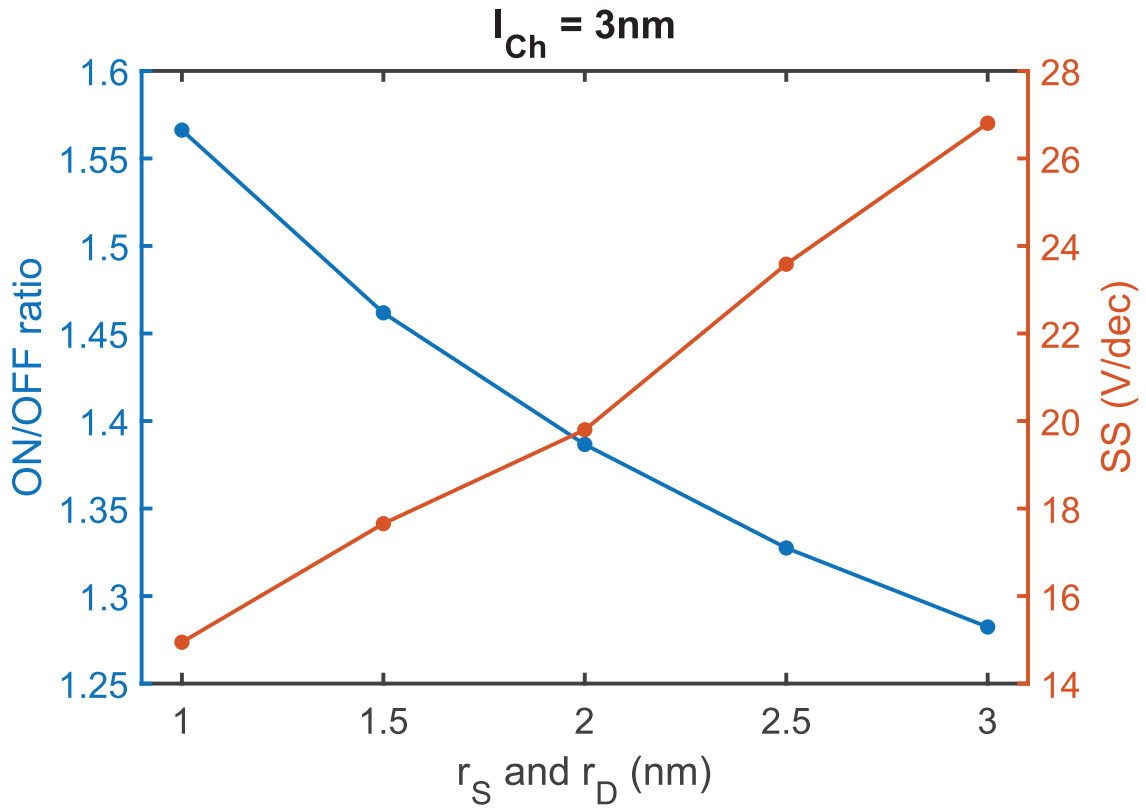

Figure 3.16: Effect of varied r_S and r_D on electronic characteristics of a 3nm junction length device.

The tip radius is important when considering the physical implementation of the device. The smaller a physical feature is, the more difficult it is to fabricate such a feature. From this perspective, it is preferred to have a device with as few small features as possible.

Decreasing or increasing the source and drain radii shows an increase and a decrease in the key performance characteristics, respectively. Only slight non-linearity is seen in the change in ON/OFF ratio at each of the junction lengths.

For the 3nm junction, shown in Fig. 3.16, similar to the effect of the gate distance,

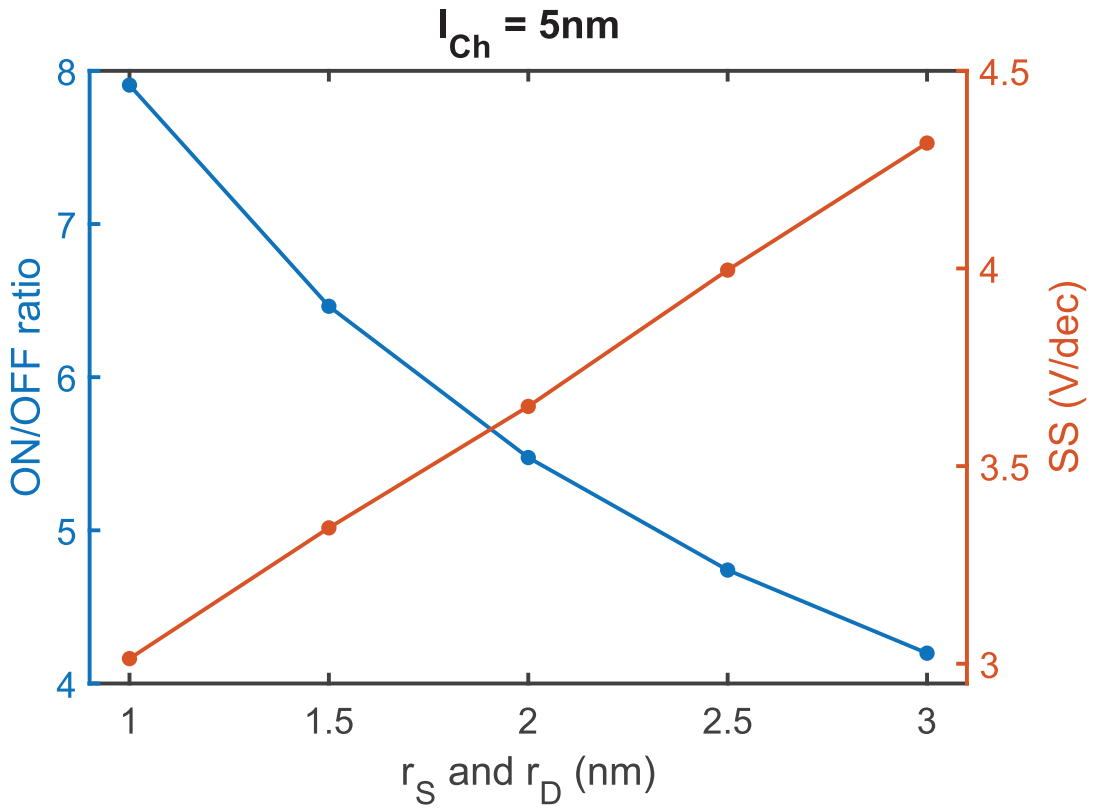

Figure 3.17: Effect of varied r_S and r_D on electronic characteristics of a 5nm junction length device.

a large decrease in the magnitude of SS, and a small increase in ON/OFF ration is seen as the radii decrease, but the key characteristics still remain outside of the viable range. With that said, if there were a fabrication process that could reliably form 3nm junction, the capability would likely be there for forming a feature with a radius of 1nm, and it would be advisable to pursue all improvements in device performance.

Looking at the results for the 5nm junction shown in Fig. 3.17, varying the radii has the expected change in key characteristics based on the effect of gate field penetration. However for the 5nm junction in particular, varying the radii above 2nm does not to have a serious effect on device performance.

For the 7nm junction, shown in Fig. 3.18, the impact of radius variation is relatively low. This conclusion cannot be derived from looking at the magnitude of the change in the values of the key characteristics alone. Instead, insight can be

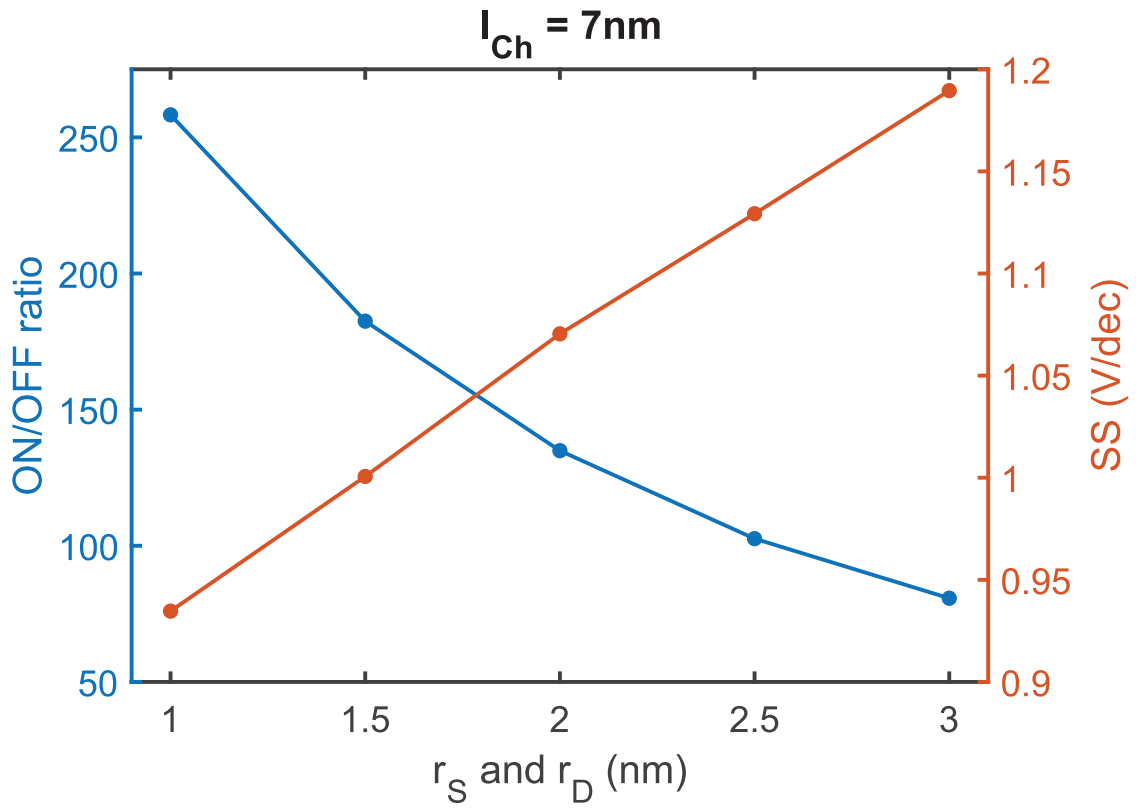

Figure 3.18: Effect of varied r_S and r_D on electronic characteristics of a 7nm junction length device.

gained through looking at the differences in the curves between the 5nm and the 7nm junction. As the tip radius is changed for 5nm and 7nm junctions, the behaviour in ON/OFF ration exhibits similar non-linear behaviour. The similar non-linear behaviour can be contrasted with the difference in non-linearity for the ON/OFF curves for 5nm and 7nm as gate distance is changed (Figs 3.13 and 3.14).

In addition to the change in key characteristics, the change in overall current, for both the ON and OFF states of the device, changes approximately proportionally to the change in source and drain radii. The overall increase in current is due to the widening of the active region of the device, and can be visualized as a widening of the current density distribution curves shown in Fig. 3.4. The smaller radius source and drain would also have a slight difference 1D potential shape between the source and drain due to geometry-induced field enhancement, however the difference is nominal

and is not reflected in the changes to the key characteristics, which is dominated by the changes in gate field penetration. In the ON state, for a device with l_{Ch} = 5nm, I_D increased from 3.5×10^{-6}mA/μm for $r_S = r_D$ = 1nm, to 5.5×10^{-6}mA/μm for $r_S = r_D$ = 3nm.

3.5.4 Discussion of the Results

Table 3.1 consolidates the data shown in the previous sections. In general, the results reinforce the idea that improved gate field penetration leads to improved performance. The trends of both the $l_{Ch} = 3nm$ and $l_{Ch} = 7nm$ show this explicitly. Performance improvements of the 3nm junction devices are all marginal when compared to the performance improvements of the 7nm junction. However, it cannot be ignored that the improved performance of the 7nm junction always comes at the cost of overall current.

A *Au*-ZrO_2-*Au* device having a channel length of 5nm strikes a balance of total current, performance characteristics, and feasibility of implementation. The results presented in this section provide a blueprint for utilizing the geometry of the BJMITT to improve performance. The conclusion is simply to increase gate field penetration wherever possible.

The most effective avenue for improved performance is to increase the channel length; however, this improvement comes with the cost of significantly reducing the overall current. The limit of overall current is one partially imposed by the potential barrier height - or the materials chosen for the device.

l_{Ch} (nm)	l_G (nm)	$r_D = r_S$ (nm)	I_D ON ($\times 10^{-6} mA/\mu m$)	I_D OFF ($\times 10^{-6} mA/\mu m$)	ON/OFF ratio	SS (V/dec)
3	10	1	1.56×10^{3}	1.00×10^{3}	1.56	14.94
	8	2	2.34×10^{3}	1.47×10^{3}	1.59	14.13
	10	2	2.18×10^{3}	1.57×10^{3}	1.39	19.80
	12	2	2.09×10^{3}	1.63×10^{3}	1.28	27.49
	10	3	2.60×10^{3}	2.02×10^{3}	1.28	26.80
5	10	1	3.52	0.44	7.91	3.01
	8	2	6.58	0.61	10.75	2.50
	10	2	4.52	0.83	5.47	3.65
	12	2	3.64	0.99	3.67	4.92
	10	3	5.03	1.20	4.20	4.31
7	10	1	47.93×10^{-3}	0.19×10^{-3}	258.26	0.93
	8	2	185.12×10^{-3}	0.21×10^{-3}	880.68	0.70
	10	2	56.40×10^{-3}	0.42×10^{-3}	134.92	1.07
	12	2	28.88×10^{-3}	0.65×10^{-3}	44.25	1.48
	10	3	57.09×10^{-3}	0.71×10^{-3}	80.73	1.19

Table 3.1: Summary of performance characteristics for *Au-ZrO_2-Au* BJMITT device at $V_D = 3$V.

3.6 Changes in Device Material

The material of the BJMITT for all of the results presented up to this point has been exclusively gold (Au) and zirconia (ZrO_2). In this section, variations of the materials used in the device are investigated. In order to present the results with as little variables as possible, the results presented in this section use the geometry of the device in sections 3.1 to 3.5.1. For each of the devices in this section, $r_S = r_D =$ 2nm and $l_G = 10$nm.

The results of devices with changes in material should be taken with the caveat that no fabrication process has been explored or tested for any materials other than Au and ZrO_2. In particular, the other metal used in the simulation, aluminum, forms native oxides in the presence of oxygen, making the fabrication of *Al-oxide-Al* tunneling devices significantly more complicated than for gold. As such, it will be understood that no fabrication process has been developed for materials other than the *Au-ZrO_2-Au*. For the *Au-ZrO_2-Au* device, a proposed fabrication process is detailed in section 3.6, along with an investigation into that fabrication process.

The most consequential difference when changing the material is the difference in barrier height $\phi = W - \chi$. The following different material combinations are investigated, with the barrier height ϕ shown below in table 3.2:

Metal	W	Insulator	χ	ϕ
Au	5.1 eV	SiO_2	0.9 eV	4.2 eV
Au	5.1 eV	ZrO_2	2.75 eV	2.35 eV
Au	4.15 eV	ZrO_2	2.75 eV	1.4 eV
Au	4.15 eV	Cr_2O_3	3.3 eV	0.85eV

Table 3.2: Material combinations used with parameters.

Of note among these examples is the Au-SiO_2-Au device which, due to the large band gap of SiO_2, has a barrier height that is greater than 3V. In addition to drastically decreasing the amount of overall current, the device does not enter the field emission regime within the bounds of the simulation. As such, the deflection of the potential barrier does not alter the effective tunneling distance of the electrons.

The remaining choices of material are done so to have such that they are approximately three quarters, half, and one quarter of $V_D = 3$V.

A variable not listed in Table 3.2 is the effective mass of the electron in the various materials. For the various metals, a unity effective mass was used. For SiO_2, effective mass values of $0.5m_e$[44] and $0.36m_e$[45, 46] have been reported, and $0.4m_e$ is used. For ZrO_2, effective mass values of $0.1m_e$[42] is used. For Cr_2O_3, reports of an effective mass value were not found. As Cr_2O_3 was chosen somewhat arbitrarily to provide an example of a theoretical device with a very low potential barrier, $0.4m_e$ is used for it as well.

3.6.1 Key Performance Characteristics

The ON and OFF currents for each of the structures listed in the table 3.2 are shown in Fig. 3.19. The Al-Cr_2O_3-Al, Al-ZrO_2-Al, and Au-ZrO_2-Au have a larger magnitude of current due to having both a potential barrier height of less than 3eV and being

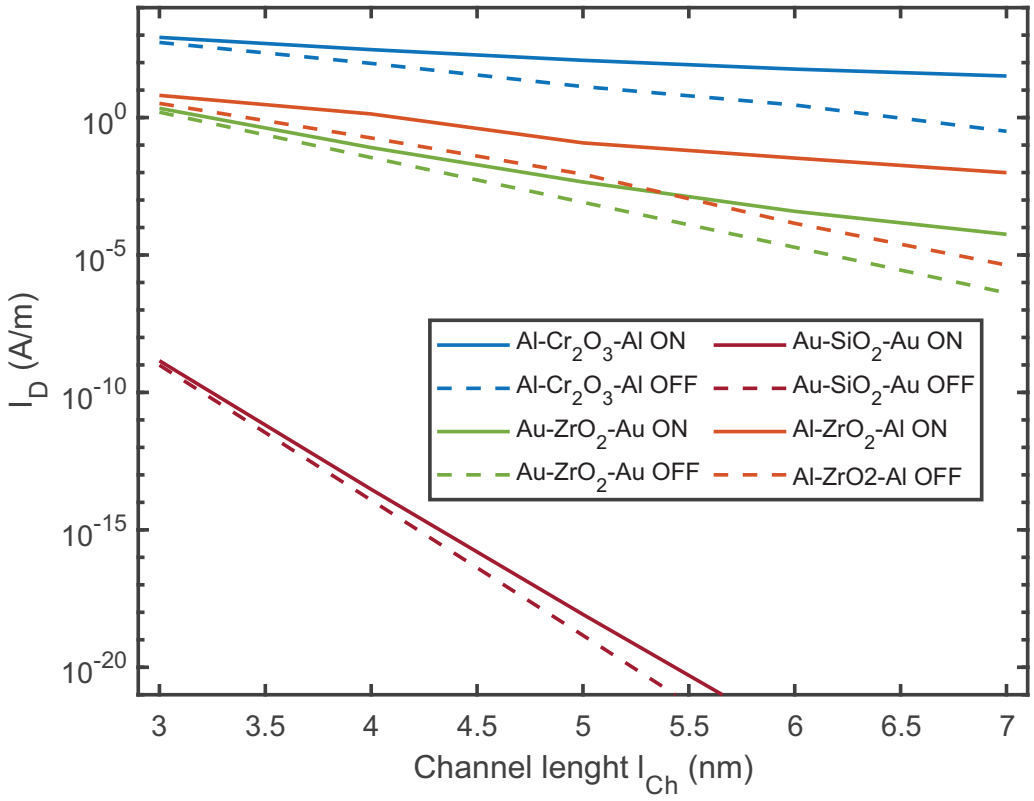

Figure 3.19: ON and OFF current at $V_D = 3V$ for devices made with the indicated materials.

in the field emission regime at $V_D = 3$V. The currents for the *Au-SiO_2-Au* device is cut off in order to show greater detail of the other results. The different slope of the *Au-SiO_2-Au* current-channel length curve is attributed to the fact that at $V_D = 3$V, the tunneling distance for the *Au-SiO_2-Au* barrier is equal to the channel length, whereas the *Al-Cr_2O_3-Al*, *Al-ZrO_2-Al*, and *Au-ZrO_2-Au* devices have a tunneling distance that is less than l_{Ch} at each data point. Fig. 3.19 provides a good indication as to the magnitude of current that is expected for a device with a given barrier height.

Fig. 3.20 shows the ON/OFF ratio vs. channel length for each of the devices. The results are shown on a logarithmic scale due to the ON/OFF ratio of the *Al-ZrO_2-Al* device having an ON/OFF ratio that is about 17 times larger than the other devices.

Fig. 3.21 shows the SS vs. channel length at $V_D = 3V$ for each of the devices.

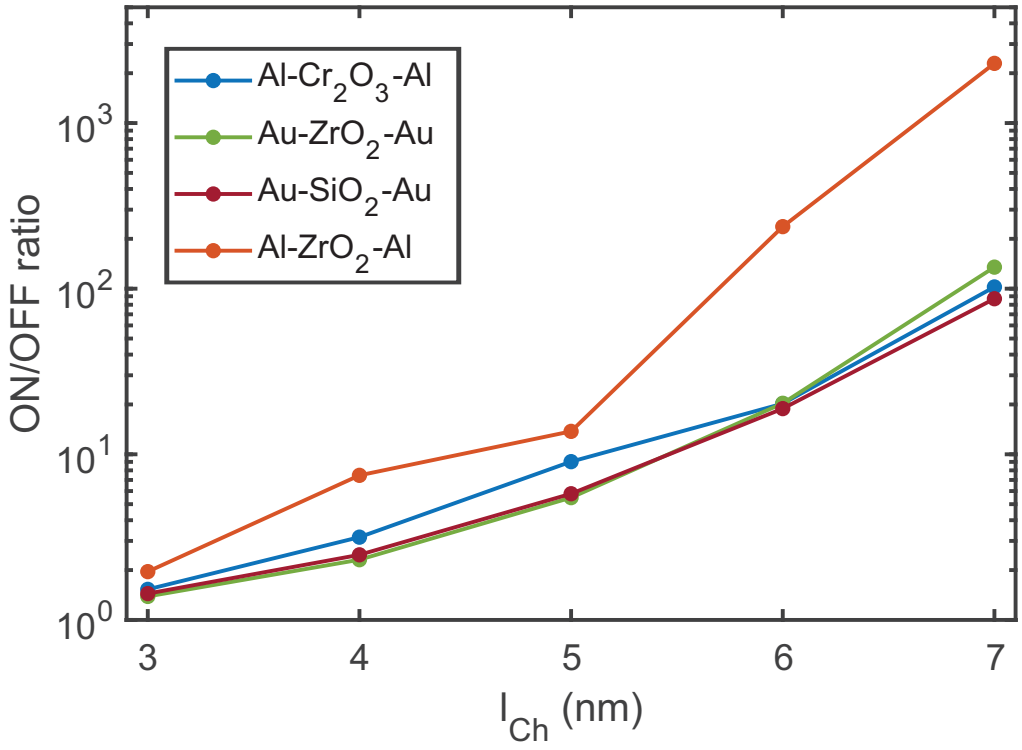

Figure 3.20: ON/OFF ratio at $V_D = 3V$ for devices made with the indicated materials.

Similar to the ON/OFF ratio, the *Al-ZrO_2-Al* device exhibits better performance when compared to the other devices, which have similar SS.

Insight into the results shown in the above comparisons can be gained by analysing how the ON/OFF ratio of the various devices changes as the source drain voltage V_D is changed. Fig. 3.22 illustrates this behaviour for each of the device material combinations with a $\chi < 3eV$. The *Al-ZrO_2-Al* and the *Al-Cr_2O_3-Al* have two distinct peaks.

The first peak is located where V_D has a slightly higher value than χ. This is the voltage at which the gate field alters the barrier between direct tunneling and field emission, leading to a large peak in ON/OFF ratio.

The second peak is located where V_D has a slightly lower voltage than 2χ. This is where the gate field has the strongest influence on effective barrier length. The increased performance of the *Al-ZrO_2-Al* relative to the other devices shown in Figures

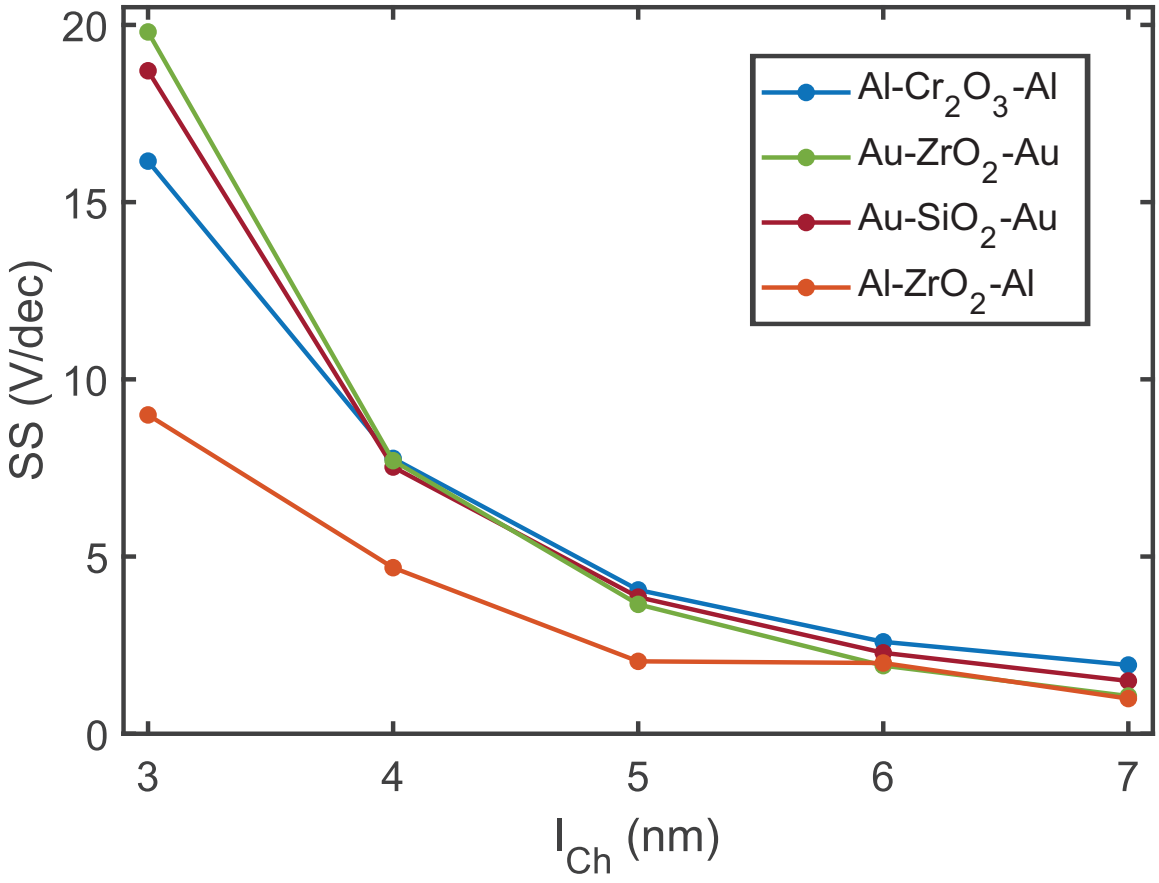

Figure 3.21: Subthreshold swing at $V_D = 3V$ for devices made with the indicated materials.

3.20 and 3.21 is attributed to the fact that $V_D = 3$V is located on the second peak of the ON/OFF vs. V_D curve for *Al-ZrO_2-Al*.

Materials	*Au-SiO_2-Au*	*Au-ZrO_2-Au*	*Al-ZrO_2-Al*	*Al-Cr_2O_3-Al*
ϕ (eV)	4.20	2.35	1.40	0.85
Peak current ratio	5.77	5.47	455	2038
V_D @ peak	3^+V*	3^+V*	1.8V	1V
On @ peak ($mA/\mu m x 10^{-6}$)	8.35x10^{-16}	4.52	85.7x10^{-3}	19.50
Off @ peak ($mA/\mu m x 10^{-6}$)	1.45x10^{-16}	0.83	1.88x10^{-4}	9.56x10^{-3}

Table 3.3: Summary of performance characteristics for the devices with varied barrier heights. *peak current ratio occurs outside of the simulation simulated voltages

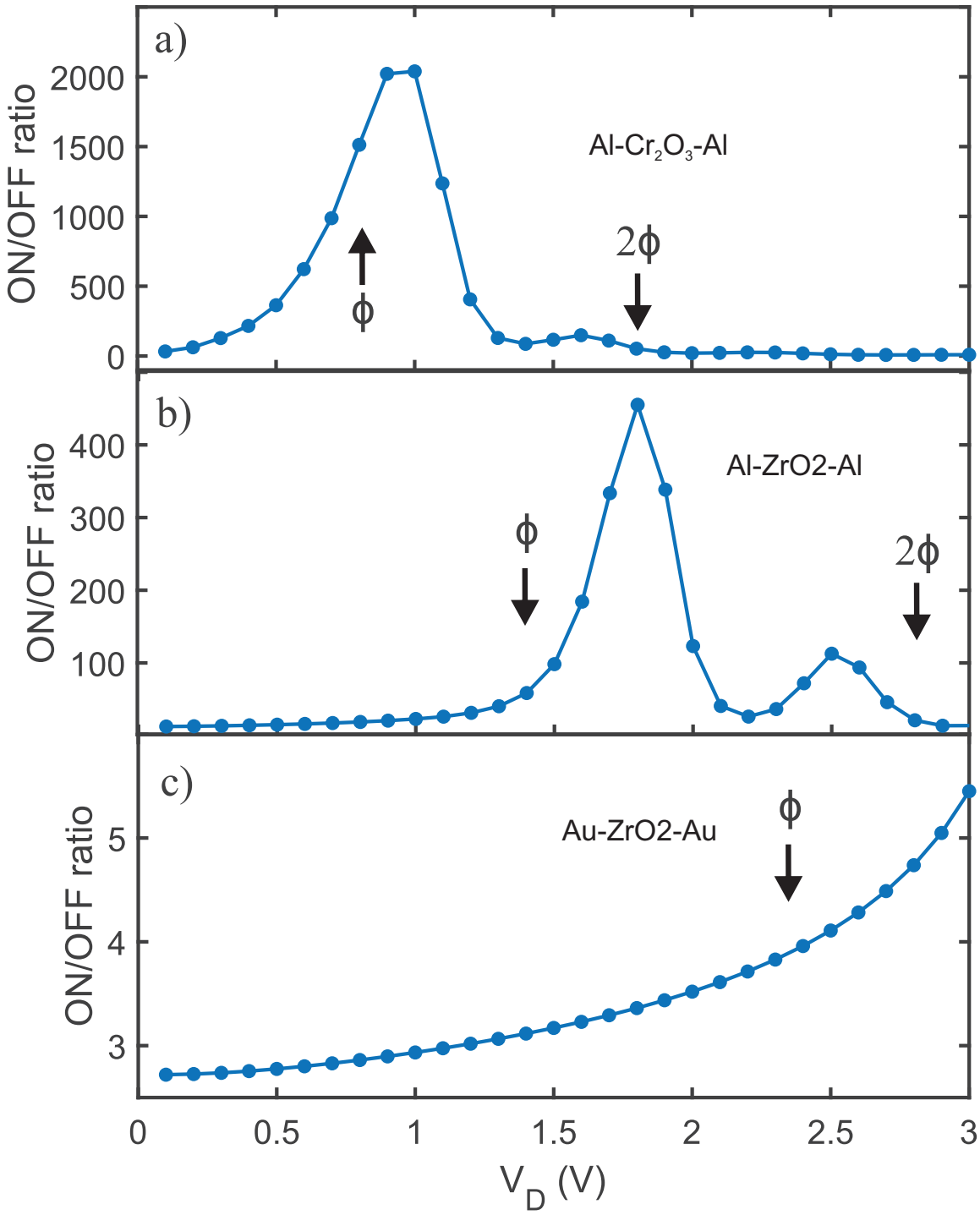

Figure 3.22: ON/OFF ratio vs. V_D for a) *Al-Cr_2O_3-Al*, b) *Al-ZrO_2-Al*, and c) *Au-ZrO_2-Au*.

3.6.2 Discussion of Results

The key results for the various material combinations is summarized in table 3.3.

We can compare the change in effective tunneling length for the *Au-ZrO_2-Au* and the *Al-ZrO_2-Al* devices at l_{Ch} = 5nm to see this conclusion. As shown previously, the *Au-ZrO_2-Au* device has a change in effective tunneling length of 0.29nm, or 10% change in the effective tunneling length, leading to an ON/OFF ratio of 5.5. For the *Al-ZrO_2-Al* device, the change in effective tunneling length is 0.49nm, or a 20% change in effective tunneling length leading to an ON/OFF ratio of 13.8. An improvement in effective tunneling length alteration generally leads to improved performance, and this improvement peaks when the effective tunneling length is around 1/2 of the total length of the junction.

However, the ON/OFF ratio of the *Au-ZrO_2-Au* and the *Au-SiO_2-Au* devices are located at a voltage V_D that is lower than the value of the first peak. This can be seen in the ON/OFF ratio vs. V_D curve of *Au-ZrO_2-Au*, where the ON/OFF ratio is trending upwards at V_D = 3V. The results indicate that the change in tunneling current for the *Au-ZrO_2-Au* device at V_D = 3V is primarily a result of the transition between direct tunneling and field emission, rather than a result only of the change in effective tunneling length.

The magnitude of the first peak relative to the second peak in Fig. 3.22a is significantly larger that the relative magnitude of the peaks in Fig. 3.22b. This is likely due to the lower χ of the *Al-Cr_2O_3-Al* barrier, which in turn leads to a shallower slope in the potential at the transition voltage between direct tunneling and field emission. For a lower barrier height and shallower slope in the potential, the gate field is able to modulate the potential barrier in a more impactful way.

The above results are well explained by referring back to eq. 1.3.1.7, rewritten here as eq. 3.1, where the wavefunction (and therefore probability density) of a plane wave particle within an inadmissible potential barrier has the form:

$$\psi_{II}(x) = C_3 e^{-\kappa z} \tag{3.1}$$

where

$$\kappa = \frac{\sqrt{2m^*(U(z) - E)}}{\hbar} \tag{3.2}$$

and V is the height of the barrier at point z and E is the energy of the plane wave particle. Eq. 1.3.1.7 tells us that the tunneling probability of the electron attenuates within a potential barrier approximately according to the following proportions:

$$D(E) \propto e^{-\sqrt{\phi}}, D(E) \propto e^{-d} \tag{3.3}$$

where d is the effective tunneling distance and ϕ is the barrier height. While these proportions show that reducing effective tunneling length has more impact on changing the tunneling rate than the barrier height, our results show that modulating the barrier height across a junction is nonetheless effective at modulating tunneling current.

The first and second peaks seen in Fig. 2.22a and 2.22b correspond to maximizing the change in the proportions of eq. 3.1, respectively.

Assuming the gate field, with the gate contacts held at a constant voltage, has an equal effect on the barrier at all values of V_D, the total change to the height of the barrier as a percentage of the overall height of the barrier between the on and off state is greatest at a maximum around the value of $V_D = \chi$. At a lower V_D the average barrier height is greater and the change is a lower proportion of the total average height. At higher V_D a portion of the barrier height is below the electron energy, and changes to that portion of the barrier height does not affect tunneling probability. This is an over-simplification, but accounts for the proximity of the first peak V_D to χ and the relative reduction in peak height between Al-Cr_2O_3-Al and

Al-ZrO_2-Al.

The second peak corresponds to a maximum in the change in the effective tunneling length of the barrier.

This explanation of the results show that, when possible, modulating the barrier between direct tunneling and field emission provides the highest improvement to key device characteristics, however the results show that modulating effective tunneling length is reliable for improving device operation for a higher potential barrier. Any and all potential modulation affects tunneling current, and the most impact on device performance is ensuring high gate field penetration.

3.7 Device Fabrication

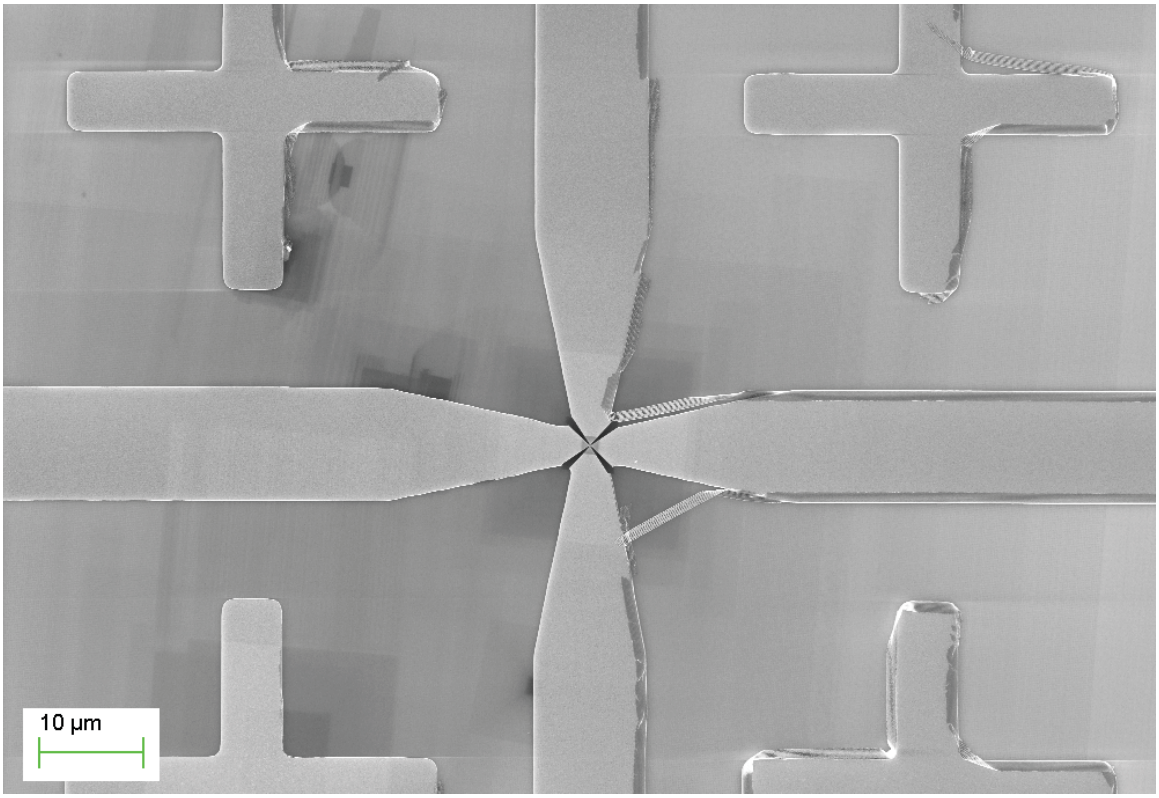

Figure 3.23: SEM image of the cross structure after lithography. The Ga FIB milling can be seen at the center of the structure.

A fabrication method for the BJMITT was developed and partially explored. In

an effort to develop a proof of concept device, Gallium and Helium focused ion beam (FIB) milling were used to etch the device structure. What follows is our best and efforts in realizing the presented device.

3.7.1 Preparation for Helium Focused Ion Beam Milling

To start, 100nm of gold was deposited on an SiO_2 wafer via electron beam deposition. Conventional photolithography, using a lift off process, was used to create a cross structure as shown in the image of Fig. 3.23, which was taken using a scanning electron microscope. The 10 micron wide arms extend from contact pads to meet at a 5 micron wide central point. The four contacts correspond to each of the source, drain, and two gates.

Focused-ion-beam milling was performed using a Zeiss Orion NanoFab helium ion microscope, which is equipped with a gallium ion focused ion beam (FIB). The gallium ion FIB was first used to mill out large sections of the center of the cross, down to an area of approximately 100nm by 100nm. This can be seen in both Fig. 3.23 and Fig. 3.24. A dose of $0.147nC/\mu m^2$ was used for gallium ion milling. A helium ion FIB was then used to mill the structure of the device.

3.7.2 Helium Ion Beam Milling

As a first attempt, a simple x-shaped pattern was milled to isolate each of the contacts; this resulted in a minimum feature size (channel length) of approximately 30nm. This result can be seen in Fig. 3.24. The following parameters were used in the etch: $10\mu m$ aperture, 1.18pA ion current, and 5 repeats of the pattern with a $5000\mu s$ dwell time, for a linear dosage of approx. $114pC/\mu m$.

While helium ion milling has a theoretical minimum resolution of 5nm, in practice, achieving such a resolution is difficult. Several factors are theorized to contribute to such a challenge. In this case, the desired high aspect ratio of the device and the

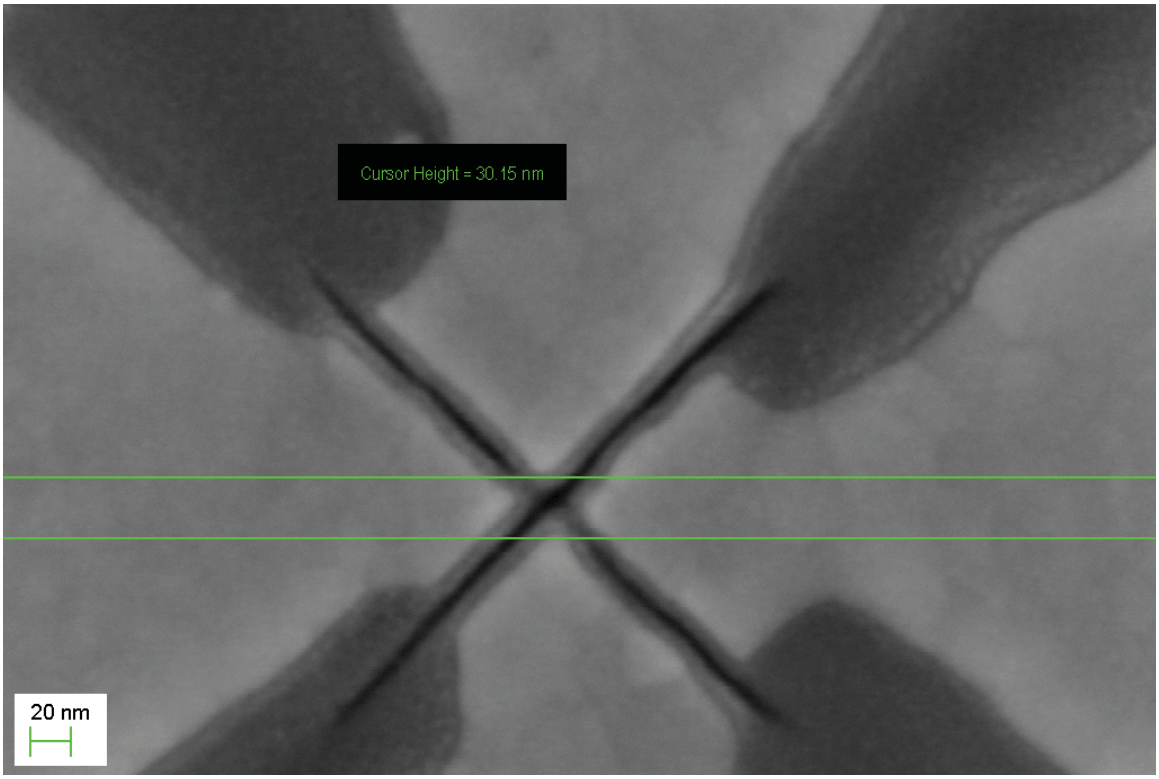

Figure 3.24: SEM image of the first attempt at milling the device structure using Helium ion FIB.

polycrystalline nature of the gold being milled lead to unpredictability in the milling rate of the He ion FIB. In order to account for this, an altered milling pattern was used for subsequent attempts. The new pattern removed any direct crossing of the active region of the device and instead, the two sides of the junction - between the gate contacts and the source/drain - were milled independently in a V-shape, so that the channel region between the source and drain was only milled by the outer edge of the beam as it passed by. The pattern used is shown in Figure 3.25, which is an SEM image of the second attempt overall and the first attempt using the new etching pattern.

Additionally the nature of the FIB introduces further challenges. The He FIB can be advantageously used to image the device in situ, however imaging actively etches the area being imaged, which may be detrimental. Furthermore, the electrostatic charging of the substrate that occurs during etching results in charge-induced drift of

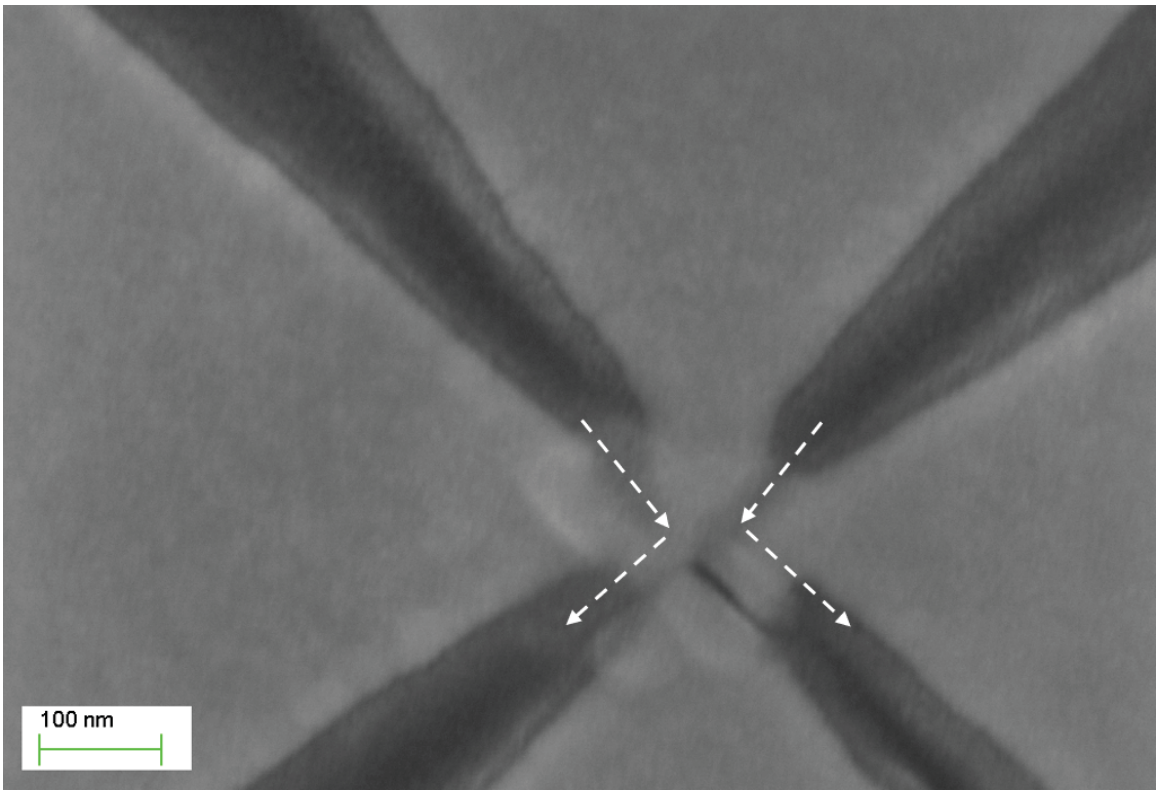

Figure 3.25: SEM image of the second attempt at milling the device structure using Helium ion FIB. The etch pattern for the He ion FIB is shown in dashed lines.

the substrate, increasing the necessity for imaging, while also increasing the number of trials needed to dial in the process.

The second attempt, using the V-shaped etching pattern, shown in Fig. 3.25, used the following etch parameters: $10\mu m$ aperture, $616fA$ ion current, and 10 repeats of the pattern with a $1000\mu s$ dwell time, for a linear dosage of approx. $35pC/\mu m$ In this case, the etch was insufficient, leaving the left side gate, source, and drain contacts visibly in contact.

In the third and final attempt, shown in Fig. 3.26, the V-shaped etching pattern was used with the following etch parameters: $10\mu m$ aperture, 2.08pA ion current, and 7000 repeats of the pattern with a $1\mu s$ dwell time, for a linear dosage of approx. $57pC/\mu m$

SEM imaging of the shown devices was done using a Zeiss Sigma FESEM. After imaging, 15nm of ZrO_2 was deposited on the device from the third attempt using

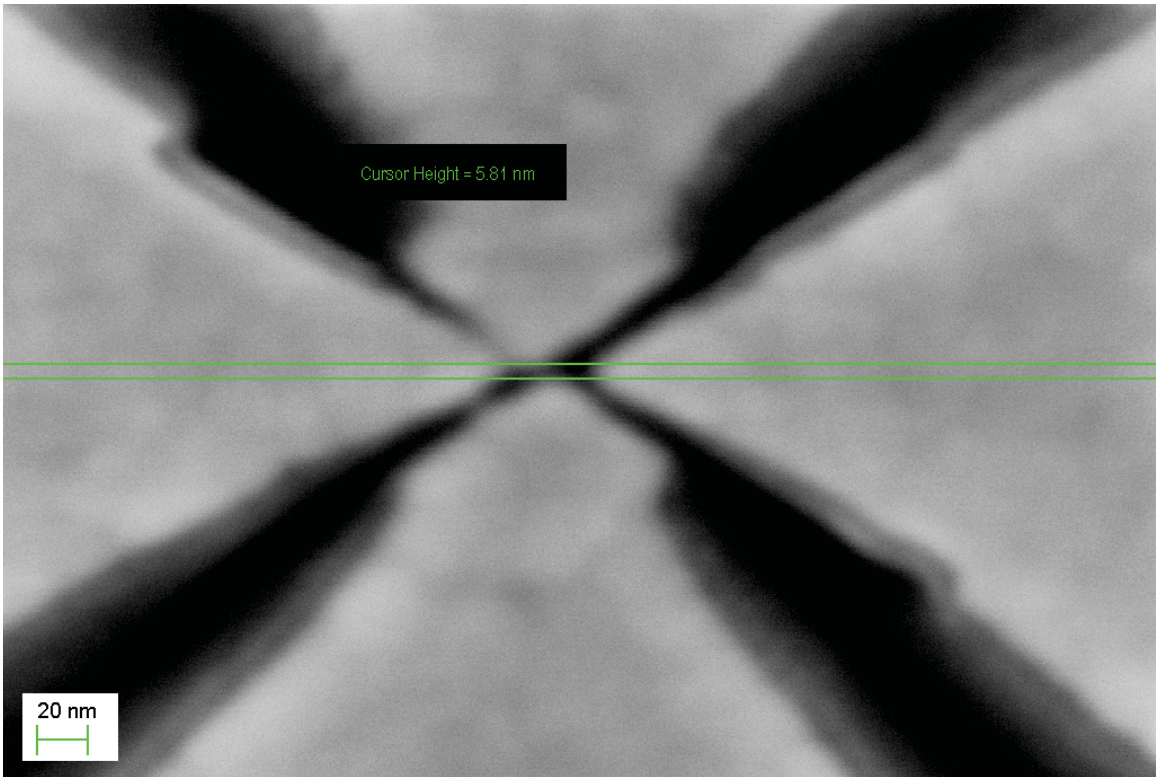

Figure 3.26: SEM image of the third attempt at milling the device structure using Helium ion FIB.

atomic layer deposition. ALD was performed using a Kurt J. Lesker ALD-150L in plasma enhanced mode at a substrate temperature of 150 Celsius, with tetrakis (dimethylamido) zirconium(IV) as the metal precursor and oxygen plasma. 190 cycles were performed for 15nm of oxide.

While the third attempt appeared visibly to be successful, when tested, no tunneling current was observed and the device had only ohmic behaviour. No further attempts were made.

Due to the size of the features, diagnosing the issues with the device is difficult. From Fig. 3.26, it is likely that the top and left contacts are shorted, and the same may be said of the bottom and left contacts, based on the slight protrusion seen on both.

3.8 Summary

In this chapter, a new class of MITT devices, the butterfly junction MITT, is presented and studied using the simulation model introduced in chapter 2. The basic operation is described and an overview of the key performance characteristics for a feasible device is presented. It is shown how the design accounts for the challenges faced at a 5nm scale, and is a realistic implementation of a 5nm-scale MITT device that can be fabricated conventional techniques. The effects of altering the device's various geometric measurements away from those of the feasible device is investigated.

Devices constructed from different materials are also investigated. While they are less feasible to fabricate using conventional processes, insight is provided into how differences band gap of MITTs affects key characteristics.

Finally, a fabrication process for the feasible device is presented and partially investigated.

Chapter 4

T-Shaped Metal-Insulator Tunneling Transistor

4.1 Introduction

In this chapter, the geometry-dependent performance of the BJMITT is further evaluated by comparing the BJMITT with a T-shaped (CMOS-style) device of similar dimensions. The geometry of the T-shaped MITT device configuration is illustrated in FIG. 4.1. The T-shaped MITT has been previously proposed and studied[27], however this study does not consider a feasible geometry. For the T-shaped MITT, similar to the BJMITT, the geometry of our proposed structure is chosen to represent a feasible device with a 5nm channel length. The features we include, most notably the rounded corners of the source and drain contacts, represent a practical implementation of a T-shaped device based on conventional fabrication techniques. These realistic features prevent gate field penetration and reduce the performance characteristics when compared to a device with unrealistic features.

The BJMITT of chapter 3 is a demonstration of how the drawbacks of realistic features can be addressed by altering device geometry alone. The performance of the

T-shaped MITT is presented here and compared with that of the BJMITT.

The T-shaped MITT has two main issues for which the BJMITT was designed explicitly to overcome by changing geometry alone. Most importantly, the source and drain contacts have an extended length of proximity at a distance of $l_C h$, within which the gate field cannot penetrate. This issue is considered, but not factored into the comparison. For the T-shaped MITT, the current is only calculated for a depth of 4nm into the channel. If the channel depth used in the calculation was increased, the ON/OFF current ratio is expected to decrease, as the local current density deeper in the channel is modulated less by the gate field. The results for the T-shaped MITT are calculated for a "best case scenario". Any contribution to the current that occurs deeper in the channel will only lower the current ratio and degrade the performance. It is evident that the dual gate structure of the BJMITT, ensuring field penetration into the entirety of the channel, leads to demonstrable improvements to performance characteristics.

Furthermore, the leakage current between the gate and source/drain will be greater for the T-shaped MITT due to the extended length of close proximity between the gate and the source/drain.

One may consider the BJMITT and the T-shaped MITT to be analogous, with geometric changes made to the T-shaped MITT to address the issues of poor field penetration and high gate-to-source/drain leakage current. The addition of the second gate addresses the field penetration issue and the tapered nature of the contacts outside of the active region addresses the leakage current.

The main advantage of a T-shaped MITT is that it's geometry is more feasibly manufactured using conventional fabrication techniques. As such, a proposed fabrication process for the T-shaped MITT is presented in section 4.4.

4.2 Device Performance

In order to provide a meaningful comparison, the geometry of the T-shaped MITT is specifically chosen to be as similar as possible to the BJMITT in section 3.2. l_{Ch}, l_G and r_S are chosen to be the same, and the materials are Au and ZrO_2.

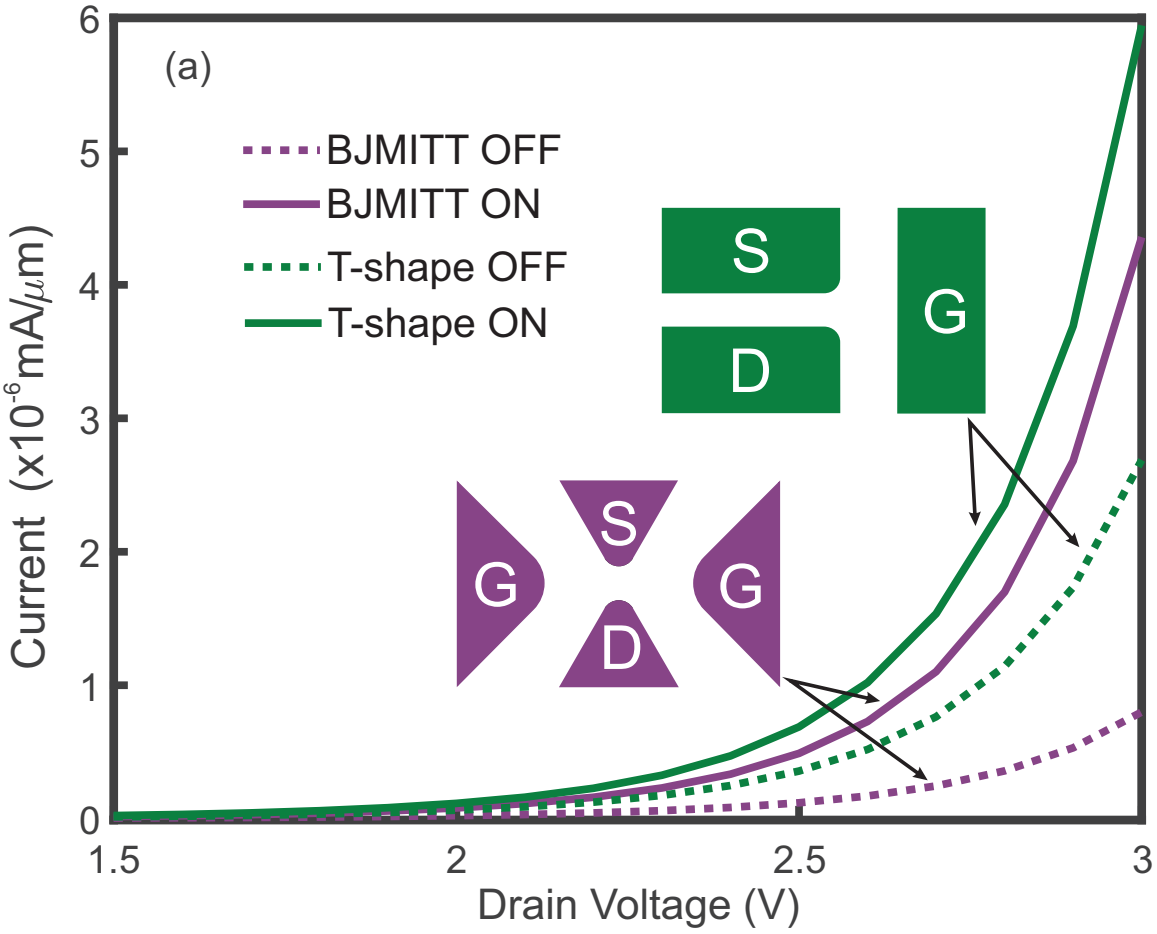

Figure 4.1: Comparison of the ON and OFF currents of the illustrated BJMITT and T-shaped MITT. The T-shape MITT current is offset with respect to the BJMITT current due to the increased deep channel current contribution.

4.3 T-shaped MITT - BJMITT comparison

The improved switching performance of the BJMITT when compared to a T-shaped (CMOS-style) junction metal-insulator-metal tunnel transistor is illustrated in Fig. 4.2. Here, the ON and OFF current along the center of the BJMITT channel are

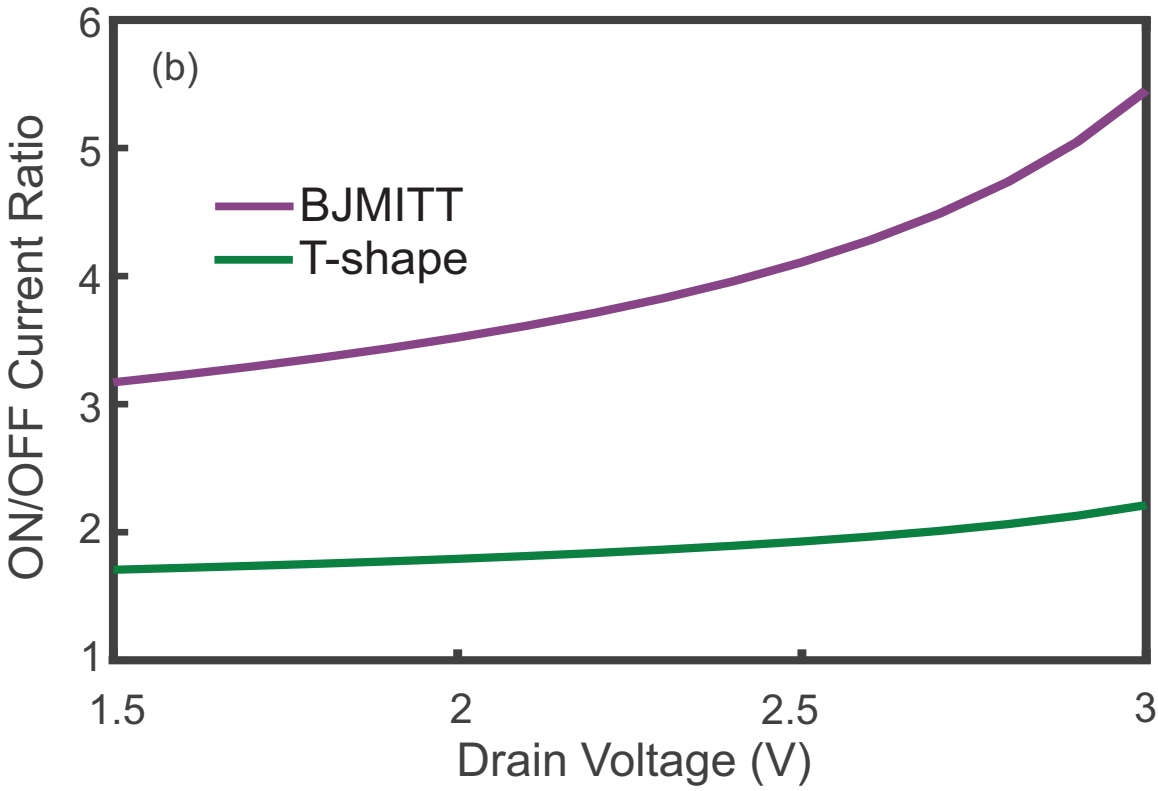

Figure 4.2: Comparison of the ON and OFF currents of the illustrated BJMITT and T-shaped MITT devices. The T-shaped MITT device current is offset with respect to the BJMITT current due to the increased deep channel current contribution.

compared to the ON and OFF of a T-shaped MITT having the same l_{Ch}, l_G and r_S. While the T-shaped MITT has a higher magnitude of current due to the larger 5nm region, the difference in current between the ON and OFF states is lower when compared to the BJMITT. Shown in Fig. 4.3, the ratio of ON to OFF current is 2.5× larger for the BJMITT at $V_D = 3$V due to the improved gate field penetration. The ON/OFF ratio is a critical metric for evaluating the performance of transistor devices, and the improvements shown here validate the BJMITT as an superior device.

The stark difference in field penetration is evident from Fig. 4.4(a), where the potential change between the source and drain (for $V_D = V_S = 0$V and $V_G = 3$V) is plotted. The corresponding channel length plotted in Fig. 4.4(b) shows how the T-shaped device has the least amount of field penetration at the location where the channel length the shortest. While the T-shaped device does have a greater magnitude

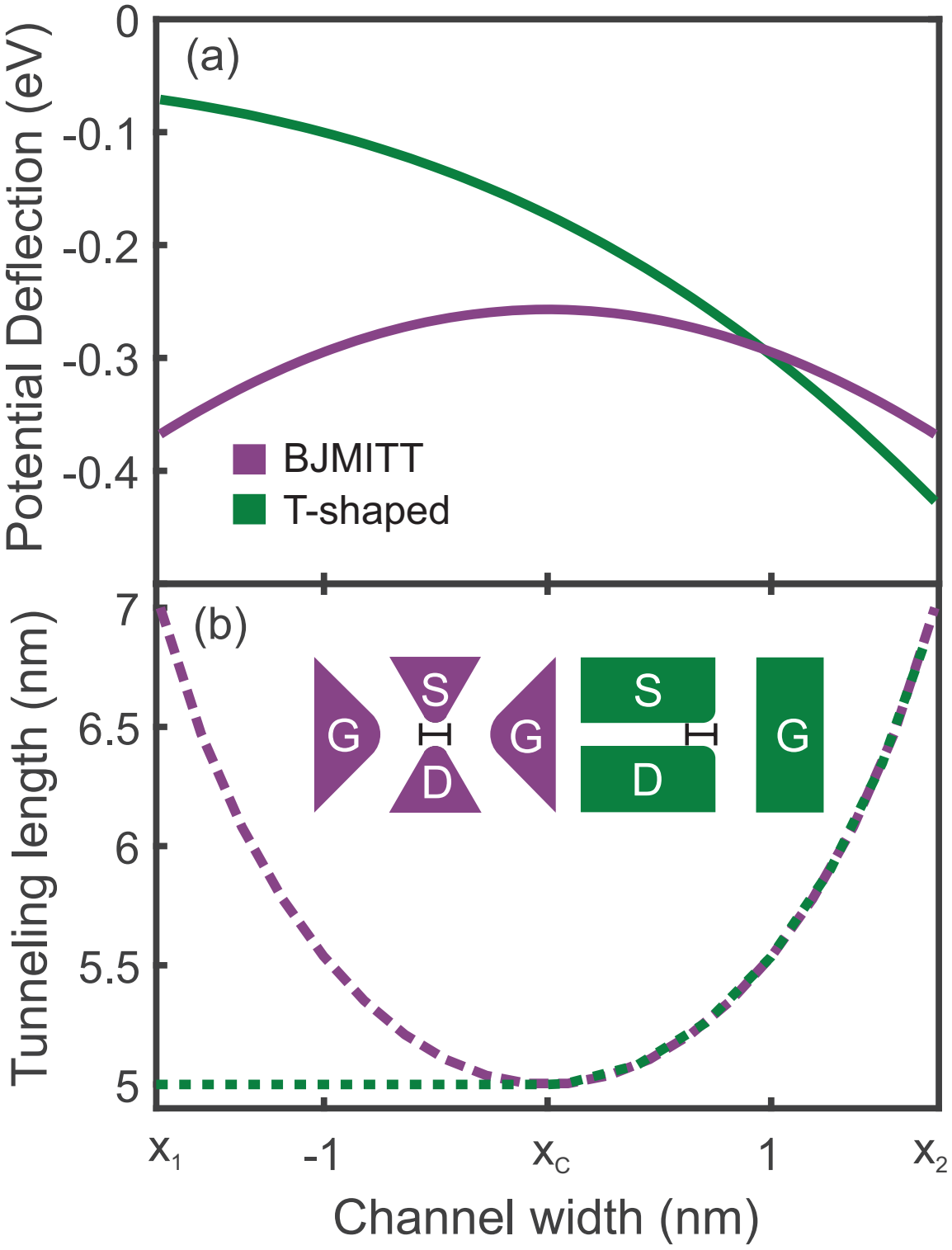

Figure 4.3: (a) the potential deflection of the BJMITT and T-shaped MITT with $V_D = V_S = 0$V and $V_G = 3$V (b) the tunneling length along y for the BJMITT and T-shaped MITT between x_1 and x_2. The inset of (b) indicates where the potential deflection was measured.

of deflection than the BJMITT for $x \geq 1$nm, this occurs where the tunneling length is greater than 5nm, and the current contribution is decreased significantly. At locations where the tunneling length is 5nm, it is clearly shown that the T-shaped device has reduced gate field penetration when compared to the BJMITT, leading to the disparity in ON/OFF ratio.

4.3.1 Improving the T-shaped MITT Performance

While this work is focused on MITT devices with homogeneous insulator layers, the ability to fabricate the T-shaped device using conventional fabrication techniques leads to an ability to fabricate a non-homogeneous insulating layer, which may be used to address the issues outlined above for the T-shaped device. As will be shown below, the proposed fabrication technique would allow for the active region (channel area) to be a different insulator than the remaining insulator region of the device. While this does not address the gate field penetration issue, it does address the leakage current issue. A material with a high band gap, such as SiO_2 may be used to fill the areas outside of the active region, with a lower bandgap insulator used in the active region, essentially creating a channel between source and drain adjacent to the gate with a lower potential barrier. A BJMITT device having similar non-homogeneous insulator features would not be possible to fabricate based on any known techniques.

It should be noted however, that for a non-homogeneous T-shaped device, the disparity in dielectric constant for each of the insulators used in the device would have an effect the ability of the gate field to modulate the potential in the channel region. In general, insulators with a lower electron affinity χ have a dielectric constant than ZrO_2. For planar MIIM devices, the potential barrier within the insulating layer with a low dielectric constant has a greater slope when compared to the high dielectric constant ZrO_2 layer. It is predicted that this will decrease the gate field penetration and, as we have shown, will lead to a reduction in device performance.

4.4 Proposed Fabrication Process

This section covers a proposed fabrication process for the T-shaped MITT device. The process has not been tested and multiple steps would likely require determination of the best option for executing the step, based on available resources, along with testing and optimization of the steps.

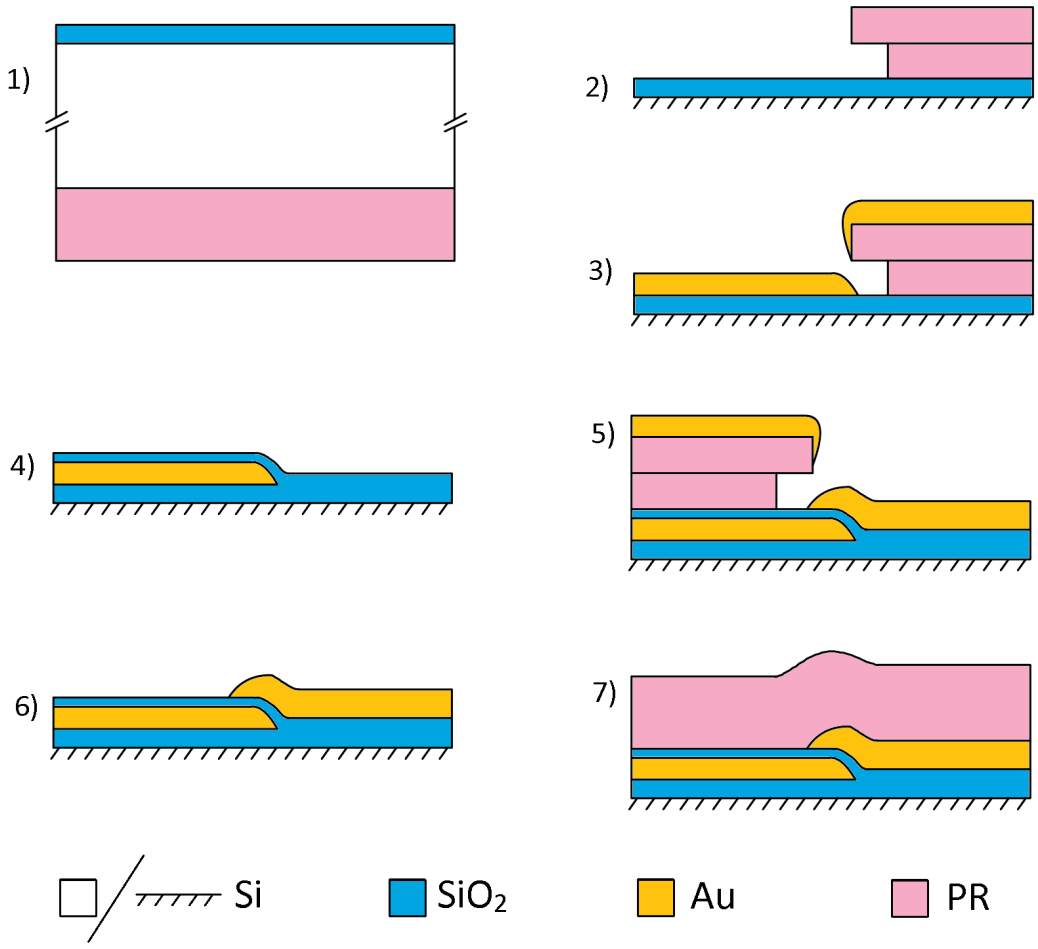

Figure 4.4: 1) Protective resist and ALD SiO_2. 2) Bilayer resist formation. 3) Deposition of Au. 4) ALD SiO_2. 5) Second bilayer resist and second deposition of Au to form the MIM junction. 6) lift off process. 7) Protective resist layer.

The process requires a double-sided polished silicon wafer having a <100> crystal orientation on the faces of the wafer. As both sides of the wafer are used, care must be taken to avoid affecting either surface. To this end, the first step is to apply a

protective layer of photoresist (PR) on one side of the wafer (herein the "bottom" side), as shown in step 1 of FIG. 4.4. The photoresist layer may be applied by a spin coat, and should use a photoresist suitable for use in an ALD machine. If proper care can be taken to not affect either surface of the wafer during fabrication, this or other protective resist steps may be omitted. The photoresist may also be exposed or not, depending on the type of resist used during other processing steps. On the opposite side of the wafer (herein the "top" side), a 20 nm layer of SiO_2 is deposited by ALD on the entire surface.

In step 2, a bilayer resist is applied, exposed, and developed to pattern a first side of the MIM junction, that is connected to a contact pad. In step 3, 100nm of Au is deposited via electron beam evaporation. Sputtering may be used, however, e-beam evaporation is preferred due to better uniformity of direction of the evaporated atoms.

In step 4, the bilayer resist is removed, and 5nm of SiO_2 is deposited on the entire top surface of the wafer by ALD, using a similar process as above. In step 5, a second bilayer resist is applied, exposed, developed to define the second side of the MIM junction, connected to a second contact pad. As Au is to be deposited again, the amount of overlap in deposition of gold to form the MIM junction is key. Less overlap is better for the device performance; however, uncertainty in the actual dimensions of both the developed resist and the edge of the deposited gold will exist. A mask (or masks) made would preferably include a number of devices, with the "expected" overlap of the two gold deposits varying between each device from less than zero overlap to 1-2microns. The deposition profiles of the gold in Figs. 4.4-4.6 are an approximation of the expected profiles, and creating a number of devices increases the chance of that expected profile being realized. Step 6 shows the removal of the second bilayer resist. In step 7, the protective photoresist layer on the bottom has been removed, and a protective photo resist layer has been applied to the top of the wafer.

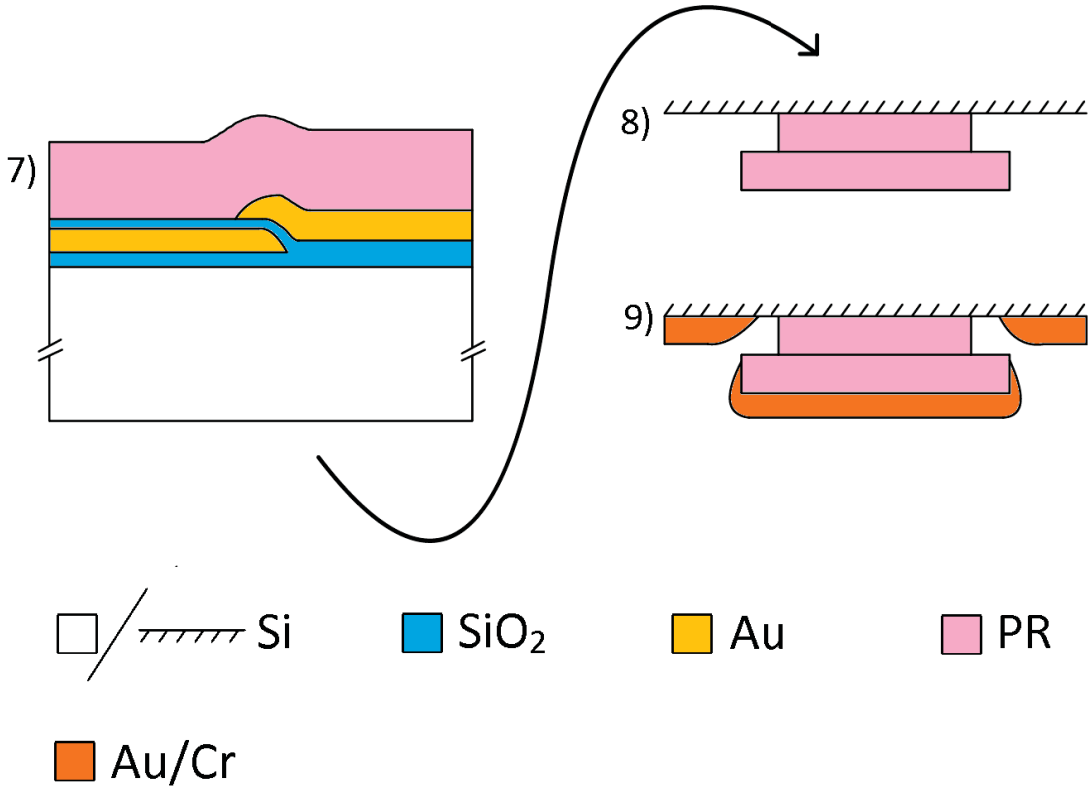

Figure 4.5: 7) Protective resist layer. 8) Backside bilayer resist formation. 9) Deposition of Au/Cr mask.

Referring to Fig. 4.5, the bottom side of the wafer, with the <100> surface silicon exposed, is patterned with a bilayer photoresist to create an etch mask for anisotropic etching of the silicon in step 8. In step 9, a 1 micron or greater etch mask of a mixture of Au and Cr is deposited to define the area in which the Si will be etched. The dimensions of the etch mask window shown in step 9 will depend on the thickness of the wafer, and will need to be aligned with the overlap region on the opposite side of the wafer.

Once the Au/Cr etch mask has been deposited, the bilayer resist and the protective resist on the top side of the wafer are removed, and a layer of Au/Cr at 1 micron thick is deposited across the entire top side of the wafer.

Referring now to Fig. 4.6, step 10 shows the result of the anisotropic etch of silicon

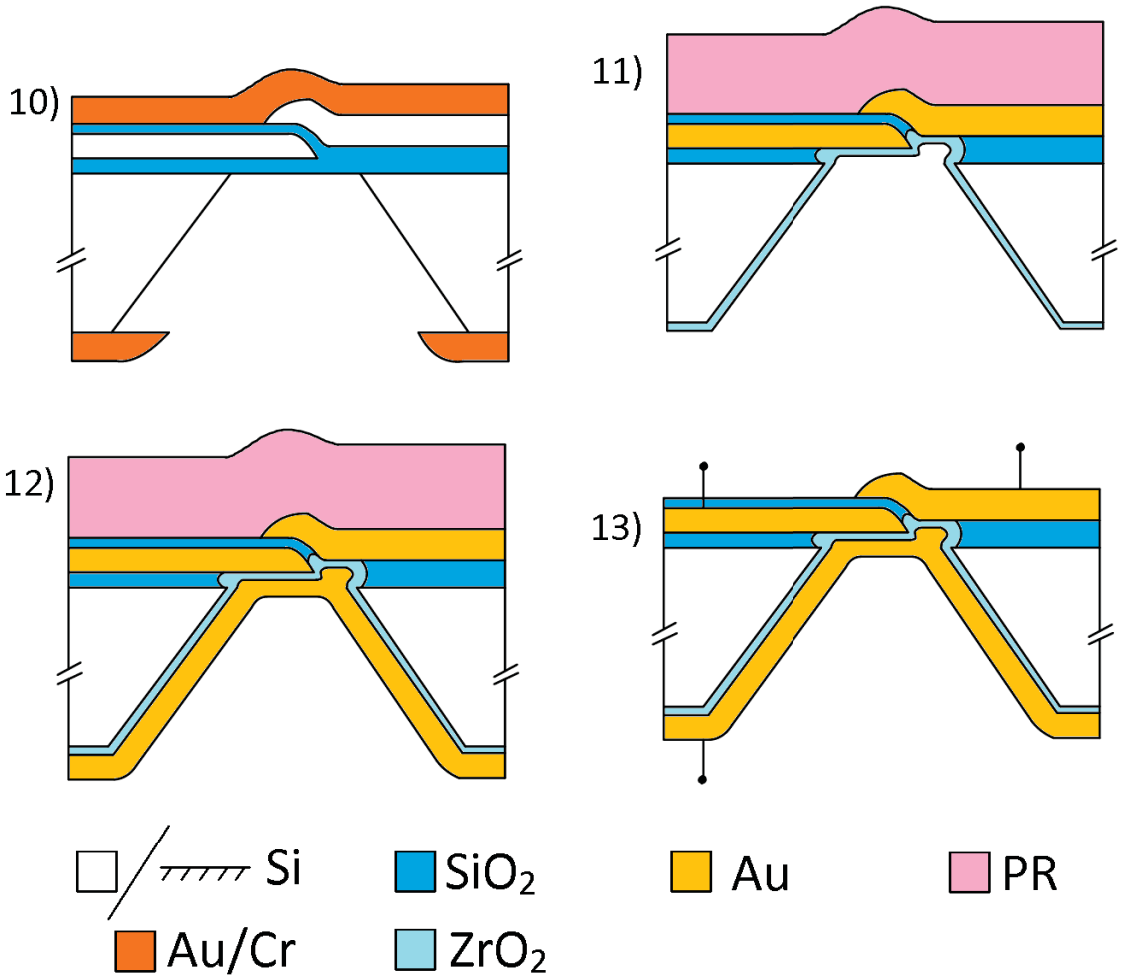

Figure 4.6: 10) Anisotropic KOH etching of Si. 11) Protective PR layer and ALD ZrO_2. 12) Deposition of Au gate contact 13) Final removal of protective layers.

through the entire wafer, to expose the underside of the MIM junction, still covered by the initial 20nm SiO_2 layer from step 1. At step 11, the Au/Cr layers on both sides of the wafer have been removed with a Cr etch, which will not etch the gold underneath the top layer. Another protective layer of PR has been applied to the top side of the wafer, and a short etch in buffered oxide etch of the SiO_2, now exposed on the bottom of the wafer, etches a short distance into the MIM junction. The SiO_2 removed from the MIM junction should be less than 20nm, but is preferably less than 10 nm. Step 11 also shows a 10nm layer of ZrO_2 deposited by ALD on the bottom

side of the wafer. The ZrO_2 fills in the MIM junction area from which the SiO_2 was removed, and creates a smaller region of *Au*-ZrO_2-*Au*.

At step 12, 200nm of Au is deposited on the bottom of the wafer to form the gate contact. Again, e-beam evaporation is preferred. In this case, the entire bottom may be covered such that the layer of gold acts as a common gate for all the devices patterned on the top side of the wafer. After the last protective layer of PR is removed from the top of the wafer, the devices are finished, and the source, drain, and gate contacts are as shown in step 13 of Fig. 4.6.

4.5 Summary

In this chapter, we compared the BJ-MITT to a T-shaped MITT. The BJ-MITT device has a 2.5 times greater ON/OFF drain current ratio. The dual gate design allows for complete gate field penetration of the channel, resulting in a 5.5 times increase between the OFF and ON currents. A proposed fabrication process using conventional, scalable fabrication techniques is proposed.

Chapter 5

Conclusion

In chapter 2, a model for simulating MITT devices was developed and presented. The model is capable of simulating 2D devices with arbitrary geometry. Some limitations of the model was discussed.

In chapter 3, a dual gate MITT device having a feasible architecture, made from an Au-ZrO_2-Au structure, was introduced. The BJ-MITT. The dependence of performance characteristics on the size of various important features of the device was investigated. It was shown how device performance is strongly correlated to gate field penetration, and how altering features to improve gate field penetration leads to a reduction in overall operating current. Devices based on different material combinations, having a variety of tunnel barrier heights, were presented and it was shown how varying the operating voltage can be optimized for differing barrier heights to achieve better performance characteristics. A process for fabricating a proof of concept Au-ZrO_2-Au device is presented.

In chapter 4, the operation of the dual gate Au-ZrO_2-Au device was compared with a single gate, CMOS-style, T-shaped Au-ZrO_2-Au device. It was shown how device performance can be improved based on changes in geometry to improve gate field penetration. A fabrication process for the T-shaped device was presented. The

proposed process uses scalable fabrication techniques.

5.1 Future Directions

Other than continuing the fabrication efforts of both sections 3.7 and 4.4, the following areas are of interest to continue the study of MITT devices.

5.1.1 Control of Trap Assisted Tunneling

In Chapter 2, trap assisted tunneling was discussed as a transport system that could be integrated into the simulation model to better simulate feasible devices. The introduction of defects into the insulator region of the MITT devices poses an interesting question - could the MITT devices have defect regions engineered to control the trap assisted tunneling by the gate field?

A sketch of this process is shown in Fig. 5.1, where defects are introduced at within the channel region, centered between the source and drain contacts. If the energy level of the traps created by the defect could be predicted (or even controlled). As the energy level of the traps would be lower than the conduction band of the insulator, a MITT device operated in this manner would have advantages.

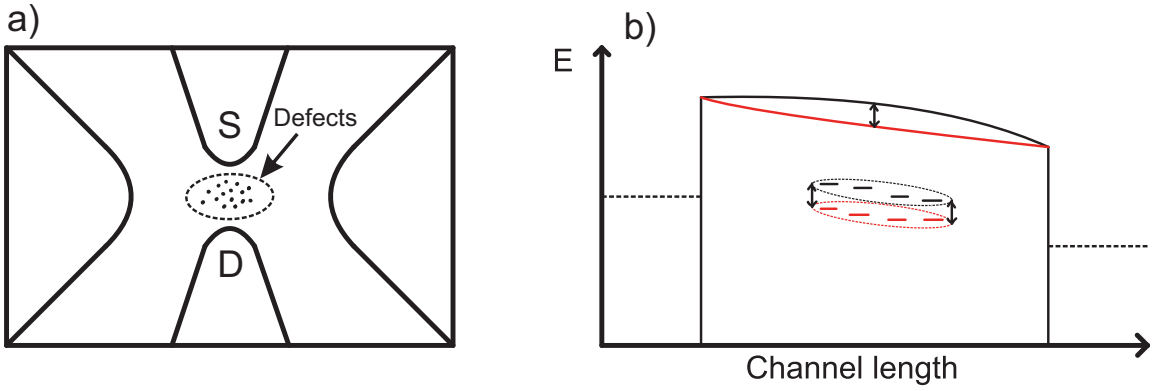

Figure 5.1: a) 2D schematic of a BJMITT device with defects introduced and localized in the channel. b) Band diagram showing the modulation of traps within the insulator by the gate field.

Larger channel length devices would likely be more feasible, as well as devices

made from insulators with larger bandgaps. Since there would not be the need to utilized field emission to generate electron tunneling, operating voltage could be lower when compared to the device in this thesis.

The challenge of this direction of study is in the fabrication. Defects would have to be engineered with no more than 1-2nm of precision, which is exceedingly difficult, if not impossible. A He ion FIB has the potential to be used, as it can create defects in material[48], however it would even have to be determined if that is a realistic possibility.

5.1.2 Multi-oxide MITT

MIIM diodes exhibit resonant tunneling and that effect, combined with the MITT structure, would likely produce devices with excellent performance characteristics. A sketch of such a device is shown in Fig. 5.2.

Applying a gate field to control the energy level of the potential well of an MIIM junction created by the dissimilar insulators would likely produce a device with excellent performance characteristics. It has been shown that when the potential well of an MIIM diode, drops below the fermi level of the metal current increases dramatically. [21]

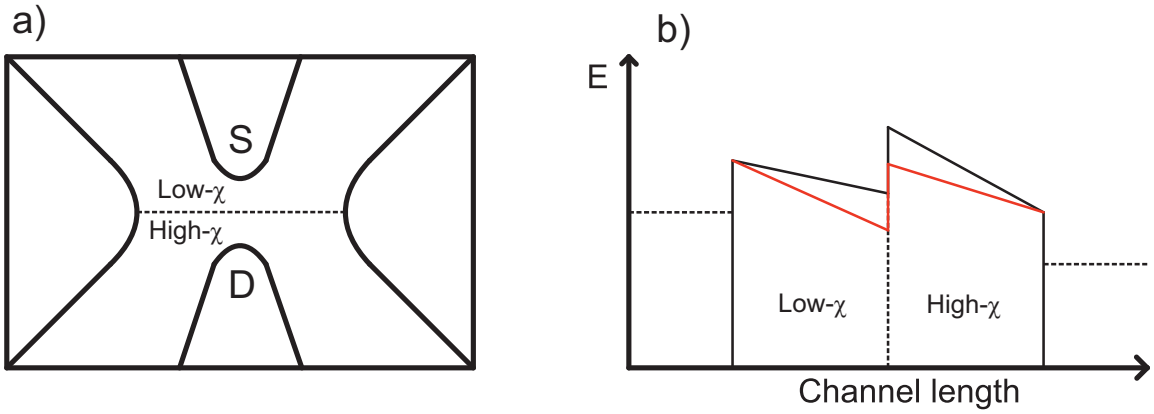

Figure 5.2: a) 2D schematic of a BJMITT device with a MIIM structure across the channel. b) Band diagram showing the modulation of the potential well created by the dual insulators.

However, an MITT device utilizing an MIIM structure likely falls out of the realm of feasibility. While it is an interesting thought experiment, and the model of Chapter 2 could be used to simulate such a device, the author of this thesis has not been able to theorize a way to fabricate such a device. The degree of difficulty and precision required likely falls outside what is possible using fabrication techniques available at the date this was written.

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Appendix A

MATLAB code

A.1 Launching Program

```
clear;
clc;
close all;

FEmode = 'wide'; %= 'CMP_wide';

simCounts = 1;

CDmin = [0  0   0   0   0   0   0   0   0];
CDmax = [3  3   3   3   3   3   3   3   3];
CDres = [31 31  31  31  31  31  31  31  31];

GBmin = [0  0   0   0   0   0   0   0   0];
GBmax = [3  3   3   3   3   3   3   3   3];
GBres = [61 61  61  61  61  61  61  61  61];

Temp = [300 300 300 300 300 300 300 300 300]; % Kelvin

SEset = 0;

junction_length_vec = [6 3.5 4  4.5 5  5.5 6  6.5 7 ];
gate_width_vec = [20 20 20 20  20  20  20  20  20 ]; % dist between gates or
    size of gate
gate_size_vec = [10 10  10  10  10  10  10  10  10 ];

source_radius_vec = [2 1  1   1   1   1   1   1   1 ];
```

```
Au    = struct('Mat','Au','work', 5.1,'effm',1,'fermi',7);
Cr    = struct('Mat','Cr','work', 4.5,'effm',1,'fermi', 7.31);
Al    = struct('Mat','Al','work', 4.15, 'effm', 1, 'fermi', 11.6);

ZrO2  = struct('Mat', 'ZrO2' ,'aff', 2.75, 'effm', 0.1, 'K', 25);
Cr2O3 = struct('Mat','Cr2O3' ,'aff', 3.3, 'effm', 0.4, 'K', 12);
SiO2  = struct('Mat', 'SiO2' ,'aff', 0.9, 'effm', 0.4, 'K', 3.9);

metal    = {Au   Al   Al   Al   Al   Al   Al   Al   Al  };
insulator1 = {ZrO2 Cr2O3 Cr2O3 Cr2O3 Cr2O3 Cr2O3 Cr2O3 Cr2O3 Cr2O3};
insulator1L= {ZrO2 ZrO2 ZrO2 ZrO2 ZrO2 ZrO2 ZrO2 ZrO2 ZrO2 };
insulator2 = {ZrO2 SiO2 SiO2 SiO2 SiO2 SiO2 SiO2 SiO2 SiO2 };


case 'wide'

tip_radius_vec = [2 2   2   2   2   2   2   2   2];
tip_res_vec   = [0.2 0.2 0.2 0.2 0.2 0.2 0.2 0.2 0.2];
gate_radius_vec = [5 5   5   5   5   5   5   5   5];

for ii = 1:simCounts

Structure = struct('metal', metal{ii}, 'insulator', insulator1{ii});

junction_length = junction_length_vec(ii);
gate_width = gate_width_vec(ii);
gate_size = gate_size_vec(ii);

tip_radius = tip_radius_vec(ii);
tip_res   = tip_res_vec(ii);
gate_radius = gate_radius_vec(ii);

Dmin = CDmin(ii);
Dmax = CDmax(ii);
Dres = CDres(ii);

Gmin = GBmin(ii);
Gmax = GBmax(ii);
Gres = GBres(ii);

T = Temp(ii);

[DEmat,I,Umat,TunPotMat,Jdiffmat,Isub] = TJT_v8_launchable_wide(Structure,
   junction_length, ...
gate_width, gate_size, tip_radius, tip_res, gate_radius, Dmin, Dmax, ...
Dres, Gmin, Gmax, Gres, T);
```

```
savestring = [mode '_' FEmode '_' metal{ii}.Mat '_' insulator1{ii}.Mat '_D'
    num2str(Dmin)...
'_' num2str(Dmax) '_' num2str(Dres) '_G' num2str(Gmin) '_' num2str(Gmax) '_
   '...
num2str(Gres) '_T' num2str(T) '_JL' num2str(junction_length) '_GW'...
num2str(gate_width) '_GS' num2str(gate_size) '_Trad' num2str(tip_radius)...
'_Tres' num2str(tip_res) '_GR' num2str(gate_radius)];

savestring = strrep(savestring, '.', 'p');

file_path = ['C:\Users\Aidan\Documents\Thesis\Simulations\' savestring '.
   mat'];

save(file_path, 'DEmat', 'I', 'Umat', 'TunPotMat', 'Jdiffmat');

clear DEmat I Umat TunPotMat Jdiffmat


end



case 'CMP_wide'

simDepth = [4 5 6 7 8 9 10 2 2];

for ii = 1:simCounts

Structure = struct('metal', metal{ii}, 'junctionInsulator', insulator1{ii},
    'junctionInsulatorL', insulator1L{ii}, 'gateInsulator', insulator2{ii
   });

junction_length = junction_length_vec(ii);
gate_width = gate_width_vec(ii);
gate_dist = gate_size_vec(ii);
source_radius = source_radius_vec(ii);
oxide_dist2 = 0.5;

%                   source_width = source_width_vec(ii);

Dmin = CDmin(ii);
Dmax = CDmax(ii);
Dres = CDres(ii);

Gmin = GBmin(ii);
Gmax = GBmax(ii);
```

```
Gres = GBres(ii);

T = Temp(ii);


[DEmat,I,Umat,TunPotMat,Isub] = TJT_v8_CMP_launchable_wide(Structure,...
junction_length, gate_width, gate_dist,source_radius,oxide_dist2,...
Dmin, Dmax, Dres, Gmin, Gmax, Gres, T, simDepth(ii));

savestring = [mode '_' FEmode '_' num2str(simDepth(ii)) '_' metal{ii}.Mat '
    _' insulator1{ii}.Mat '_' insulator1L{ii}.Mat '_' insulator2{ii}.Mat '
    _D' num2str(Dmin)...
'_' num2str(Dmax) '_' num2str(Dres) '_G' num2str(Gmin) '_' num2str(Gmax) '_
    '...
num2str(Gres) '_T' num2str(T) '_JL' num2str(junction_length) '_GW'...
num2str(gate_width) '_GS' num2str(gate_dist) ...
'_GR' num2str(source_radius)];

savestring = strrep(savestring, '.', 'p');


file_path = ['[filepath]' savestring '.mat'];

save(file_path, 'DEmat', 'I', 'Umat', 'TunPotMat', 'Jdiffmat','Isub');

clear DEmat I Umat TunPotMat Jdiffmat Isub


end
```

A.2 Variable Set up and Final Calculation Function

```
function [DEmat,I,Umat,TunPotMat,Jdiffmat,Isub] = TJT_v8_launchable_wide(
    Structure, junction_length, gate_width, gate_size, tip_radius, tip_res,
     gate_radius, Dmin, Dmax, Dres, Gmin, Gmax, Gres, T)

kB     = 1.38e-23; % Bolztmanns
Temp   = T;        % Temp
q      = 1.602e-19; % Elementary charge
m      = 9.11e-31; % Electron mass
hbar   = 1.054e-34; % Plancks in Js
epsilon = 8.85e-14; % Permittivity of free space (F/cm)

ImageForce = true;
meshPlotOn = true;

[vert,tria,xS,zS,xD,zD,xS_center,zS_center,~,zD_center,xGL,zGL,xGR,zGR,~,
    includeSx,~,~,~,~]...
= create_junction_fib_wide(tip_radius,tip_res,gate_radius,junction_length,
    gate_width,gate_size);

Eres = 1000;

MatInfo.mWork =  Structure.metal.work;   % Metal work function : Au
MatInfo.mFermi = Structure.metal.fermi;  % Metal Fermi Energy (eV)
MatInfo.mEffm =  Structure.metal.effm;   % Metal effective mass (multiple
    of free electron mass) : Au

MatInfo.iAff   =  Structure.insulator.aff;  % Insulator electron affinity (
    eV): Al2O3
MatInfo.iEffm =  Structure.insulator.effm;   % Insulator effective mass (
    multiple of free electron mass): Al2O3
MatInfo.Idiel =  Structure.insulator.K;    % Insulator dielectric constant

ImageForce = true;
Svolt = 0;
Gcount = 0;
TunPotMat = zeros(Gres,Dres,(length(xS_center)),300);
DEmat = zeros(Gres,Dres,(length(xS_center)),Eres);
Isub = zeros(Gres,Dres,(length(xS_center)));
I = zeros(Gres,Dres);
Umat = cell(Gres,Dres);
Jdiffmat = zeros(Gres,Dres,(length(xS_center)),Eres);
for Gvolt = -1*linspace(Gmin,Gmax,Gres)
Gcount = Gcount + 1;
Dcount = 0;
```

```
for Dvolt = -1*linspace(Dmin,Dmax,Dres)
Dcount = Dcount + 1;

[U] = solve_potential_fib_math(vert,tria,MatInfo,Svolt,Dvolt,Gvolt,xS,zS,xD
    ,zD,xGL,zGL,xGR,zGR);

potPlot.U = U;
potPlot.vert = vert;
potPlot.tria = tria;
Umat{Gcount,Dcount} = potPlot;
Wcount = 0;
for ww = 1:length(xS_center)
Wcount = Wcount + 1;

z1 = zS_center(ww);
z2 = zD_center(ww);
x1 = includeSx(ww);

xVec(Wcount) = xS(ww+1) - xS(ww);

xtemp = linspace(x1,x1,300);
ztemp = linspace(z1,z2,300);

junction_sub_length(Wcount) = z1 - z2;

tunnel_potential = griddata(vert(:,1),vert(:,2),U,xtemp,ztemp)+ MatInfo.
    mFermi...
+ MatInfo.mWork - MatInfo.iAff;

if ImageForce

Twidth = junction_sub_length(Wcount)*1e-9;
x = linspace(0,Twidth,300);
ImgCorr = zeros(1,300);
k1 = -1;
k2 = -1;

for kk = 2:299
for ll = 0:11
ImgCorr(kk) = ImgCorr(kk) - ((q.^2)/(16*pi*MatInfo.Idiel*epsilon*100))*...
((k1*k2).^ll)*(k1/(x(kk)+ll*((Twidth))) + k2/((ll+1)*((Twidth))...
- x(kk)) + 2*k1*k2/((ll+1)*((Twidth))));
end
end

tunnel_potential = q*tunnel_potential - ImgCorr;
tunnel_potential(1) = 0;
```

```
tunnel_potential(end) = 0 + Dvolt*q;
end

TunPotMat(Gcount,Dcount,Wcount,:) = tunnel_potential;

Emin = MatInfo.mFermi-1.5;
Emax = MatInfo.mFermi+0.5;
Eres = 1000;

Evec = linspace(Emin,Emax,Eres);
% tic
%        DEvec = zeros(1,Eres);
Jdiffvec = zeros(1,Eres);
for Ecount = 1:Eres

Evar = Evec(Ecount);
[DE] = find_DE_FET_launchable(tunnel_potential,junction_sub_length(Wcount),
   MatInfo,Evar);

DEmat(Gcount,Dcount,Wcount,Ecount) = DE;

E = q*Evec(Ecount);
Esym = sym(E);
Efs = q*MatInfo.mFermi;
Efd = q*(MatInfo.mFermi+Dvolt);
Et = kB*Temp;

Jdiffsym = (q.*m.*1.*kB.*Temp)./(2.*(pi.^2).*(hbar.^3)).*...
DE.*log((1+exp((Efs-Esym)./Et))./(1+exp((Efd-Esym)./Et)));

Jdiff = double(Jdiffsym);
Jdiffvec(Ecount) = Jdiff;
Jdiffmat(Gcount,Dcount,Wcount,Ecount) = Jdiff;

end
Isub(Gcount,Dcount,Wcount) = trapz(Evec.*q,Jdiffvec);
end
Iint(1:Wcount) = Isub(Gcount,Dcount,:);
I(Gcount,Dcount) = trapz(xS_center*(1e-9),Iint);
end
end
end
```

A.3 Function to Draw Device Boundaries and Launch Meshing Program

```
function [vert,tria,xS,zS,xD,zD,xS_center,zS_center,xD_center,zD_center,xGL
    ,zGL,xGR,zGR,preScount,includeSx,includeSz,preDcount,includeDx,
    includeDz] = create_junction_fib_wide(tip_radius,...
tip_res,gate_radius,junction_length,gate_width,gate_size)

zGL = linspace(0,gate_size,gate_size+1);
xGL = linspace(0,gate_size,gate_size+1);

zGL_temp = linspace(-1*sqrt(2).*gate_radius/2,sqrt(2).*gate_radius/2,
    gate_radius*3);
xGL_temp = sqrt(gate_radius.^2 - zGL_temp.^2);

zGL_temp = zGL_temp + zGL(end) + zGL_temp(end);
xGL_temp = xGL_temp + xGL(end) - xGL_temp(1);

zGL = [zGL zGL_temp(2:end)];
xGL = [xGL xGL_temp(2:end)];

zGL_temp = linspace(zGL(end),zGL(end)+gate_size,gate_size+1);
xGL_temp = linspace(xGL(end),0,gate_size+1);

zGL = [zGL zGL_temp(2:end)];
xGL = [xGL xGL_temp(2:end)];

zGR = zGL;
xGR = max(xGL) - xGL + max(xGL) + gate_width;

sim_height = max(zGL);
sim_width = max(xGR);

xS_center = linspace(-1*tip_radius*sin(pi/3),tip_radius*sin(pi/3),2*
    tip_radius/tip_res);
zS_center = -1*sqrt(tip_radius.^2 - xS_center.^2);
zS_center = zS_center + tip_radius + sim_height/2 + junction_length/2;

zS_left  = linspace(sim_height,max(zS_center),gate_size+1);
xS_left  = linspace(tan(pi/6).*(max(zS_center)-sim_height)+xS_center(1),
    xS_center(1),gate_size+1);

zS_right = linspace(max(zS_center),sim_height,gate_size+1);
xS_right = linspace(xS_center(end),tan(pi/6).*(sim_height-max(zS_center))+
```

```
    xS_center(end),gate_size+1);

xS = [xS_left xS_center(2:(end-1)) xS_right] + sim_width/2;
zS = [zS_left zS_center(2:(end-1)) zS_right];

xD = xS;
zD = -1*zS + max(zS);

xD_center = xD(length(xS_left):(length(xS_left)+length(xS_center)-1));
zD_center = zD(length(xS_left):(length(xS_left)+length(xS_center)-1));

xS = xS';
zS = zS';
xD = xD';
zD = zD';
xGL = xGL';
zGL = zGL';
xGR = xGR';
zGR = zGR';

preScount = 6 + length(zS_left);
includeSx = (xS_center + sim_width/2)';
includeSz = zS_center';

preDcount = 4 + length(xS) + length(zS_left);
includeDx = xD(length(zS_left):(length(zS_left)+length(zS_center)-1));
includeDz = zD(length(zS_left):(length(zS_left)+length(zS_center)-1));

%
plot(xS,zS,'o')
hold all
plot(xD,zD,'o')
plot(xGL,zGL,'o')
plot(xGR,zGR,'o')
axis image

% OUTLINE

node = [xGL(1) zGL(1); xGL(end) zGL(end); xS(1) zS(1); xS(end) zS(end);...
xGR(end) zGR(end); xGR(1) zGR(1); xD(end) zD(end); xD(1) zD(1)];

edge = [1 2
2 3
3 4
4 5
5 6
6 7
```

```
7 8
8 1];

% Source Edge
nodeS = [xS(2:(end-1)) zS(2:(end-1))];
nodeS_size = size(nodeS,1);
edgeS = [];

for ii = 1:(nodeS_size-1)
edgeS = [edgeS; ii ii+1];
end

nodeSize = size(node,1);

node = [node; nodeS];
edge = [edge; 3 nodeSize+1; (edgeS+nodeSize); nodeSize+nodeS_size 4];

% Drain Edge
nodeD = [xD(2:(end-1)) zD(2:(end-1))];
nodeD_size = size(nodeD,1);
edgeD = [];
for ii = 1:(nodeD_size-1)
edgeD = [edgeD; ii ii+1];
end

nodeSize = size(node,1);

node = [node; nodeD];
edge = [edge; 8 nodeSize+1; (edgeD+nodeSize); nodeSize+nodeD_size 7];

% LEFT Gate Edge
nodeGL = [xGL(2:(end-1)) zGL(2:(end-1))];
nodeGL_size = size(nodeGL,1);
edgeGL = [];
for ii = 1:(size(nodeGL,1)-1)
edgeGL = [edgeGL; ii ii+1];
end

nodeSize = size(node,1);

node = [node; nodeGL];
edge = [edge; 1 nodeSize+1; (edgeGL+nodeSize); nodeSize+nodeGL_size 2];

% Gate Edge
nodeGR = [xGR(2:(end-1)) zGR(2:(end-1))];
nodeGR_size = size(nodeGR,1);
edgeGR = [];
```

```
for ii = 1:(size(nodeGR,1)-1)
edgeGR = [edgeGR; ii ii+1];
end

nodeSize = size(node,1);

node = [node; nodeGR];
edge = [edge; 6 nodeSize+1; (edgeGR+nodeSize); nodeSize+nodeGR_size 5];

part{1} = [1 2 3 4 5 6 7 8];

hfun = @size_funtion;

xmid = sim_width/2;
zmid = sim_height/2;

[vert,etri,tria,tnum] = refine2(node,edge,part,[],hfun,xmid,zmid) ;

figure(1)
patch('faces',tria(:,1:3),'vertices',vert, ...
'facecolor','w', ...
'edgecolor',[.2,.2,.2]) ;
hold on; axis image off;
patch('faces',edge(:,1:2),'vertices',node, ...
'facecolor','w', ...
'edgecolor',[.1,.1,.1], ...
'linewidth',1.5) ;

drawnow;

end
```

A.4 Function to Solve 2D Potential

```
function [U] = solve_potential_fib_math(vert,tria,matInfo,Svolt,Dvolt,Gvolt
    ,xS,zS,xD,zD,xGL,zGL,xGR,zGR)

Ne = length(tria);
N  = length(vert);

K = zeros(N,N);
b = zeros(N,1);

for e = 1:Ne
Ke = zeros(3,3);
be = zeros(3,1);

x1 = vert(tria(e,1),1);
z1 = vert(tria(e,1),2);

if inpolygon(x1,z1,xS,zS)
K(tria(e,1),tria(e,1)) = 10^30;
b(tria(e,1),1) = Svolt*10^30;
end
if inpolygon(x1,z1,xD,zD)
K(tria(e,1),tria(e,1)) = 10^30;
b(tria(e,1),1) = Dvolt*10^30;
end
if inpolygon(x1,z1,xGL,zGL) || inpolygon(x1,z1,xGR,zGR)
K(tria(e,1),tria(e,1)) = 10^30;
b(tria(e,1),1) = Gvolt*10^30;
end

x2 = vert(tria(e,2),1);
z2 = vert(tria(e,2),2);

if inpolygon(x2,z2,xS,zS)
K(tria(e,2),tria(e,2)) = 10^30;
b(tria(e,2),1) = Svolt*10^30;
end
if inpolygon(x2,z2,xD,zD)
K(tria(e,2),tria(e,2)) = 10^30;
b(tria(e,2),1) = Dvolt*10^30;
end
if inpolygon(x2,z2,xGL,zGL) || inpolygon(x2,z2,xGR,zGR)
K(tria(e,2),tria(e,2)) = 10^30;
b(tria(e,2),1) = Gvolt*10^30;
end
```

```
x3 = vert(tria(e,3),1);
z3 = vert(tria(e,3),2);

if inpolygon(x3,z3,xS,zS)
K(tria(e,3),tria(e,3)) = 10^30;
b(tria(e,3),1) = Svolt*10^30;
end
if inpolygon(x3,z3,xD,zD)
K(tria(e,3),tria(e,3)) = 10^30;
b(tria(e,3),1) = Dvolt*10^30;
end
if inpolygon(x3,z3,xGL,zGL) || inpolygon(x3,z3,xGR,zGR)
K(tria(e,3),tria(e,3)) = 10^30;
b(tria(e,3),1) = Gvolt*10^30;
end

a(1) = z2-z3;
a(2) = z3-z1;
a(3) = z1-z2;

bl(1) = x3-x2;
bl(2) = x1-x3;
bl(3) = x2-x1;

Area = 0.5*det([1 x1 z1;1 x2 z2;1 x3 z3]);

% Calculate local stiffness matrix
for p = 1:3
for q = 1:3
Ke(p,q) = (-1/(4*Area))*(a(p)*a(q)+bl(p)*bl(q));
end
end

% Calculate Global stiffness matrix
for p = 1:3
i = tria(e,p);
for q = 1:3
j = tria(e,q);
K(i,j) = K(i,j) + Ke(p,q);
end
b(i,1) = b(i,1) + be(p);
end

end

U = K\b;
```

```
figure(5)
trisurf(tria,vert(:,1),vert(:,2),U)
drawnow;

end
```

A.5 Function to Calculate D(E) Values

```
function [DE] = find_DE_FET_launchable(tunnel_potential,junction_length,
    MatInfo,Evar)

hbar = 1.054e-34; % Plancks in Js
m    = 9.1094e-31; % rest mass of electron
q    = 1.6e-19;   % elementry charge

iEffm = MatInfo.iEffm;
mEffm = MatInfo.mEffm;

E = Evar.*q;
N = 298;

x = (1e-9)*linspace(0,junction_length,N+2);

meff = iEffm*ones(length(x))*m;     % Generate effective mass array
meff(1) = mEffm*m;
meff(end) = mEffm*m;

k = zeros(N+2,1);
S = zeros(N+1,1);
M = zeros(2,2,N);

U = tunnel_potential;

% Generate k array
for n = 1:N+2
k(n) = sqrt(2*meff(n)*(E-U(n)))/hbar;
end

% Generate S array
for n = 1:N+1
S(n) = (meff(n+1)/meff(n))*(k(n)/k(n+1));
end

% Fill M matries
for n = 1:N+1
a = (1+S(n))*exp(-1i*(k(n+1)-k(n))*x(n));
b = (1-S(n))*exp(-1i*(k(n+1)+k(n))*x(n));
c = (1-S(n))*exp(1i*(k(n+1)+k(n))*x(n));
d = (1+S(n))*exp(1i*(k(n+1)-k(n))*x(n));

M(:,:,n) = 0.5 * [a b; c d];
```

```
end

% Combine M matrices
Mt = M(:,:,N+1);
for n = 1:N
Mt = Mt*M(:,:,N+1-n);
end

AN1 = (meff(N+2) * k(1))/(meff(1) * k(N+2) * Mt(2,2));
DE = ((meff(1) * k(N+2))/(meff(N+2) * k(1)))*abs(AN1)^2;

end
```