University of Alberta

Nanostructured Inductors for Millimetre-Wave Applications

by

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Abstract

Modern integrated and system-on-chip electronics require high-quality on-chip passive components. Existing inductor designs for microwave and millimetre-wave applications are typically prohibitively large and have low quality factors, requiring circuit designers to avoid integrating them or to use less desirable alternatives. This research studied vertical on-chip inductor structures through electromagnetic simulations and measurements on two materials. Simulations demonstrated that magnetic anisotropic materials produce useful inductances and quality factors at microwave frequencies. Thin magnetic films deposited using glancing angle deposition were fabricated as inductors and measured up to 70 GHz, producing inductances as high as $1\ \mathrm{nH/\mu m^2}$, which is significantly higher than other CMOS compatible technologies reported to date. The highest quality factor measured for the films was 3, with the measurements suggesting that the quality factor continues to increase at higher frequencies. Carbon nanotube inductors were also fabricated and measured, however, the contact resistance was found to be prohibitively high.

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List of Symbols and Abbreviations

C	Symbol for capacitance
CNT	Carbon nanotube
GLAD	Glancing angle deposition
j	Symbol for the imaginary number ($j = \sqrt{-1}$)
L	Symbol for inductance
MMW	Millimetre-wave
MMWI	Millimetre-wave inductor
MWCNT	Multi-wall carbon nanotube
NSF	Nano-structured film
Q	Symbol for the quality factor
R	Symbol for resistance
S-Parameters	Scattering parameters
SWCNT	Single wall carbon nanotube
X	Symbol for reactance
Z	Symbol for impedance ($Z = R + jX$)
Z-Parameters	Impedance Parameters

Chapter 1: **Introduction to Inductors at GHz Frequencies**

1.1 Inductors and Circuits

1.1.1 Introduction

This thesis discusses the challenges involved in integrating inductors into modern radio-frequency integrated circuits (RFICs) and proposes new nanotechnology-based inductor designs for on-chip inductors.

This thesis begins with an overview of modern inductor designs in the first chapter. The subsequent chapters introduce vertically-aligned nanoscale structures for on-chip inductors, including simulations and fabricated device measurements.

1.1.2 Ubiquitous computing and advanced communications

The last several decades have brought about great advances in semiconductor technology which has made portable electronic devices an indispensable part of our daily lives. Many advanced electronic circuits and systems are now inexpensively available to the general public in the form of laptops, tablets, smartphones, global positioning systems (GPS), heath monitoring devices, and many others. In addition to core computing, many of these portable electronic devices contain advanced radio technologies for communicating with other portable and stationary devices.

These advanced communicating devices require small and low-power transceivers to send and receive signals to base stations and each other [1]. Integrated transceivers are complex devices that are often built monolithically in a single chip. Transceivers, like any circuit, are constructed out of transistors, resistors, capacitors and inductors. Although transistors have been aggressively scaled down to nanometer sizes, passive components such as inductors and capacitors have not noticeably scaled [2]. The scaling behaviour for inductors is a significant problem in modern high-frequency electronic systems design because the area of a single spiral on-chip inductor is a thousand times larger than a transistor. This area inefficiency has motivated efforts to build circuits with a minimum number of inductors or to look for alternative technologies for implementing on-chip inductors. Moreover, the low quality factor of integrated inductors, due to metal and substrate losses, poses a significant challenge to overcome in the design of modern CMOS radio frequency integrated circuits [3].

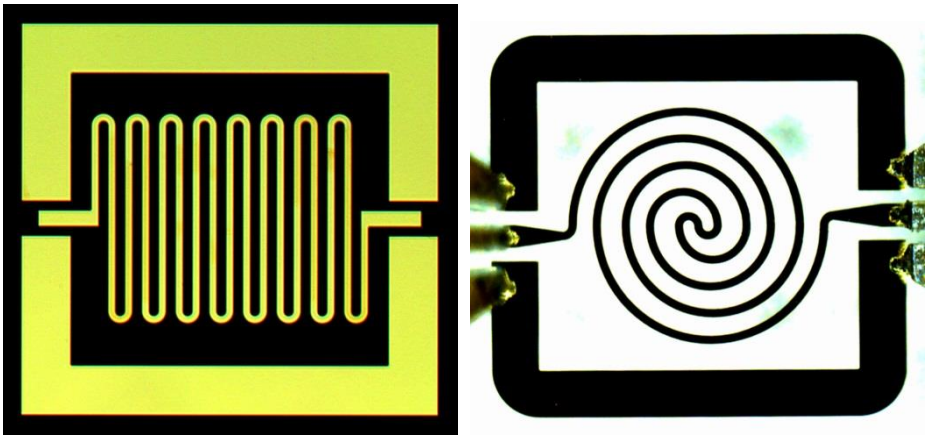
This thesis will discuss the challenges associated with building modern integrated inductors, using modern inductor technologies, and it will propose new inductor technologies for radio-frequency applications.

1.1.3 What are inductors

Inductors are one of the fundamental electronic components, along with resistors, capacitors and transistors. Inductors are useful in a wide variety of applications, ranging from power system transformers to microwave filters. Large scale, discrete inductors are typically made by wrapping coils of wire around a core material such that the magnetic field from each of the wires adds in a constructive manner to create a large magnetic field in the core material. Due to the creation of the magnetic field, inductors resist changes in currents flowing through the device.

While discrete inductors are relatively simple to build, the field of integrated electronics is based on planar fabrication technology involving the deposition and patterning of layers of materials. These layers are deposited on to the chip and patterned in an iterative process until they have been built up into functioning device. This planar fabrication technology limits the devices created to a primarily 2-dimensioal structure. Vertical connections between layers are possible; however, it is necessary that any device fabricated on-chip have only 2 principle dimensions. In other words, all devices on a modern chip should be planar.

Unfortunately, solenoid structures are intrinsically 3-dimensional and do not translate well into planar structures. To avoid the use of 3D structures, a number of 2-dimensional designs have been developed and are currently used in commercial devices, such as the designs shown in Figure 1.1. These 2D structures mainly consist of spiral inductors (shown in Figure 1.1b), but they have many drawbacks compared to 3-dimensional des[4]igns. For example, planar inductors suffer from large parasitic coupling to the substrate, inducing losses and limiting their maximum operation frequency in addition to occupying significantly larger areas than their 3D counterparts of the same inductance. A typical area for a 1 nH on-chip inductor is approximately $10^4\ \mu m^2$ (when implemented as a square-spiral), which is huge compared to a typical transistor area of only few tens of μm^2 [5][6][7].



(a) Planar meander inductor (b) Planar circular-spiral inductor

Figure 1.1: Planar inductors.

Integrated electrical component sizes are continuously being reduced for increased circuit density, lower power consumption, and increased speed. Recently, inductor designs have not been able to scale as fast as other components. For low frequency and discrete devices, solenoid structures are known to produce high quality inductors with useful inductance values. These structures are used extensively in large discrete devices, such as transformers and electric motors. However, for high frequency integrated devices it is impractical to have large discrete components due to high costs and exact manufacturing requirements. For this reason there is a high demand for small inductor designs that can be integrated on-chip with other electronic components, such as digital CMOS chips.

1.2 A brief overview of the proposed inductor technologies

This thesis will introduce the use of nano-structured materials for millimetre-wave (mm-wave) inductor applications. This research into new materials and structures for mm-wave inductors will attempt to bridge the size and quality gap between inductors and other integrated chip components. The finite element simulations of the proposed inductor devices will be presented as well as measured results from fabricated samples. The resulting inductor technologies show promise, with high inductance and acceptable quality factors in the mm-wave frequency range.

The two nanostructured materials that will be presented are carbon nanotubes (CNTs) deposited with PECVD and nanowire films fabricated by glancing angle deposition (GLAD).

Nanostructured thin films are constructed using fabrication processes that produce wafer-scale arrays of nanoscale structures through techniques such as GLAD. The GLAD technique is based

on physical vapour deposition, which makes it very versatile in the types of materials that can be deposited. This thesis will introduce the use of anisotropic magnetic structures as a building block for integrated RF inductors. These inductors have inductance density when compared to traditional inductor designs and quality factors which are suitable for commercial applications.

Both CNTs and GLAD films are promising alternatives to modern integrated inductor technologies. This thesis will introduce the background necessary to evaluate inductor technologies and explore new materials for advancing the state of modern integrated inductors.

Chapter 2 introduces on theory necessary to evaluate inductor parameters and provides background information about the current state of inductor technologies. Chapter 3 presents the electromagnetic (EM) simulation results for new inductor designs using the proposed material technologies. Chapter 4 presents the measured results for the nanostructured thin film devices and compares these results with the simulation results from chapter 3. Chapter 5 presents the measured results for carbon-nanotube array-based inductors. Finally, chapter 6 concludes this dissertation by summarizing the research work and suggesting directions for our future research.

Chapter 2: **Inductance and Inductors**

2.1 Introduction

This chapter will introduce the concepts behind modern inductors, including the mathematics and theory of inductors. Once the basic concepts have been covered, a survey of the various types of modern inductors will be presented as well as some new technologies that promise improved performance over existing technologies.

2.2 Inductance

2.2.1 Introduction

Inductance is the name given to the physical phenomenon of the creation of an electric field in response to a changing current in a circuit. This phenomenon is an electromagnetic property which is described by Maxwell's equations and that relates changes in magnetic fields to electric fields. Devices that are built to exhibit inductance are called inductors. Inductors are used in many kinds of circuits including filters, resonators, biasing circuits, transformers, and regulators. When the inductance effect is undesired, it is called a parasitic effect and it is often modeled in circuits as extra circuit elements called parasitic elements, typically limiting the performance of a circuit.

Inductance is a frequency-dependent effect, often becoming more important at higher frequencies as the impedance of inductors increases with frequency. This makes inductors especially important in radio-frequency (RF) circuits both because of its uses in RF circuits (eg. filters, biasing, resonators) and its undesired effects. Inductors are especially useful in conjunction with capacitors; together they form resonators which can be used as building blocks for filters, switches, and matching circuits [8]. However, inductors can also be used on their own as RF chokes (open-circuits), transformers, and as RF biasing elements (eg. inductively degenerated biasing).

2.2.2 Maxwell's Equations

Inductance, like all electromagnetic phenomenon, is governed by a set of equations called Maxwell's Equations. Maxwell's equations are the foundation of classical electrodynamics and govern all electromagnetic phenomena [9]. Maxwell's equations can be written as in equations 2.1-2.4 [9].

$$\nabla \cdot \mathbf{E} = \frac{\rho}{\varepsilon_0} \tag{2.1}$$

$$\nabla \cdot \mathbf{B} = 0 \tag{2.2}$$

$$\nabla \times \mathbf{E} = -\frac{\partial \mathbf{B}}{\partial t} \tag{2.3}$$

$$\nabla \times \mathbf{B} = \mu_0 \mathbf{J} + \mu_0 \varepsilon_0 \frac{\partial \mathbf{E}}{\partial t} \quad 2.4$$

Maxwell's equations describe the two vector fields in classical electrodynamics and their interactions with each other, as well as a quantity called charge. The two vector fields are called the electric field (denoted **E**) and the magnetic field (denoted **B**), with charge (ρ) and current (**J**) acting as the physical sources for those fields [9]. However, current is just the movement of charge, making charge the source of all electric and magnetic fields.

Inductance is a derived quantity of Maxwell's equations; the derivation is shown in the next section (section 2.2.3).

2.2.3 Definition

At the beginning of this chapter, inductance was introduced with its definition; that it is the creation of an electric field in response to a change in current. None of Maxwell's equations directly relate a change in current and an induced electric field; however, equation 2.4 relates a current to a magnetic field and equation 2.3 states that a change in a magnetic field produces an electric field. In the quasi-static case, the second term ($\frac{\mu\varepsilon\partial \mathbf{E}}{\partial t}$) **B** causes an electric field [9]. This can be assumed to be equal to 0because the magnetic field produced by a change in **E** is small compared to the field produced by **J**. In this case, if **J** is known, then **B** is also known from equation 2.4. One key point to note from equation 2.4 is that **B** is proportional to **J**, therefore a change in **J** means a proportional change in **B.**With this knowledge, we can note that equation 2.3 directly relates an electric field with a changing magnetic field. However, in this form to solve for the generated electric field, the calculation of a curl is required. To simplify this equation, the curl theorem can be applied and both sides of the equation can be integrated over an area as shown in equation 2.5.

$$\int (\nabla \times \mathbf{E}) \cdot d\mathbf{a} = -\int \frac{\partial \mathbf{B}}{\partial t} \cdot d\mathbf{a} \quad 2.5$$

Then the curl theorem can be applied to the left side [9]:

$$\int (\nabla \times \mathbf{E}) \cdot d\mathbf{a} = \oint \mathbf{E} \cdot d\mathbf{l} \quad 2.6$$

Next, the derivative with respect to time can be taken outside the integral on the right side of equation 2.5. Finally, the integral is just the total magnetic flux through the area $\boldsymbol{a}$, which is denoted by Φ in equation 2.7.

$$-\int \frac{\partial \mathbf{B}}{\partial t} \cdot d\mathbf{a} = -\frac{\partial}{\partial t} \int \mathbf{B} \cdot d\mathbf{a} = -\frac{d}{dt}(\Phi) \quad 2.7$$

One important relation to note from equation 2.7 is that it is just the time derivative of the definition of magnetic flux, shown in equation 2.8.

$$\Phi = \int \mathbf{B} \cdot d\mathbf{a} \tag{2.8}$$

Then the curl theorem can be applied to the left side to change the area integral into a line integral, as shown in equation 2.6 [9].

$$\int (\nabla \times \mathbf{E}) \cdot d\mathbf{a} = \oint \mathbf{E} \cdot d\mathbf{l} = -V \tag{2.9}$$

Where $\mathbf{l}$ is the circumferential loop around the area $\boldsymbol{a}$. The right hand side of equation 2.6 is just the definition of the negative of the voltage around the loop, V.

Finally, substituting the relations from equations 2.7 and 2.6 into equation 2.5 gives equation 2.10.

$$-V = -\frac{d\Phi}{dt} \tag{2.10}$$

Equation 2.10 is not useful for circuit designers because it requires the explicit calculation of the total magnetic flux through a loop and its change with respect to time, which is generally hard. To simplify the calculation, it is useful to note that Φ is proportional to **B** and in the quasi-static case, **B** is proportional to a current I [9]. This constant of proportionality is called the inductance and it is given the symbol L and has the unit of henries (H), as shown in equation 2.11 [9].

$$\Phi = LI \tag{2.11}$$

Substituting equation 2.11 into equation 2.10 yields equation 2.12, which is very useful in circuit analysis.

$$V = L\frac{dI}{dt} \tag{2.12}$$

Equation 2.12 is a very useful equation because it relates inductance to quantities that are easily measured: voltage, current and time. Unlike equation 2.3, all the quantities in equation 2.12 are scalar quantities that don't require vector analysis or calculus to compute. Equation 2.12 says that the inductance of a device can be determined by changing the current running through a device and measuring the voltage produced by the changing current. The voltage produced is always opposing the change in current [9].

2.2.4 Inductance and energy

As magnetic fields store energy, it is possible to use inductance as a convenient way to calculate the magnetic energy stored in a circuit since inductance is the relation between current and a produced magnetic field. The energy stored in the magnetic field of an inductor is given by

equation 2.13, where W is the energy stored in the field, L is the inductance of the device, and I is the current through the device [9].

$$W = \frac{1}{2}LI^2 \tag{2.13}$$

Equation 2.13 provides physical insight into the physical operating principle of inductors: moving current stores energy in the form of a magnetic field. Applying an electric field (ie. a voltage) to a charge causes it to move, creating a current. The current stores energy in a magnetic field. Changing the current causes a change to the magnetic field which in turn creates an electric field. Therefore, energy is converted from magnetic energy into electric energy.

2.2.5 Inductance in the frequency domain and Quality Factor

The primary figure of merit for an inductor is called the quality factor. Similar to capacitors, the quality factor is defined as the ratio of the energy stored in the device to the energy dissipated by the device (equation 2.14) [8][10].

$$Q = \omega \frac{\text{peak energy stored}}{\text{average energy dissipated}} = \frac{\omega(2E_{\text{M}} - 2E_E)}{P_{av}} \tag{2.14}$$

The magnetic energy stored in the circuit can be expressed in terms of the inductance given in 2.13. The energy dissipated by the resistor is given by $P = VI = I^2R$. The electric energy present in a capacitor is given by equation 2.15 [8].

$$E_E = \frac{1}{2}V^2C = \frac{1}{2}I^2\frac{1}{\omega^2 C} \tag{2.15}$$

Combining equations 2.13, 2.14, 2.15 gives equation 2.16.

$$Q = \frac{\omega(2E_M - 2E_E)}{P_{av}} = \frac{\omega\left(2\frac{1}{2}LI^2 - 2\frac{1}{2}I^2\frac{1}{\omega^2 C}\right)}{I^2R} = \frac{\omega L - \frac{1}{\omega C}}{R} = \frac{\Im\{Z\}}{\Re\{Z\}} \tag{2.16}$$

Physically, the energy dissipated by the inductor is due to ohmic losses (heating), parasitic losses (coupling to the substrate) and radiation losses.

The most important result of the definition of the quality factor shown in equation 2.16 is that the quality factor is the tangent of the input impedance phasor of a 1-port device, given by equation 2.17 [11]. It is much easier to measure the impedance of a device than it is to measure the energy stored in the electric and magnetic fields. This equivalent definition of the quality factor is useful for determining the quality factor of an experimental device due to the ease of measuring the impedance of a device. The quality factor can be calculated from the S-parameters measured by vector network analyzers (VNA).

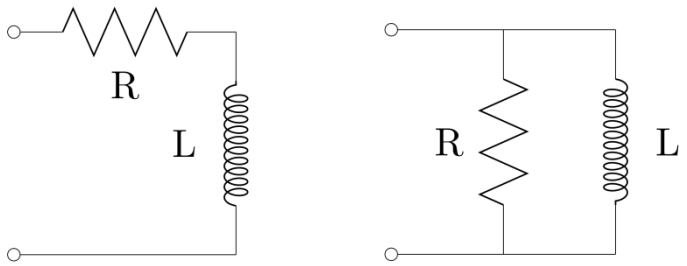
$$Q = \tan\theta = \frac{\Im\{Z\}}{\Re\{Z\}} \qquad 2.17$$

For the purposes circuit modeling, there are two elementary circuits which can simply describe a genetic inductor: an ideal inductor in series or in parallel with a resistor. The total energy dissipated in the inductor is modeled using the resistor and the inductive reactance is modeled with the ideal inductor, shown in Figure 2.1a. The result for a series resistance model for the quality factor is shown in equation 2.18.

$$Q = \frac{\Im\{Z\}}{\Re\{Z\}} = \frac{\omega L}{R} \qquad 2.18$$

If the inductor is modeled with a parallel resistance, as shown in Figure 2.1b, then the resulting quality factor can be calculated by equation 2.17; the result is given by equation 2.19. The resulting quality factor for the parallel circuit is the inverse of the quality factor in the series circuit. For a series circuit, the inductor is ideal if the resistance is equal to 0, however in the parallel circuit the inductor is ideal when the resistance is infinite.

$$Q = \left(\frac{\omega L R^2}{R^2 + \omega^2 L^2}\right)\left(\frac{R^2 + \omega^2 L^2}{\omega^2 L^2 R}\right) = \frac{R}{\omega L} \qquad 2.19$$



(a) (b)

Figure 2.1: Inductor circuits. (a) Inductor model with a series resistance. Increasing the resistance in this model means that more power is lost in the resistor when compared to the inductor. (b) Inductor model with a parallel resistance. Increasing the resistance means that more power is stored in the inductor when compared to the resistor.

Equation 2.14 indicates that the quality factor of an inductor can be understood as a measure of how much energy is stored in the magnetic field compared to the energy lost through operation of

the inductor. An ideal inductor is one that has no real power loss, indicating a device that conserves energy in a circuit. In contrast, a purely restive element converts energy in a circuit to other kinds of energy (eg. mechanical, optical, radiation, heat, etc.). The lack of storage of energy in a resistor means that a resistor has a quality factor of 0.

For most applications of inductors, high quality factor inductors are essential for good system performance. The exception for high quality factors is wideband systems (resonators, impedance matching, etc.) which may require lower quality factors; however, due to the simplicity of building integrated resistive components it is simple to arbitrarily lower the quality factor of a high-quality inductor. A low quality factor means that the inductor exhibits a high resistance in proportion to its reactance, which can introduce noise into a high-frequency circuit [12].

2.3 Magnetic materials

2.3.1 Magnetic polarization in response to an applied field

The relations discussed so far have related the values of **E** and **B** or V and I directly with no discussion of the effect of materials on the magnetic field and the inductance. Similar to the electric polarizability materials, some materials also exhibit a magnetic polarizability in response to applied magnetic fields. This polarization is often denoted by **M** and it contributes directly to the total magnetic field **B** [9].

The magnetic field can therefore be broken up into two components, a component due to free-flowing current (denoted **H**) and a component due to bound atomic currents (**M**). These components are analogous to the electric **D** and **P**, however they tend to be more useful than **D** and **P** in practical scenarios [9]. Therefore, the total magnetic field is given by equation 2.20 [9].

$$\mathbf{B} = \mu_0(\mathbf{H} + \mathbf{M}) \qquad 2.20$$

It is quickly worth noting that authors sometimes refer to **H** as the magnetic field due to its usefulness in solving equations with linear materials [8]; however, this usage is confusing and can lead to a number of incorrect conclusions [9].

A permanent magnet is a simple example of the differences between **B** and **H**. Permanent magnets have a well-understood **B**-field and the **H**-field outside of a permanent magnet is equivalent after scaling by μ_0 ($\mathbf{M} = 0$ outside the magnet) [13]. However, inside the magnet there is a magnetic dipole **M**, which has a divergence on the surface of the magnet. Taking the divergence of equation 2.20 results in equation 2.21, indicating that the **H**-field has a discontinuity on the surface of a permanent magnet and that this can be viewed as a magnetic "charge" [13]. The implication of this charge is that the **H** field acts the same way as an electric field, with field lines going from north

"charge" to south "charge". This behaviour results in an **H** field that is not only different from **B** inside a magnetic material, but is also in the direction opposing **B**.

$$\nabla \cdot \mathbf{H} = -\nabla \cdot \mathbf{M} = \rho_{magnetic} \quad 2.21$$

In general, **M** is an independent property of a material; however, there is a class of materials called *linear materials* for which **M** is proportional to **H**, shown in equation 2.22. The constant of proportionality, χ_m, is called the magnetic susceptibility [9]. Plugging equation 2.22 into equation 2.21 gives equation 2.23, where μ is called the magnetic permeability and it is a material property [9]. Many magnetic materials are linear materials for small values of **H**.

$$\mathbf{M} = \chi_m \mathbf{H} \quad 2.22$$

$$\mathbf{B} = \mu_0(1 + \chi_m)\mathbf{H} = \mu\mathbf{H} \quad 2.23$$

2.3.2 Magnetism

There are a wide variety of materials that respond differently to magnetic fields classified into several groups [14]; however, there are only two forms of magnetism that interact strongly with external applied magnetic fields: ferromagnetism and ferrimagnetism [15].

A ferromagnetic material is a material in which every atom in the lattice spontaneously aligns to have the same magnetic moment, which produces a strong external magnetic field [14][9]. However, despite this alignment of magnetic moments, ferromagnetic materials often do not spontaneously have macroscopic magnetic fields because the aligned atoms form groups [9]. These groups are called domains, which may have a moment in any direction and tend to cancel each other out in a bulk material [14]. Domains can be aligned by an external magnetic field, resulting in a relative permeability for the material which is typically much greater than 1 [9]. Typical examples of ferromagnetic materials include iron, nickel, steel, etc [15].

In contrast to ferromagnetic materials, ferrimagnetic materials tend to be high resistivity compound materials, called ferrites [8]. Ferrimagnetic materials consist of two types of lattice sites: sites that align to external magnetic fields and sites that anti-align to external magnetic fields [14]. The two different lattice sites typically have different magnitudes of their magnetic spin, which produces a net magnetic field [14]. Similar to ferromagnets, ferrimagnets can be aligned to form a macroscopic field by applying an external magnetic field [14]. Ferrimagnets are often used in microwave devices to produce anisotropic materials to make non-reciprocal devices [8].

Since both ferromagnetic materials and ferromagnetic materials have magnetic permeabilities that are greater than 1, they are suitable for use as magnetic cores in inductors [9].

2.4 Loop and Partial Inductance

2.4.1 The inductance problem

Section 2.2.3 showed the definition of inductance and the derivation of inductance from Maxwell's equations; however, the arguments used all contained areas and loops, not single elements. This definition is useful for analyzing devices that contain easily identifiable loops, such as solenoids, however it is much more difficult to analyze more complex structures where the loop may not be easily identifiable or the loop may have multiple devices connected across it. One example of these kinds of complex structures include integrated circuits, which may have many signal and ground lines and often have devices connected between them.

2.4.2 Partial inductance

The solution to the inductance problem is to use an alternate solution to magnetic flux: the magnetic vector potential, **A**. The magnetic flux of a loop can be written in terms of the magnetic vector potential as in equation 2.29 [9]. Whereas the magnetic flux is dependent on the magnetic field and the area of the enclosed loop, it is dependent only on the magnetic vector potential and the circumference of the loop.

$$\Phi = \int \mathbf{B} \cdot d\mathbf{a} = \oint \mathbf{A} \cdot d\mathbf{l} \qquad 2.24$$

This change from area to length is important because the magnetic flux can then be written by knowing only the path and the magnetic vector potential along the path and not the magnetic field over an area. This means that a specific portion of the magnetic flux can be attributed to a specific portion of the loop, which is not possible with the area integral [16]. Due to the properties of integrals, the loop integral can be expressed as a sum of its parts (equation 2.33).

$$\oint \mathbf{A} \cdot d\mathbf{l} = \int \mathbf{A} \cdot d\mathbf{l_1} + \int \mathbf{A} \cdot d\mathbf{l_2} + \cdots = \sum_i \int \mathbf{A} \cdot d\mathbf{l_i} \qquad 2.25$$

Equation 2.25 states that the contour integral of **A** can be split into an arbitrary number of segments and the total integral is equal to the summation of the contribution of each segment. Using this equation, it is possible to express the total magnetic flux as the summation of partial fluxes from each segment [16].

$$\Phi = \Phi_1 + \Phi_2 + \cdots \qquad 2.26$$

Thus, the inductance of an arbitrary segment of conductor can be expressed as equation 2.26.

$$\Phi_{partial} = \int \mathbf{A} \cdot d\mathbf{l}_{partial} \qquad 2.27$$

Combining equation 2.24 with equation 2.27 gives the partial inductance of a current path (equation 2.28).

$$L_{partial} = \frac{\Phi_{partial}}{I} = \frac{\int \mathbf{A} \cdot d\mathbf{l}_{\boldsymbol{partial}}}{I} \qquad 2.28$$

Equation 2.28 is extremely useful in practical applications of inductance calculations because it can be used to express inductances that would be cumbersome or computationally impossible to express using the magnetic field [16]. It can be used to calculate the self or mutual inductances of any set of conductors. Equation 2.28 forms the basis of numerous inductance extraction programs, such as FastHenry [17], [18] and FastMaxwell [19].

2.4.3 Partial Inductance of a straight wire

Two important cases of the calculation of partial inductances are the self-inductance of a single wire and the mutual inductance of parallel wires. All current-carrying conductors have a self-inductance and a mutual inductance term between all other conductors in a system which must be added together to form the total inductance of a device.

Perhaps the most important partial inductance formula is the self-inductance of a straight wire (of circular cross section). The formula for the partial inductance of a single straight wire is given by equation 2.29 [16].

$$L_{wire} = \frac{\mu_0 l}{2\pi}\left[\ln\left(\frac{l}{r} + \sqrt{\left(\frac{l}{r}\right)^2 + 1}\right) - \sqrt{1 + \left(\frac{r}{l}\right)^2} + \frac{r}{l}\right] \qquad 2.29$$

Where L_{wire} is the self-inductance, μ_0 is the permeability of free space, l is the length of the wire, r is the radius of the wire.

The inductance resulting from equation 2.29 is shown in Figure 2.2 for various realistic on-chip trace lengths and widths. The self-inductance of these wires are trivially small, however, the inductance increases as the trace width is reduced or the trace length is increased. In the case of a long wire, where $l \gg r$, then equation 2.29 is reduced to the simpler equation 2.30.

$$L_{wire} = \frac{\mu_0 l}{2\pi}\left[\ln\left(\frac{2l}{r}\right) - 1\right] \qquad 2.30$$

This equation clearly shows a strong dependence on the length of the wire and a weaker dependence on the radius of the wire. Overall equation 2.31 is approximately linear for each order of magnitude of the ratio l/r.

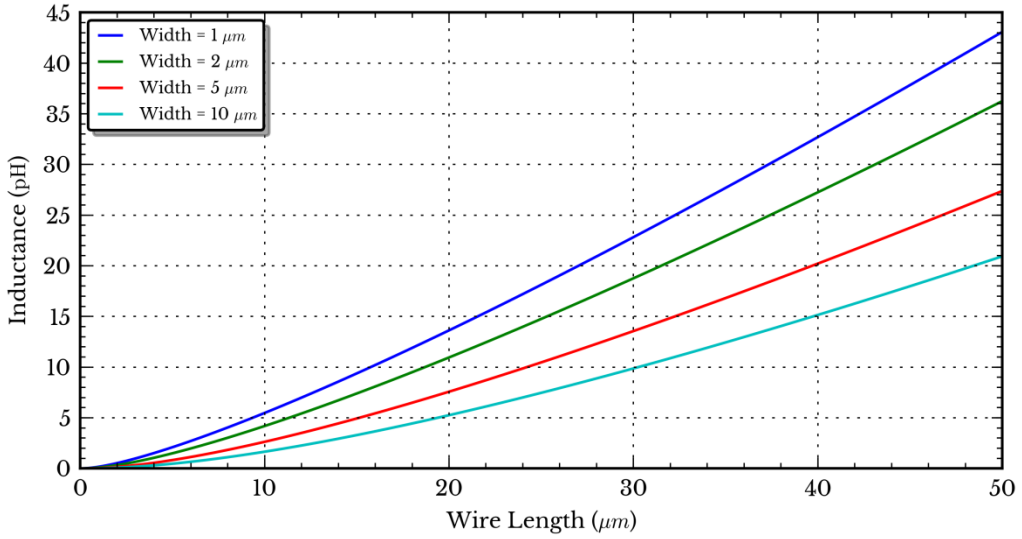


Figure 2.2: Self inductance of a single wire as a function of length. Multiple curves are shown which represent various wire widths as shown in equation 2.29.

The next most important case is two parallel wires, separated by a distance, d. For the same physical reasons as in equation 2.29, the equation is identical, but with $r \to d + r_w$ where r_w is the radius of the wire [16]. The mutual inductance of two wires is then equal to the self-inductance of a single wire of a larger radius, equation 2.31.

$$M = \frac{\mu_0}{2\pi} l \left[\ln\left(\frac{l}{d + r_w} + \sqrt{\left(\frac{l}{d + r_w}\right)^2 + 1} \right) - \sqrt{1 + \left(\frac{d + r_w}{l}\right)^2} + \frac{d + r_w}{l} \right] \quad 2.31$$

Similarly to equation 2.29, equation 2.31 simplifies if the length of the wires is larger than the radius of the wires and the distance between them. In many cases, the wire radius is much smaller than the separation of the wires. In the case that two small wires are parallel for a long distance, the mutual inductance of the two wires is reduced to equation 2.32.

$$L_{wire} = \frac{\mu_0 l}{2\pi} \left[\ln\left(\frac{2l}{d}\right) - 1 \right] \quad 2.32$$

2.5 Existing Inductor Types

2.5.1 About

Due to their utility in analog systems, discrete inductors are core components of many electronic systems. Discrete inductors often take the form of wire wrapped in a helix or a toroid and are still widely used today in power systems, such as power transformers. However, to mass-manufacture RF components in an inexpensive fashion, it is necessary to integrate inductors into integrated circuits that can be manufactured in a monolithic fashion. This integration has proven to be difficult, due to the challenges of adapting inductor designs to planar technologies.

In an effort to mitigate the poor performance of modern on-chip inductor designs, various technologies are being developed and demonstrated by researchers: active inductors, microelectromechanical system (MEMS) inductors, and nano-technology-based inductors (nano-inductors).

2.5.2 Helical Coils

In order to analyze the performance of on-chip inductors, it is helpful to understand the principles behind the discrete helical (or toroidal) coils that are used in low-frequency applications.

Helical coils (also called solenoids [20, p. 155]) are lengths of wire wrapped around a cylindrical object. Ideal helical coils are simple to analyze analytically and have the well-known result for inductance shown in equation 2.33, where L is the inductance of the coil, μ is the permeability of the material inside the coil, N is the number of turns (ie. number of times the wire wraps around the core material), A is the cross-sectional area of the coil and l is the length of the coil [9].

$$L = \frac{\mu N^2 A}{l} \qquad 2.33$$

Equation 2.33 is derived under the assumption that there is a single layer of wire wrapped around the core and that the spacing between the turns is small compared to both the radius of the helix as well as the length of the coil [9]. If these conditions are true, then the helix can be analyzed as a cylinder of current that produces a magnetic field inside the cylinder's radius and equation 2.33 is an exact result for the inductance. This well-known result can be used to design helical coils with a large inductance.

If the assumptions about the wire radius, packing and helix radius are not valid, then additional terms are added to equation 2.33. If the coil is a circular coil and it is short, then equation 2.33 must be multiplied by the Nagaoka constant [11].

$$K_n = \frac{1}{1 + 0.9\left(\frac{r}{l}\right) - 0.02\left(\frac{r}{l}\right)^2} \quad 2.34$$

Where r is the radius of the coil and l is the length of the coil. The Nagaoka constant reduces the predicted inductance of a short coil due to the increased importance of the fields at the end of the coil. The Nagaoka constant can also be modified to take into account the effect of multiple layers of wrappings of wire around the core. If the coil is a multi-layer coil then the Nagaoka constant becomes equation 2.35 [11].

$$K_n = \frac{1}{1 + 0.9\left(\frac{r}{l}\right) + 0.32\left(\frac{t}{r}\right) + 0.84\left(\frac{t}{l}\right)} \quad 2.35$$

Where t is the thickness of the winding and r is now the mean distance of the winding, and l remains the length of the coil.

The above equations assume that the coil is an ideal current sheet. If the coil turns are not spaced close together, then the helix can no longer be analyzed purely as a cylinder and an additional factor must be considered [11]. Equation 2.36 shows the scaling factor for a helix; this scaling factor is multiplied with equation 2.33 to produce the total inductance.

$$K_{helix} = \left(1 - \frac{l(A+B)}{\pi r N K_n}\right) \quad 2.36$$

Where,

$$A = 2.3\log_{10}\left(\frac{1.73d}{c}\right) \quad 2.37$$

$$B = 0.336\left(1 - \frac{2.5}{N} - \frac{3.8}{N^2}\right) \quad 2.38$$

Where N is the number of windings, d is the diameter of the conductor, and c is the winding pitch (turns per meter). Together, equations 2.33 and 2.36 allow for a first-order calculation of the inductance of a real helix.

2.5.3 Planar Inductors

Planar spiral inductors are perhaps the most common inductor used in the integrated circuit industry today [6]. In its basic form, a planar spiral inductor is a single-layer metal trace that forms a spiral shape. Typically, a secondary metal layer is used to connect the inside terminal of the spiral to the outside of the device [21]; however purely single-layer inductor designs do exist (eg. a single loop, or the spiral shown in Figure 1.1b). Planar spiral inductors are usually used because they are relatively simple to design and construct, however they occupy a large die area and they have low quality factors, often less than 10 [6].

Spiral inductors take a variety of shapes, including square, circular, and octagonal [6]. These designs can be further classified as symmetric and non-symmetric. Of the basic shapes (square, circular and octagonal), the circular spiral is known to have the highest quality factor; however, many design tools do not allow for curvi-linear shapes [22][23]. Figure 2.3 shows a two-turn asymmetric square inductor. This style of planar spiral inductor requires a trace on a second metal layer to connect the inner terminal to a location outside of the spiral so that it can be connected to other devices.

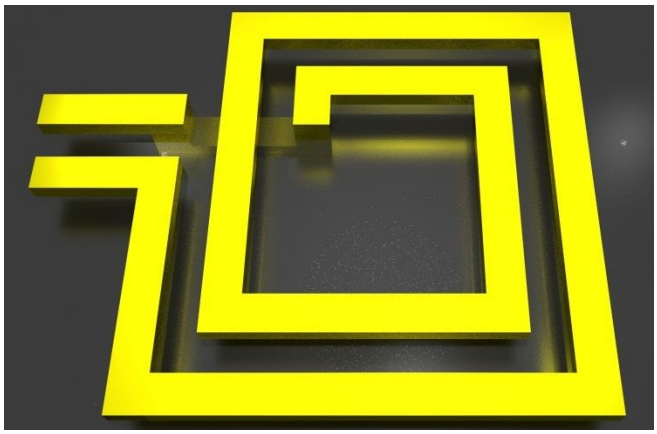


Figure 2.3: Two-turn square-spiral planar inductor. Note that the inner turn is connected to the outer terminal by a set of vias and a wire on a second layer.

Due to their use in microelectronic circuits, there are well-characterized design equations for planar spiral inductors. For a given square-spiral inductor, the approximate inductance is given by equation 2.39, where L is the inductance, μ_0 is the permeability of free space, n is the number of turns and r is the outer radius of the spiral [6].

$$L \approx \mu_0 n^2 r \qquad 2.39$$

When designing a planar spiral inductor, it is more typical to design for a specific inductance and solve for the number of turns needed. An approximate equation for the number of turns required for a given winding pitch (P in turns/meter) and inductance is given by equation 2.40 [6].

$$n \approx \left(\frac{PL}{\mu_0}\right)^{\frac{1}{3}} \qquad 2.40$$

Equation 2.40 is useful for many cases because the inductance is often set by circuit requirements and the possible pitches are determined by the fabrication process. The number of turns can then be estimated and then the radius can be calculated by equation 2.39. Since both of these equations are approximate, the resulting design should then be refined by more accurate equations or electromagnetic finite element simulations.

A more accurate approximation of the inductance value of a square planar spiral inductor is given by equation 2.41 [6], where r is the outer radius of the coil and a is the mean radius of the coil. This equation is more accurate than equation 2.39 and it can analyze inductors which have turns removed, ie. the center of the spiral is removed [6]. However, equation 2.41 requires the number of turns, the mean radius and the outer radius of the coil, which are three independent variables, making equations 2.39 and 2.40more suitable for initial designs, which can then be refined.

$$L \approx \frac{37.5\mu_0 n^2 a^2}{22r - 14a} \qquad 2.41$$

The inductance of planar inductors can also be calculated using Greenhouse's method [24]. Greenhouse's method is to decompose the inductor into its linear segments and then to calculate the self and mutual inductances of each of these segments and then sum them [25]. Greenhouse expresses this relationship with equation 2.42, where L_{total} is the total inductance, L_0 is the sum of the self-inductances of the linear segments and $\sum M$ is the sum of the mutual inductances of the linear components [24].

$$L_{total} = L_0 + \sum M \qquad 2.42$$

In addition to spiral inductors, there is another style of inductor called a meander inductor. A meander inductor structure is shown in Figure 2.4; instead of forming a spiral, the wire trace meanders back and forth, creating multiple 3/4–loops. The inductance of meander inductors can be calculated by calculating the self and mutual inductances of the segments and adding them together [25]. Meander inductors are simple to fabricate because they require only one metal layer [26]. Meander inductor designs can be scaled down with no change in the designs; however, this causes a linear decrease in the inductance and quality factor, in the case that all dimensions are scaled down linearly [26]. The maximum reported inductance per area of a meander inductor is 0.053 nH/micron [26].

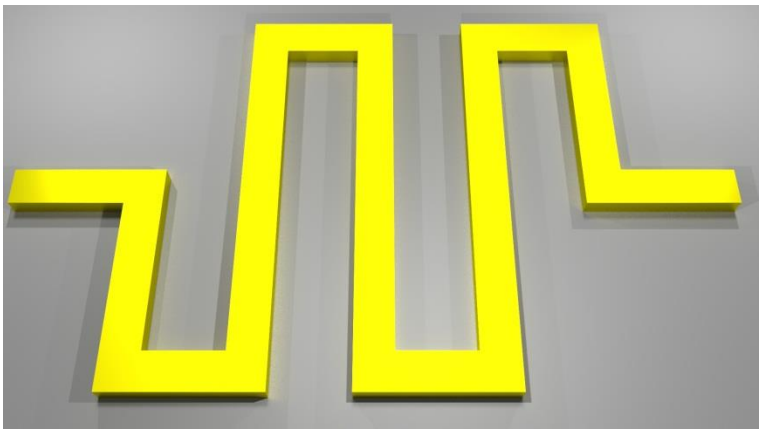


Figure 2.4: Two-turn meander inductor

Due to the prevalence of planar inductors for use in on-chip devices, a number of techniques have been developed to increase the quality factor. Most of these techniques involve changing the substrate to reduce losses. One technique for silicon substrates is to place PNP junctions directly under the planar inductors [27]. The PNP junctions block the paths of the eddy currents that would normally be present in a silicon substrate, which reduces the overall losses of the planar inductor and increases the quality factor. Another substrate alteration method is to etch the substrate away from under the inductor [28], or to build the inductor over a conductive ground shield that restricts the field from entering the silicon [29].

Other techniques to increase the quality factor include varying the metal trace widths to reduce skin effect losses [30], which can produce quality factors above 40 for a 20 nH inductor; however, this modification comes at a cost of increased area required.

2.5.4 Active Inductors

Active inductors are devices that mimic the impedance behaviour of passive (classical) inductors but are constructed out of active elements. These devices exhibit high quality factors near their design frequency and occupy a small area [31]. In addition, because these devices are built using CMOS devices, they require no additional process steps over the devices already being built.

Active inductors are an alternative to the use of lossy and low-quality factor integrated inductors, especially for devices that require high quality factor inductors, such as voltage controlled oscillators where they reduce phase noise [32]. Active inductors are constructed from active devices (transistors) to produce an inductive impedance [33]. Active inductors have high quality factors [34]; however, they inherit the undesirable characteristics of active devices: non-linearity, noise, and power consumption [3]. In addition, active inductors are sensitive to fabrication process

parameters, voltages and temperatures, all of which may affect the performance of active inductors [3].

The drawbacks to active inductors prevent them from being a catch-all solution to on-chip inductance. Active inductors always consume power, even when not in use and they only function as inductors within a narrower frequency band than passive inductors [35]. Active inductors are also only linear for certain biasing and signal input conditions, which must be accounted for during the design of the inductor since linearity is important for many RF circuits [36][37]. Last, some active inductor designs require planar inductors, which increases the area of the circuit [31].

Despite these drawbacks, active inductors have the highest quality factors of any integrated inductor device currently produced. This high quality factor makes the use of active inductors essential for some applications (VCOs).

The quality factor of active inductors is typically increased by using a negative resistance circuit [33].

2.5.5 MEMS Inductors

Microelectromechanical system-based (MEMS) inductors are passive inductors that utilize advanced fabrication techniques to allow the creation of 3D elements on a chip. MEMS inductor designs are typically microscopic re-creations of the solenoid structures used for discrete inductors [38].

These inductors have a high quality factor and usable inductance, similar to discrete inductors, but they typically take up less chip area than planar inductors because they are utilizing the more area-compact helix structure rather than the area-inefficient spiral structure. However, MEMS inductors have the drawback that they are relatively difficult to build. Typically a MEMS inductor will have more process steps than a spiral inductor and it may require process steps that are incompatible with the CMOS devices that are already present on the same chip. These difficulties are an active area of research that is applicable to the entire MEMS field.

Spiral inductors implemented on high resistivity silicon on insulator wafers (HRSOI) show improved characteristics, including quality factors as high as 16 for a 2.46 nH planar spiral inductor [39].

2.6 New materials for inductors

2.6.1 Nanotechnology and inductors

The inductor designs (planar, active, and MEMS) in the previous sections all have substantial drawbacks that prevent widespread adoption of inductors for on-chip systems. In recent years,

there have been increasing efforts to utilize nanotechnology to produce inductive devices of acceptable performance and fabrication characteristics. Nanotechnology-based inductors utilize new structures and materials to produce inductive behaviour with high-quality factors and high inductances.

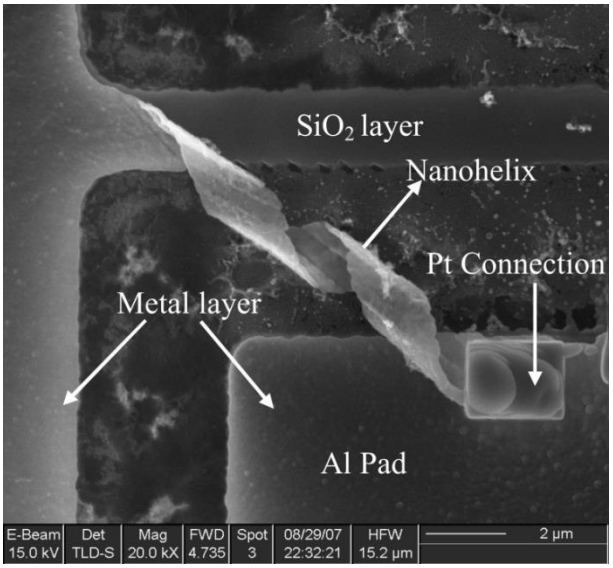


Figure 2.5: Stressed thin-film inductor © 2008 IEEE, reproduced from [38]. The original figure text: SEM image of a suspended two-turn nanohelix aluminum inductor fabricated using FIB-SIT. The inductor with an air-core is 2 µm higher [sic] above [the] silicon substrate and is isolated from the substrate through a silicon dioxide layer between the metal layer and the substrate.

One example of these kinds of inductors is carbon nanotube (CNT) devices [40]. Other examples include stress-induced coiling of thin films into helices [38], bio-templating of helices using plants [41] and graphene-based inductor traces [42].

Table 1 shows the published performance results from a wide variety of inductor types, ranging from novel inductor designs to

Table 1: Comparison of performance of existing inductor devices.

Type	**Inductance (nH)**	**Area (um^2)**	**Inductance/Area ($nH \cdot \mu m^{-2}$)**	**Quality Factor**	**Self-Resonance Frequency**
Meander [26]	0.003	0.056	0.053	0.004	--
Planar spiral [39]	2.46	--	--	16.3	17.2 GHz
Planar spiral [39]	10.2	--	--	8.59	5.8 GHz
Planar spiral [43]	7.15	6.97×10^6	1.03×10^{-6}	33.5	2.33 GHz

Planar spiral [43, p. -]	20	22.7×10^6	8.8×10^{-7}	22.7	0.71 GHz
Planar, magnetic core [28]	--	--	0.3	0.25	--
Stacked Loop [44]	0.42	441	9.5×10^{-4}	17	50 GHz
Stacked Loop [45]	4.8	3421	0.0014	11	20 GHz
Active (26 mW power consumed) [31]	22	10^6	2.2×10^{-5}	45	--
Bio-template helix [41]	0.061	8.3×10^5	7.3×10^{-8}	--	--
Stress-formed helix [38]	28	20	1.4	1.5	350 MHz
Single MWCNT [40]	0.67	20	0.034	168	> 1 THz
SOI Planar spiral [46]	3.4	$\approx 10^5$	3.4×10^{-5}	15.5	8.6 GHz
Ferrite Solenoid [47, p. -]	1.4	90×10^3	1.6×10^{-6}	--	$\approx$ 20 GHz
Active (369 mW power consumed) [34]	26	630×10^3	4.1×10^{-5}	3400	2.2 GHz
Planar spiral [30]	20	$\approx 10^6$	2×10^{-5}	44	8.5 GHz

2.6.2 Nanostructured thin films

Nanostructured thin films are thin material films that have a nano-scale sub structure. Nano-scale structures can be created on a wafer scale through the use of advanced deposition techniques, such as glancing angle deposition (GLAD).

GLAD is an altered physical vapor deposition technique in which the substrate is tilted so that the substrate normal is at a very large angle relative to the incoming material flux. The large angle of incidence creates a shadowing effect that causes the final film structure to be anisotropic [48]. Changing the deposition angle produces varying densities of structures [48]. The GLAD technique also uses the rotation of the substrate to control the exact shape of the structures that are produced. If the substrate is rotated at intervals, then the film will consist of polyhedron structures; if the substrate is rotated continuously then helices are grown; and if the substrate is rotated quickly (1-2 rpm [49]) then vertical posts are grown [50]. Since GLAD uses physical vapour deposition, the GLAD technique can be applied to any material that can be deposited using physical vapor deposition techniques [51].

Figure 2.6 shows a conceptual diagram for a helix array grown by the GLAD process. GLAD can produce the regular array shown in Figure 2.6 by pre-processing the substrate so that it has a pattern before deposition [49]. Normally, the GLAD process produces structures that are evenly distributed but randomly placed [52].

An example of a GLAD deposition setup is shown in Figure 2.7 (sputtering). The substrate is held at a large angle relative to the flux source (visible as a plasma in the image). The substrate is rotated during the deposition process to produce the desired nano-scale structure.

Typically, GLAD films have high porosity and high surface area [51] which makes them useful for applications like humidity sensing [53] and photovoltaic cells [51]. The nanostructure of GLAD films results in a bulk anisotropic conductivity, especially at deposition flux angles greater than 60°, relative to the deposition source [54].

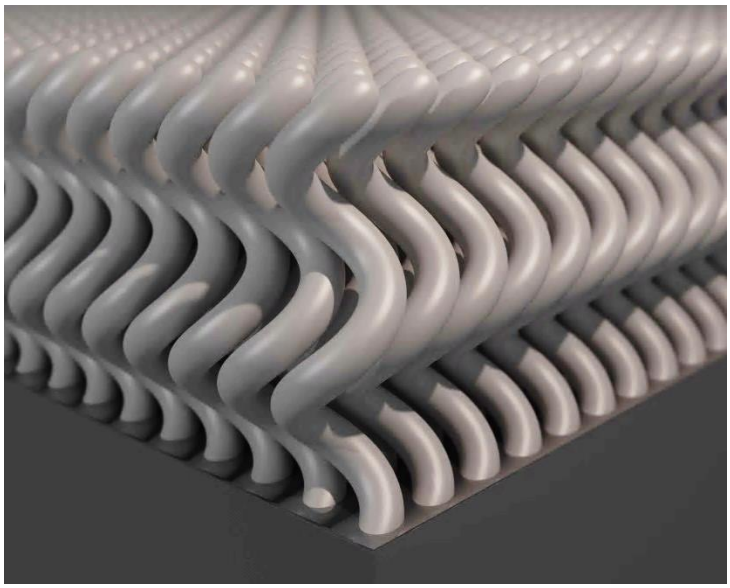


Figure 2.6: Conceptual diagram of the cross section of a helical GLAD film.

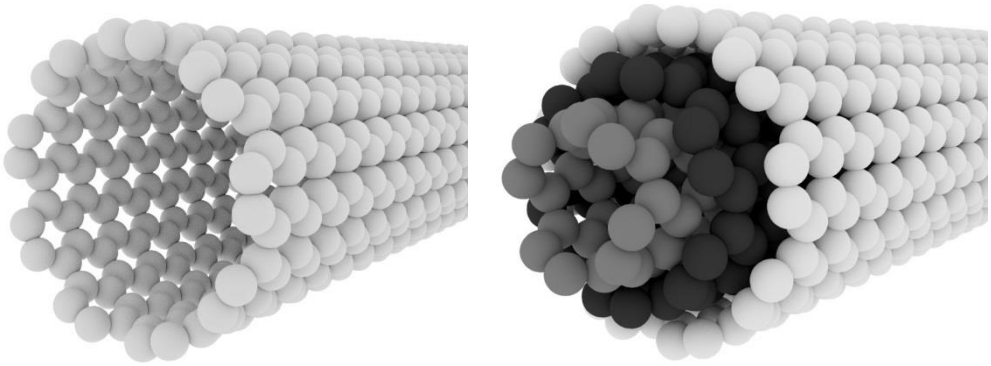
Figure 2.7: Set-up to perform glancing angle deposition with a sputtering system.

Structures that have been grown with the GLAD technique can have a continuous (regular) film deposited on top of them, called capping the film [55].

Etching GLAD films can be made difficult by the large capillary forces induced by the nanostructure of the GLAD film [56].

2.6.3 Carbon nanotubes

Carbon nanotubes (CNTs) are single-molecule objects of incredibly large size. The structure of a CNT is a graphene sheet (single layer of carbon atoms) rolled into a cylindrical shape, such as the ones shown in Figure 2.8 [57]. Carbon nanotubes have two general structures: single-wall carbon nanotubes and multi-wall carbon nanotubes. The single wall carbon nanotubes (SWCNTs) consist of a single cylinder of carbon atoms, as shown in Figure 2.8a. The cylinder ends are capped by hemispheres of carbon atoms, similar to buckminsterfullerenes. Multi-wall carbon nanotubes (MWCNTS) are similar to SWCNTs; however they have multiple tubes arranged in a coaxial configuration, as shown in Figure 2.8b.



(a) (b)

Figure 2.8: The structure of a carbon nanotube (ends not shown). On the left (a) is a single-wall carbon nanotube that consists of a single tube of carbon atoms. On the right (b) is a multi-wall carbon nanotube which consists of concentric rings of carbon atoms. The spheres in the multi-wall carbon nanotube are all carbon and are shaded to show how each tube is positioned in relation to the other tubes.

CNTs have a number of unique properties: they exhibit behaviour of a 1-dimensional object and they can either be metallic or semiconducting, depending on the orientation of its atomic lattice [57]. Their semiconducting behaviour has made them interesting materials for potential use as transistor devices [58], while their metallic behaviour has made them interesting for use as interconnects and inductors [59]. This section will discuss CNT properties with respect to creating inductor devices.

Figure 2.9 shows a lumped-element model for a single-wall carbon nanotube including all of the important physical effects in the CNT. The two most important qualities of carbon nanotubes with respect to inductor applications are their overall resistance and their overall inductance.

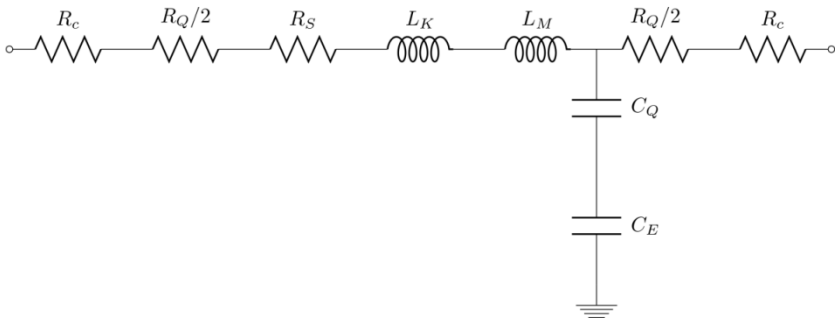


Figure 2.9: Circuit model for a short, single-wall carbon nanotube [60]. R_c is the contact resistance, R_Q is the quantum resistance, R_S is the scattering (ohmic-like) resistance, L_K is the kinetic inductance, L_M is the magnetic inductance, C_Q is the quantum capacitance, and C_E is the electrostatic capacitance of a CNT to ground.

There are a number of sources of resistance in a carbon nanotube: quantum scattering resistance, contact resistance, and ohmic resistance [61]. Despite the quantum mechanical contribution to CNT resistance, CNTs have a very low bulk resistivity, of approximately 10^{-7} Ωm mainly due to their small size. However, CNT contact resistance is typically very high, on the order of kilo-ohms, which is in addition to the quantum resistance [57]. The quantum resistance is a purely quantum mechanical consequence of inserting an electron into the conduction band of a carbon nanotube; For a single-wall carbon nanotube, it is calculated to be approximately 6 kΩ [62]. The quantum resistance of each conducting channel is given by equation 2.43[40].

$$R_Q = \frac{h}{4e^2} = 6.45\ \text{k}\Omega \tag{2.43}$$

The distributed scattering resistance per unit length is given by equation 2.44 [40].

$$R_S = \frac{h}{4e^2}\frac{1}{\lambda_{CNT}} \tag{2.44}$$

Where λ_{CNT} is the mean free path of an electron in the CNT, which can be approximated by equation 2.45.

$$\lambda_{CNT} \approx 1000D \tag{2.45}$$

Carbon nanotubes have a distributed inductance that arises from the kinetic energy of an electron in a 1-dimensional system, this is called kinetic inductance. The kinetic inductance is caused by quantum mechanical considerations of a 1-dimensional system [63] and is given by equation 2.46.

$$\mathcal{L}_K = \frac{h}{2e^2 v_F} \tag{2.46}$$

Where $\mathcal{L}_K$ is the kinetic inductance, h is Planck's constant, e is the electron charge, and v_F is the Fermi velocity in a CNT. The Fermi velocity is approximately $v_F = 8 \times 10^5$ m/s, resulting in a kinetic inductance of $\mathcal{L}_K = 16\ \text{nH}/\mu\text{m}$ for a single electron spin [63], since metallic CNTs have two conducting channels, the kinetic inductance is therefore $L_K = \frac{h}{4e^2 v_F} = 8\ \text{nH}/\mu\text{m}$. This result dwarfs the magnetic inductance for the same SWCNT, $\mathcal{L}_M \approx 1\ \text{pH}/\mu\text{m}$ [63], making the inductance of a carbon nanotube almost entirely due to the quantum-mechanical properties the tube. The derivation of the above relations and values did not depend on any particular material properties that are unique to carbon nanotubes and so it is a general result that the inductance of a1-dimensional nano-scale object is always mainly due to the kinetic inductance and not the magnetic inductance [63].

Experimental measurements of the impedance of single-wall CNTs (SWNTs) show impedance values that are approaching the inductance and impedance predictions above [64]. The

experimental upper limit for the resistance per length of a carbon nanotube is $10\ \mathrm{k\Omega/\mu m}$ and experimental evidence suggests that the resistance per unit length of a carbon nanotube is a significant portion of the overall resistance [65].

Assuming a series model for the carbon nanotube, the quality factor for a single SWCNT is calculated by equation 2.47, where ω is the angular frequency, l is the carbon nanotube length, $\mathcal{L}_K$ is the kinetic inductance, L_M is the magnetic inductance, $R_{contact}$ is the contact resistance, and R_S is the scattering resistance distributed along the carbon nanotube length. The capacitance of the CNT is not a significant effect because it is incredibly small (approximately $193\ \mathrm{aF/\mu m}$) [40].

$$Q = \frac{\Im(Z)}{\Re(Z)} = \frac{\omega l \mathcal{L}_K + \omega L_M}{2R_{contact} + R_Q + lR_S} \tag{2.47}$$

For a $20\ \mu\mathrm{m}$ long SWCNT with a diameter of 2 nm (and no contact resistance) the circuit parameters are:

$$R_Q = 6.4\ \mathrm{k\Omega}$$

$$lR_S = 64\ \mathrm{k\Omega}$$

$$L_M = 35.6\ \mathrm{pH}$$

$$lL_K = 160\ \mathrm{nH}$$

Using the above parameters, at 60 GHz the quality factor for this CNT is only 0.94. Therefore, the quality factor of a single SWCNT is small, despite the high inductance.

Chapter 3: **Nanostructured thin films as inductors**

3.1 Nano-scale structures

3.1.1 Introduction

This chapter will introduce the concepts of vertically-aligned nanostructured thin films for use as on-chip inductors. First, the materials that are the inspiration for this work will be presented followed by comprehensive simulations that begin with a single nanostructure and end with large-scale models for predicting inductor performance.

3.1.2 Nano-scale wires and helices

Nano-structured materials are a new class of materials that have unique properties that differ from the bulk form of the material. The properties of nano-structured materials allow unique solutions to the problem of creating high quality and small on-chip inductors. Examples of the use of nano-scale materials to solve engineering problems are becoming common in the literature. One of the advantages of nano-structured materials is their ability to achieve complex, three-dimensional shapes in small volumes and areas.

One important class of nano-structured materials is nanostructured films (NFs). NFs can be made out of a variety of materials [66] and by using a variety of techniques [67]. It is possible to use NFs to create nano-scale helices, which are candidates for use as integrated, on-chip inductors.

There are numerous examples of NSH in the literature, such as the stressed-film helix shown in Figure 2.5, the coiled carbon nanotubes shown in Figure 3.1 and nanostructured metallic thin films [68]. For this work, materials and structures that had already been experimentally demonstrated in the literature were investigated for potential as inductors. Figure 3.2 shows two examples of metallic nano-scale helix structures reported in the literature [69]. These structures are closely packed to form a film and have heights of approximately 1 μm.

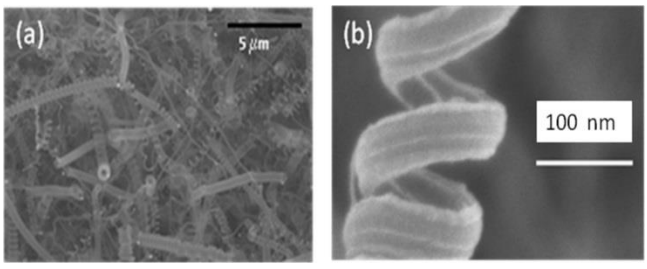
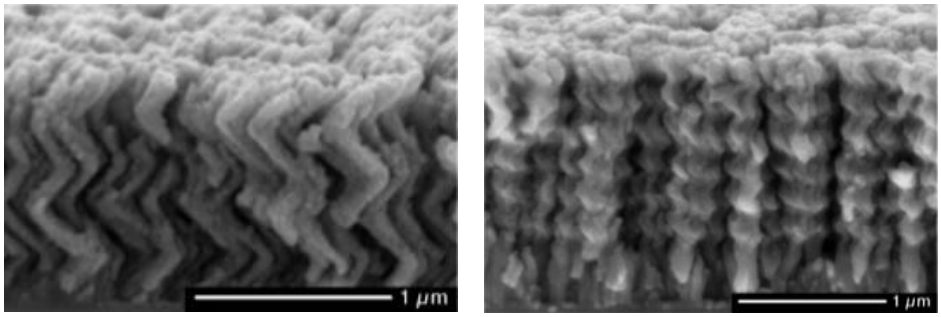


Figure 3.1: Image © IEEE 2010, reproduced from [70]. Original image caption: (a) SEM image for coiled CNWs [sic] with a (b) more detailed view. No preferred alignment was observed.

The two structures shown in Figure 3.2 were analyzed to determine if nano-scale helices are suitable for developing integrated on-chip inductors. To study the properties of nano-helix structures, representative values for the heights, line width, and helix width were found from the images in Figure 3.2. These measurements were then used to create simulation models for analysis. The models for the helices were generated and simulated using ANSYS High Frequency Structural Simulator (HFSS). The measured parameters for the helices shown in Figure 3.2 are tabulated in Table 3.1.



(a) (b)

Figure 3.2: Nano-scale helix structures fabricated using physical vapour deposition from [69]. Both (a) and (b) were modeled as part of this work. In this work, (a) is called a wide helix and (b) is called a narrow helix.

Table 3.1: Physical parameters for the helices shown in Figure 3.2.

Property	Wide Helix	Narrow Helix
Helix radius	82.15 nm	76.9 nm
Helix pitch	457 nm	270 nm
Wire radius	35.71 nm	51.3 nm
Wire length	2.068 μm	3.321 μm
Number of turns	3	6
Analytical helix inductance	3.11×10^{-13} H	6.32×10^{-13} H
Analytical wire inductance	1.28×10^{-12} H	1.79×10^{-12} H
Cross-section polygons	10	10
Sections per turn	20	20

The values shown in Table 3.1 were measured from the bitmap images in [69] using the GNU Image Manipulation Program (GIMP) measuring tool. The lengths were estimated by counting the

lengths (in pixels) with GIMP and then converting the lengths in pixels to physical lengths using the scale bars in the image.

3.1.3 Simulation methodology

The performance of nano-scale helices at microwave frequencies was studied with ANSYS High Frequency Structural Simulator (HFSS). HFSS is a 3D full-wave finite element simulator which can do frequency-domain electromagnetic simulations of structures to obtain the S-parameters . The S-parameters were internally processed into Z-parameters by HFSS, which were then be used to calculate the important quantities of passive inductor structures: inductance, resistance and quality factor.

The Z-parameter for a 1-port device is a single number that represents the input impedance of the port [8]. The impedance is a complex number of the form given in equation 3.1, where Z is the impedance, R is the resistance and X is the reactance.

$$Z = R + jX \tag{3.1}$$

For an inductor, the reactance takes the form of equation 3.2, where j is the imaginary number, ω is the angular frequency and L is the inductance.

$$X = j\omega L \tag{3.2}$$

Re-arranging equation 3.2 directly gives the inductance in terms of the impedance in equation 3.3.

$$L = \frac{\Im(Z)}{\omega} = \frac{X}{2\pi f} \tag{3.3}$$

Finally, the quality factor is defined as shown in equation 3.4, where Q is the quality factor, $\Im\{Z\}$ is the imaginary part of the impedance and $\Re\{Z\}$ is the real part of the impedance.

$$Q = \frac{\Im(Z)}{\Re(Z)} = \frac{\omega L}{R} \tag{3.4}$$

A single-wire simulation models are shown in Figure 3.3. Figure 3.3a shows the model of the wide helix and Figure 3.3b shows the model of the narrow helix. In addition to the helix itself, the models consist of a connecting wire on the top and the bottom of the structure. These wires connect the helix structures to wave ports. The top wire is the positive terminal and the bottom wire is the ground connection.

The wave port is a boundary condition that acts as a semi-infinite waveguide with a phasor output. The polarization vector of the electric field is specified by the user. For the helix simulations, the polarization vector was always chosen from the top wire to the bottom wire. The resulting electric field at the port is shown in Figure 3.4.

All boundary elements of the simulation space have a radiation boundary applied, which is an absorbing boundary condition that does not reflect outgoing waves. This choice of boundary condition is equivalent to placing the inductor in an empty space that is fed by a semi-infinite waveguide.

Most inductor parameters were simulated over a range of frequencies. These simulations used *discrete* sweeps, which means that each simulation point in the frequency range was explicitly solved by the simulator. This solution method was preferred over the *interpolated* sweep because the interpolated sweep was found to give unstable (widely varying) results when large frequency ranges were simulated, which was not observed with discrete sweeps. Since each frequency point was explicitly solved for, there was an additional time cost over the interpolated sweep, however, the results were more accurate. For the curves presented throughout this document, the data is linearly interpolated between frequency points. Typically for these simulations, the frequency resolution was between 1 GHz and 0.1 GHz.

3.1.4 Devices studied

To analyze the suitability of nano-structured thin films as inductors it was necessary to study the structure on multiple scales: individual device, device array, and film approximation. Due to the nature of the nano-structure of the film, it was not possible to accurately model an entire film using the computing resources that were available.

The individual structures were studied first to analyze the performance behaviour of the film with respect to the materials used and the nano-scale structure. Next, arrays of the inductor structures were used to analyze the scaling behaviour of the films. Finally homogeneous anisotropic films were analyzed to determine the performance of a full structure.

3.2 Single Helix

3.2.1 Helices as inductors

A helix is defined using the parameters of height (h), pitch (p), number of turns (n), as defined in Appendix B. The single helix is the physical structure used in helical inductors, which are successfully used as discrete inductors. Using the advanced fabrication technologies introduced above, it is possible to fabricate helices which are integrated into a microelectronic system.

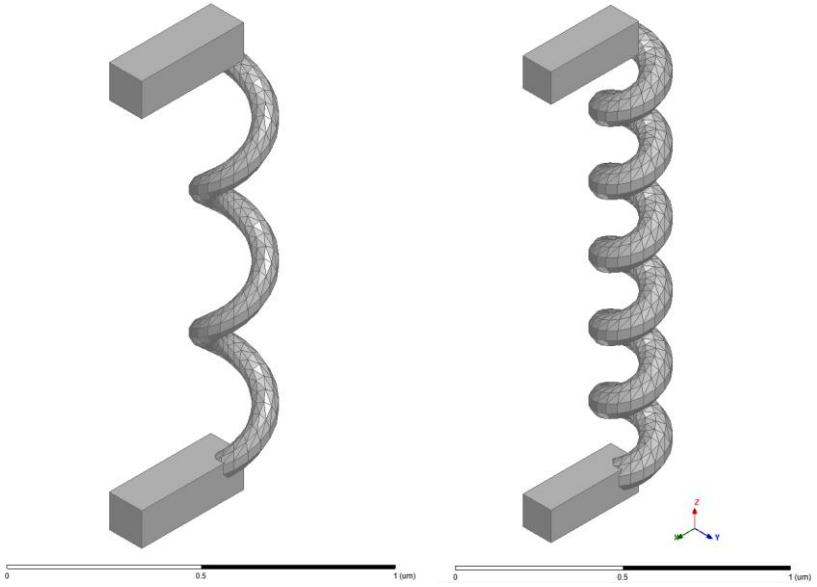
Integrated helices have much lower aspect ratios than the helices used to create solenoid inductors. To characterize the performance of integrated helices, their performance was compared to an equal length of wire. The length of wire in a helix is given by equation 3.5. This equation is derived in Appendix B.

$$l_{wire} = h\sqrt{(2\pi RT)^2 + 1} \quad 3.5$$

3.2.2 Single helix electromagnetic simulations

The helices shown in Figure 3.2 were studied for potential as inductors because they were examples of devices that had been previously fabricated in the lab [69]. The two helix shapes, called the wide inductor (Figure 3.2a) and the narrow inductor (Figure 3.2b) were modeled in HFSS as shown in Figure 3.3a and Figure 3.3b, respectively.

In addition to the physical characteristics of the individual helices, the packing of the two structures is different. The wide helix in Figure 3.2a intertwines with the surrounding helices. The narrow helix in Figure 3.2b and can be seen to be largely separate from the surrounding helices (although still densely packed).



(a) (b)

Figure 3.3: Models of single helices in free space. (a) Model of an individual element from the film shown in Figure 3.2a. (b) Model of an individual element from the film shown in Figure 3.2b

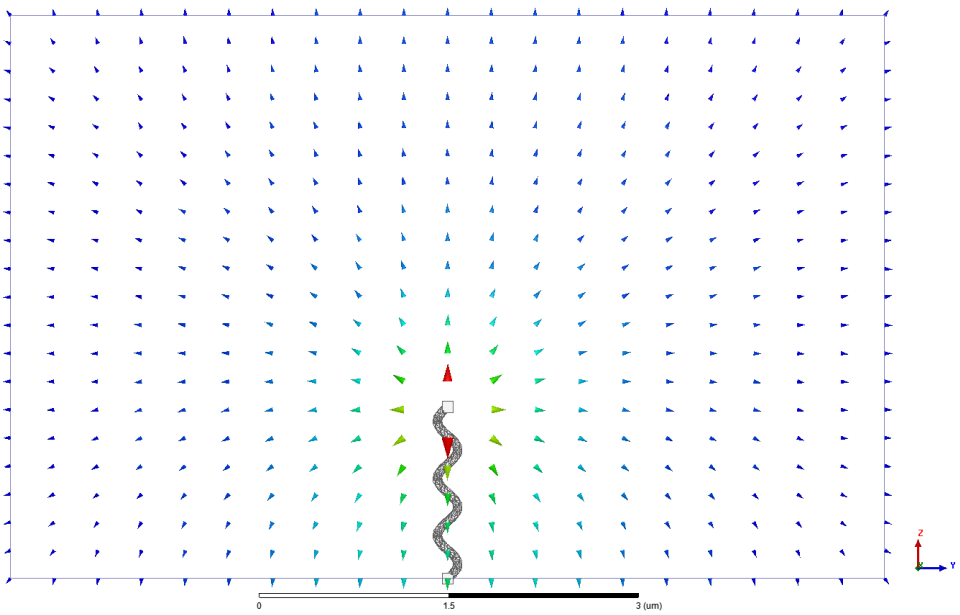


Figure 3.4: Wave port excitation in relation to the inductor model. The colored arrows show the electric field solution in the wave port plane.

Besides the nanostructure model, the simulation environment also can affect the simulation. The simulation space for the inductor models consisted of a cube that defined the simulation are that had a radiation boundary condition. The cube was roughly centered around the coordinate system origin, but shifted upwards (in the z-direction) by one micron to increase the port area. A wave-port excitation was applied to the upper portion of one face of the cube. The wave port is shown in Figure 3.4 as the large blue rectangle outline. The inductor has one terminal connected to the outer edge of the wave port, which acts as a ground terminal; the other terminal is connected to the interior of the port as a signal terminal.

The source electric field resulting from these terminal connections can be seen by the colored arrows in Figure 3.4; blue represents a low field strength, green to yellow is a medium field strength and a red represents the highest field strength. The arrow directions indicate the direction of the electric field. The field is strongest along the helix structure which indicates that the excitation wave is terminating across the structure.

3.2.3 Inductor material effects

There are a wide variety of materials that could potentially be used as nano-inductor structures. In macro-scale helix structures, the quality factor is dependent on the resistance of the coil wire, the losses in the core material as well as the magnetic permeability of the core material [71]. Similarly, in nanoscale structures there are a wide variety of potential materials that may be used.

A variety of materials were simulated as the wire material to determine the main factors in determining a high inductance and quality factor. The material parameters that were considered in choosing these materials were the conductivity, the magnetic permeability and the simplicity of fabrication (as defined by availability in the University of Alberta's NanoFab). To cover a range of these parameters, the following materials were simulated: aluminum, cobalt, copper, gold, iron, nickel and perfect electric conductor (PEC).

These materials all have high conductivities, which was expected to produce the best quality factors. In addition, cobalt, nickel and iron also have a high magnetic permeability, meaning that they react strongly to magnetic fields [2].

Both the wide and narrow helix structures were simulated with the magnetic and non magnetic materials. The simulated results for the two structures were very similar, as explained below.

Figure 3.5 shows the inductance of the wide helix as calculated from the impedance by equation 3.3. Figure 3.5 indicates that the magnetic metals have inductances that are orders of magnitude higher than the non-magnetic metals. The materials that produced the highest inductances were the three elemental magnetic metals: cobalt ($\mu_r = 250$), nickel ($\mu_r = 600$) and iron ($\mu_r = 4000$). The inductances produced by the magnetic metals range from 0.02 to 0.2 nH which is useful for millimetre-wave frequencies (30 GHz to 300 GHz). This value of inductance is over an extremely small chip area of $0.043\ \mu m^2$, giving an inductance per area of $0.46\ nH/\mu m^2$ to $4.6\ nH/\mu m^2$, which is extremely large compared to previously reported inductors shown in Table 1.

Figure 3.5 also shows that the inductance of the non-magnetic materials is only weakly dependent on material above 20 GHz and completely independent of material above 50 GHz.

Interestingly, Figure 3.5 also shows that the inductance for these structures is essentially constant over the frequency range (1 GHz to 100 GHz). This indicates that the self-resonance frequency is much higher than 100 GHz. This means that these inductors are suitable for ultra-broad-band applications.

Figure 3.6 shows the quality factor for the wide inductor. Similar to the inductance results shown in Figure 3.5, the magnetic materials all show enhanced performance over the non-magnetic materials, especially at high frequencies. The highest quality factor is observed in iron, despite the fact that it has a lower resistance than nickel. The absolute value of the quality factor for these devices is relatively low compared to other inductor technologies as shown in Table 1.

All of the materials shown in Figure 3.6 exhibit a linear quality factor at low frequencies because the structure is significantly smaller than the skin depth. This means that the current is

approximately uniform across the interior of the conducting wire and the quasi-static approximation holds that the resistance is constant. For most of the materials in Figure 3.6, the skin depth remains larger than the wire width; however, iron experiences a saturation of quality factor above 60 GHz. This is due to the reduced skin depth of iron due to its high permeability.

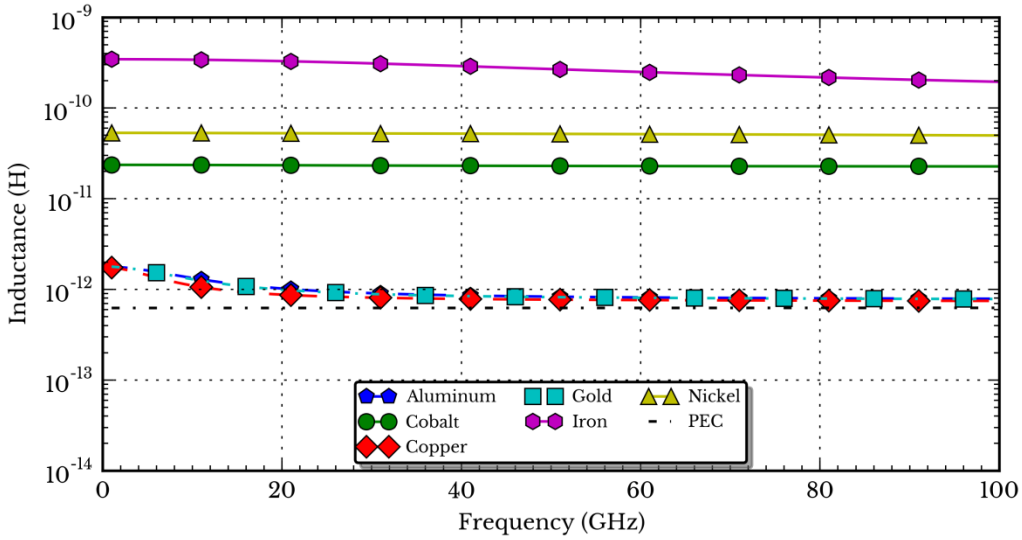


Figure 3.5: Inductance of the single wire shown in Figure 3.3 in free space.

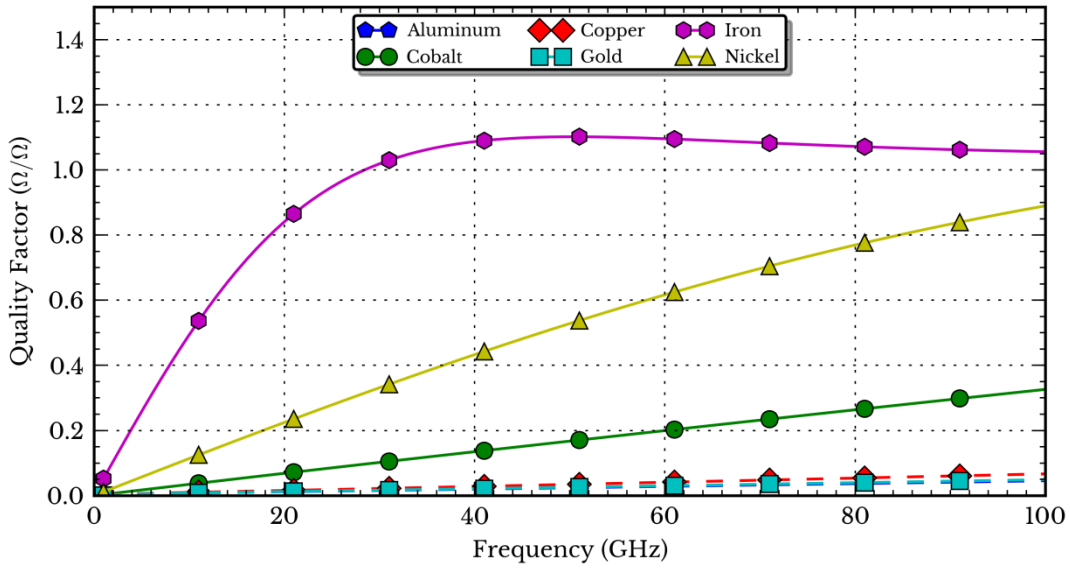


Figure 3.6: Quality factor of a single wire shown in Figure 3.3 in free space

The behaviour of the inductor with respect to the skin effect can be approximated by the planar skin depth (skin depth on a plane interface). The formula for skin depth is given by equation 3.6, where δ is the skin depth, ω is the angular frequency, σ is the conductivity, and μ is the permeability of the material [8]. The value used by HFSS for σ is 10.3×10^6 S/m and for μ it is $4000\mu_0$.

$$\delta = \sqrt{\frac{2}{\omega\sigma\mu}} \tag{3.6}$$

As a rough estimate, the skin effect becomes significant when the skin depth is equal to the radius of the wire (≈ 35 nm). Solving equation 3.6 for the frequency gives equation 3.7. When the material parameters for iron and the radius of the wire are used in equation 3.7, the resulting frequency is 4.8 GHz.

$$f = \frac{1}{\pi\mu\sigma\delta^2} \tag{3.7}$$

To verify this approximation of the skin depth effect, the resistance of the structure is shown Figure 3.7. For most of the materials shown in Figure 3.7, the resistance is essentially constant, which is predicted by the skin effect. For example, the frequency that the skin depth equals the structure radius for gold is 4.8 THz, which is much higher than the frequencies of interest. However, the resistance of the iron increases rapidly, which is predicted by the skin effect. The reduction in current penetration at high frequencies also reduces the overall inductance, as seen in Figure 3.6. Figure 3.7 also indicates that the resistance of nickel is increasing; this is also due to the skin effect, because the skin depth reaches the wire radius at approximately 23 GHz.

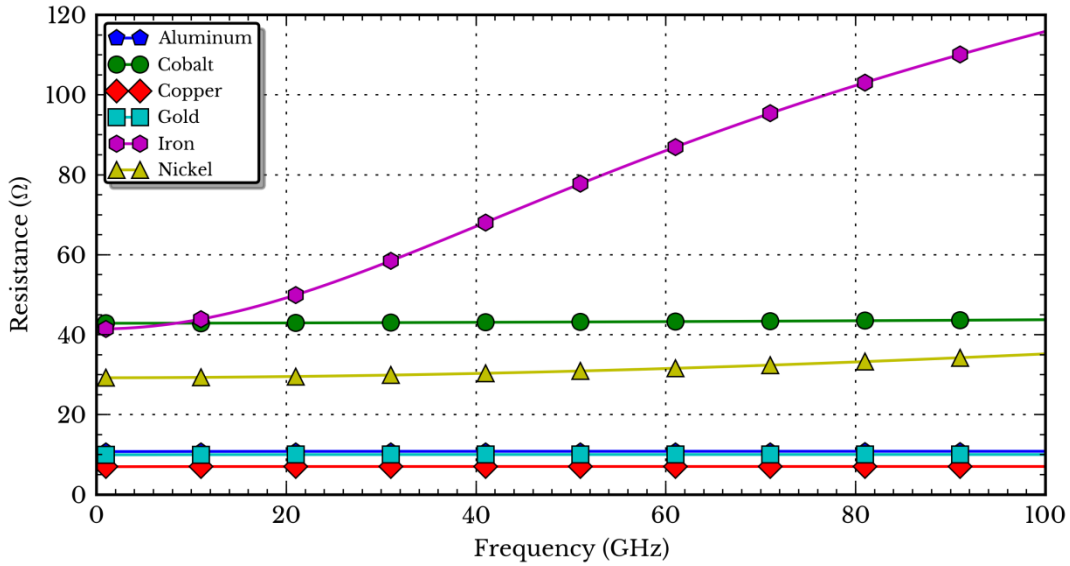


Figure 3.7: Resistance of a single wire shown in Figure 3.3 in free space.

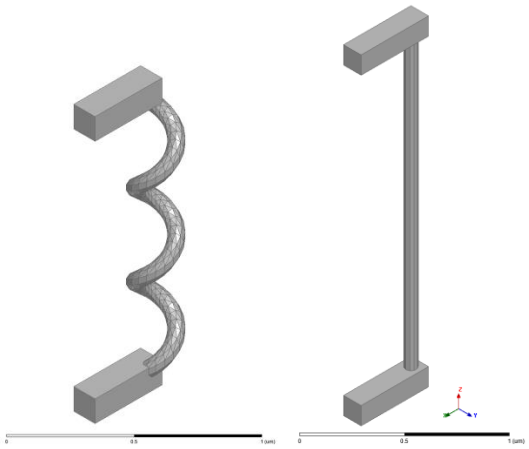
3.2.4 Comparison of helix structures

Section 3.2.3 demonstrated that for a single inductor structure, using a magnetic material produced the best inductance and quality factor; however, there is potentially a wide variation of inductor performance with respect to the exact helix shape.

Particularly, it is important to know how much inductance is gained by using a helix structure, compared to a linear wire structure. To compare these two cases directly, it is necessary to know the exact length of the helix wire. The wire length of a helical coil is given by equation 3.5. For the wide inductor, $R = 82.15$ nm, $T = 2.2$ Turns/μm, giving a total wire length of 2.068 μm.

The HFSS model for this linear wire is shown in Figure 3.8. The wire model was simulated using the same simulation environment as shows a linear wire that has a length equivalent to the wire

length of the helix in Figure 3.3a. This model is located at the same distance from the port as the helix.



(a) (b)

Figure 3.8: (a) Helix model shown in Figure 3.3a next to (b) its post inductor of equivalent length and wire width.

Figure 3.9 shows the simulated wire inductance compared with the simulated helix inductance for gold, iron and nickel structures. For the magnetic materials (iron and nickel), the inductance of the wire and the helix are very closely matched. For gold, the helix structure has an advantage over the wire structure until about 20 GHz, after which the wire exhibits a slightly higher inductance than the helix.

The results in Figure 3.9 indicate that the material parameters have a large effect on the inductance of the nanostructure whereas the physical structure only plays a significant role on the device performance in the case that non-magnetic materials are used.

Figure 3.10 shows the quality factor for the results shown in Figure 3.9. Similar to the inductance results, the quality factor does not significantly change with the change in structure. This indicates that if a magnetic material is used then the film may be fabricated in any way that produces the desired nanostructure length to produce the desired inductance.

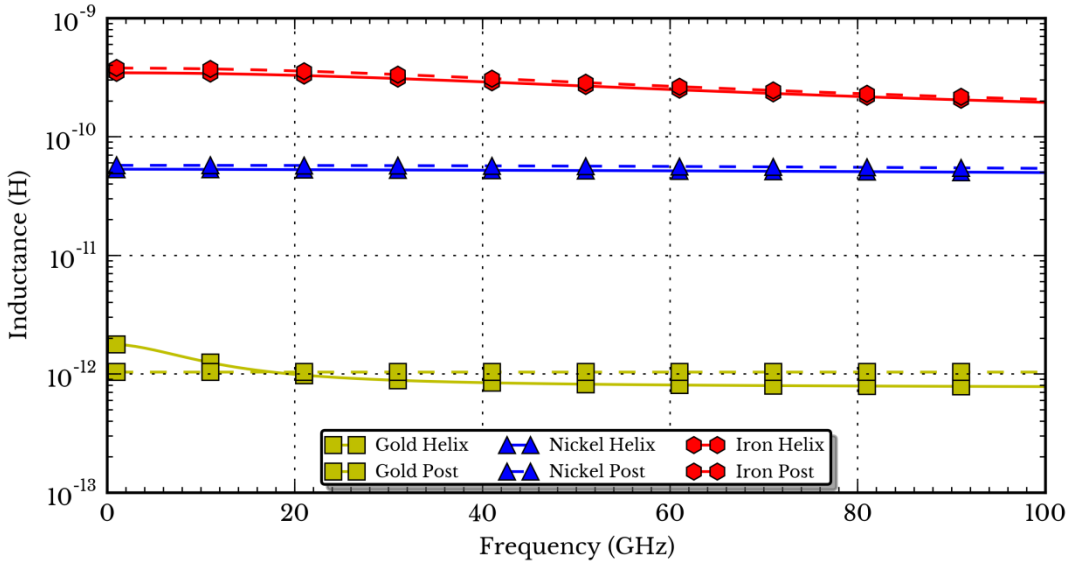


Figure 3.9: Comparison of the inductance of the wide helix and the equivalent linear wire.

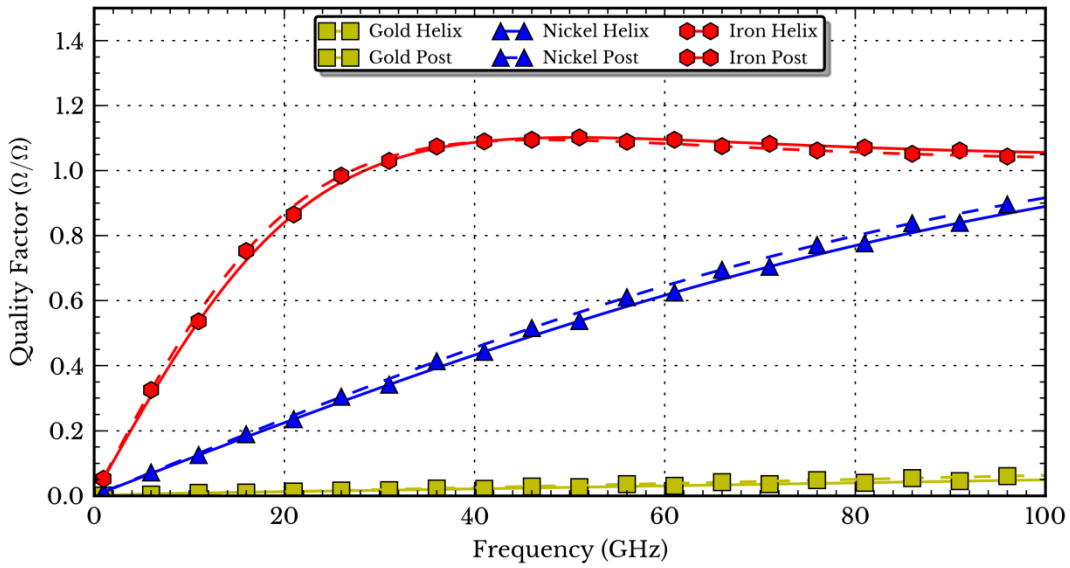


Figure 3.10: Comparison of the quality factor of the wide helix and the equivalent wire.

The performance of the narrow helix was similar to the wide helix. Figure 3.11 shows the inductance of the narrow helix, wide helix, and the equivalent posts together on one plot. The narrow helix has a higher inductance than the wide helix for each of the materials, however the difference is reduced at high frequencies. The increased inductance of the narrow helix is expected since it has a longer wire length than the wide helix.

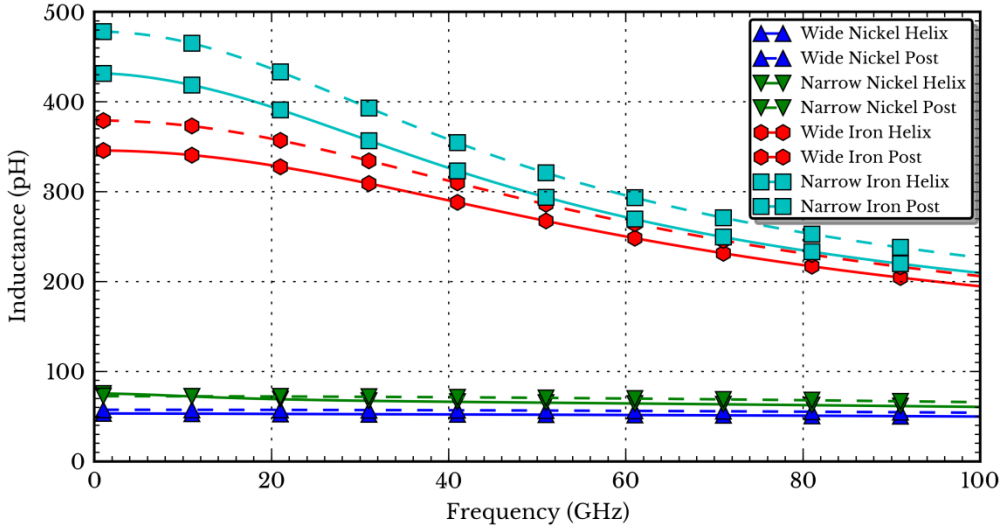


Figure 3.11: Comparison of the inductance of the wide and narrow helix made of iron and nickel. Also shown are the inductances of the equivalent post inductors for both the narrow and wide helix.

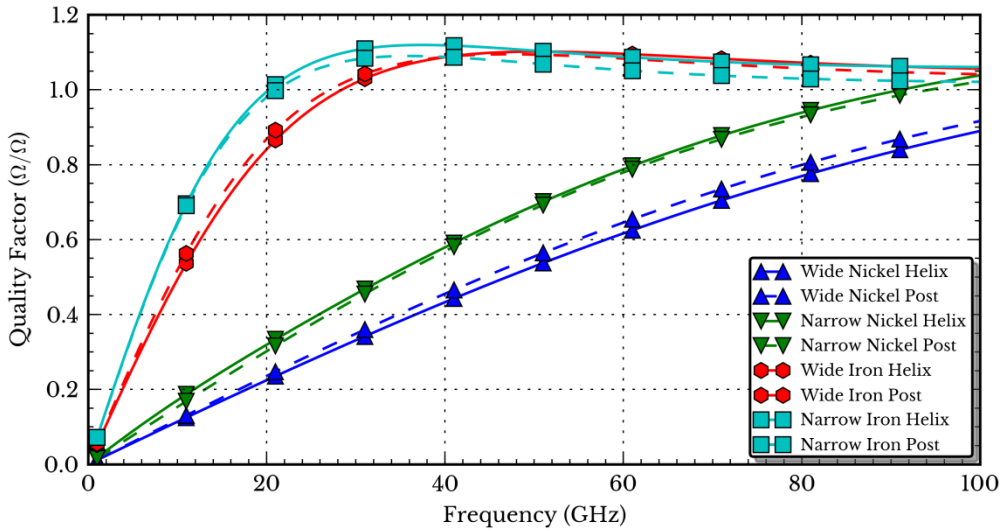


Figure 3.12: Comparison of the quality factor of wide and narrow helices made of iron and nickel. Also shown are the quality factors of the equivalent post inductors for both the narrow and wide helix.

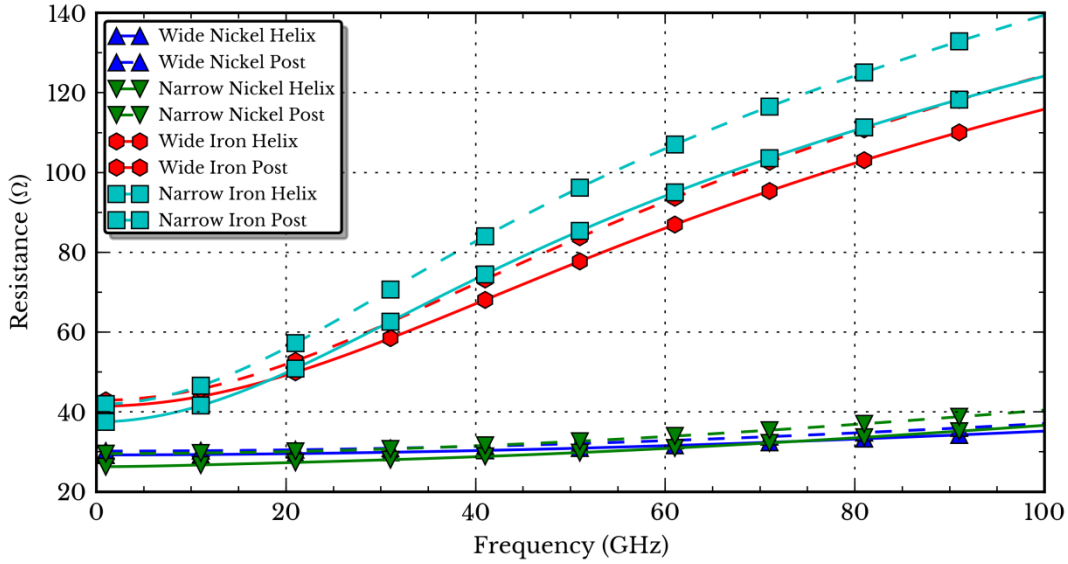


Figure 3.13: Comparison of the resistance of wide and narrow helices and the equivelent length of a straight wire.

Figure 3.12 shows the quality factor of the helices and posts and Figure 3.13 shows the resistance. The resistance of the narrow helix is higher than the wide helix.

3.3 Surrounding Medium

3.3.1 Single helix in an effective medium

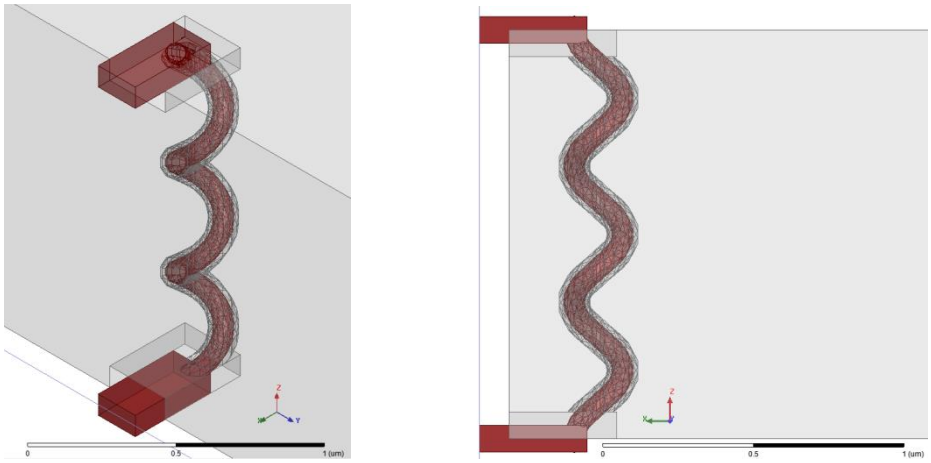
As previously discussed, the fabrication techniques for nano-scale inductors usually produce arrays of devices instead of just a single device. Section 3.5 simulated these structures using models that directly included the nanostructure of the film; however, to simulate the bulk properties of these films, an effective medium model was used. The effective medium model is an equivalent structure that can account for large numbers of closely packed devices. In addition, these simulations reduce the required random access memory (RAM) and computer time for an equivalently-sized structure.

Figure 3.2 demonstrates that with the GLAD technique, the resulting devices are very closely packed, which implies that the performance of any particular element is affected by the surrounding elements. CNTs also form closely-packed arrays, and will be discussed further in chapter 5. This effect can be modeled as an effective medium, meaning that the effect of the

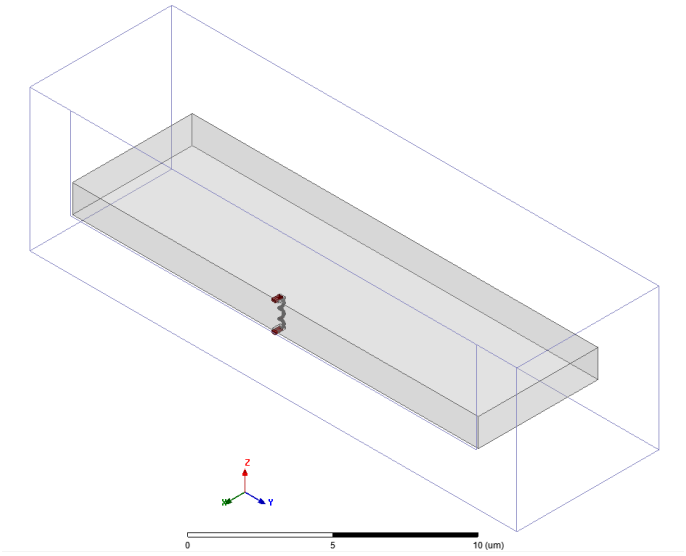
surrounding elements is equivalent to a conductor placed in a homogenous surrounding material (medium).

The effective medium approach is desirable, because a homogeneous material is much simpler to model numerically. For this work, it was found that accurately modeling nano-scale films with the detailed structure produced simulations that required large amounts of RAM, often into the tens of gigabytes. Replacing the accurate structure simulations with homogeneous effective media greatly reduced the total memory and time required to complete a simulation.

Figure 3.14 shows an effective medium model for a single helix embedded in a film. Figure 3.14a shows a close-up view of the inductor structure. The layout of the helix is similar to that shown in Figure 3.3, with a helix connected to a wave-port with a top and bottom wire. However, the exact dimensions of the helix differ from Figure 3.3. Figure 3.14b shows the same structure from the side and indicates the current path through the helix. Both of these images show that the inductor wire itself is separated from the film by a small air-gap. This gap allows for simulation of conductive films without shorting the helix through the medium. Figure 3.14c shows the entire simulation area, including the film, wire and radiation boundary. The effective medium allows for HFSS to use a coarse mesh far away from the helix, which allows the simulation to model a large on-chip area with reasonable accuracy.



(a) (b)



(c)

Figure 3.14: Model of a single inductor embedded in an effective medium.

3.3.2 Ideal magnetic material

Since magnetic materials produce the highest quality factors for inductors, they are one of the main focuses of this work. For such structures, the material surrounding each of the nanostructures is going to be magnetic. To determine the ideal effect that the surrounding material has on a nano-helix, the helix was simulated in a magnetic, non-conducting material. This simulation determined the effect of surrounding the helix with a material with a high permeability but no losses due to conductivity.

One class of materials which exhibits a low conductivity but a high magnetic permeability are ferrite materials (ferrites). Ferrites are magnetic-dielectric materials, meaning that they have a high μ_r parameter (relative magnetic permeability), but are non-conductive. Typically, ferrites are iron-oxide materials with other impurities added [8]. By using a widely-spaced array and filling the inter-post spacing with a ferrite material, the expected outcome would be similar to increasing the bulk permeability of the material without changing the other parameters.

Figure 3.15 shows the inductance of the single helix structure embedded in a film with varying magnetic permeability and no conductivity ($\sigma = 0$). Figure 3.15 shows that the inductance is improved significantly as the permeability is increased. The increase in the inductance is proportional to the increase in permeability over the permeability of free space. The permeability of the surrounding material is frequency-invariant (non-dispersive) so the inductance of the structure is constant over the entire frequency range.

Similarly, Figure 3.16 shows that the quality factor is increased significantly with the increase in permeability. The quality factor increases linearly with frequency, which is a result of the constant inductance and the nearly-constant resistance.

Figure 3.17 shows the resistance of the inductor structure, which exhibits nearly constant behaviour with a slight frequency dependency. The spread in resistance at 100 GHz is about 10 Ω between the highest and lowest resistance, which is small compared to the linear increase in the frequency; this results in the linear quality factor observed in Figure 3.16.

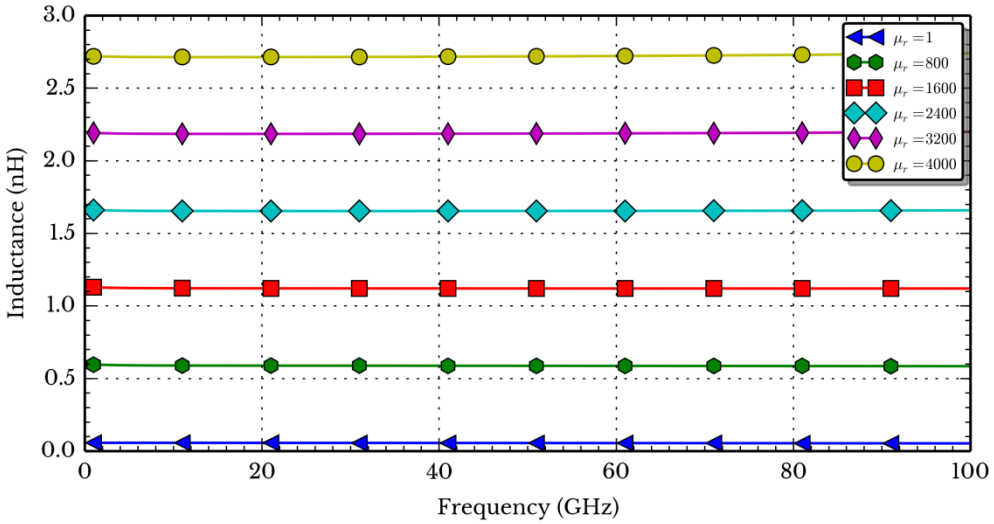


Figure 3.15: Inductance of a single helix in an ideal magnetic material.

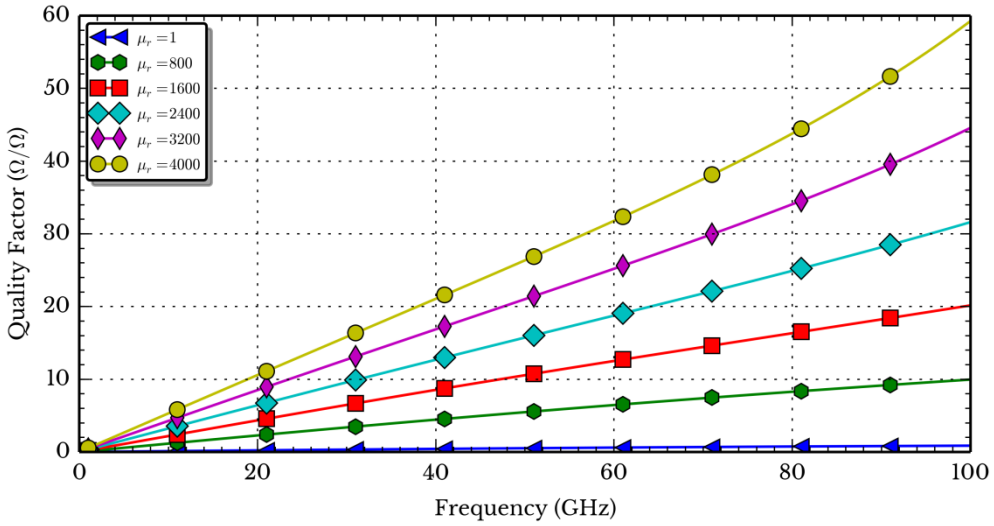


Figure 3.16: Quality factor of a single helix in an ideal magnetic material.

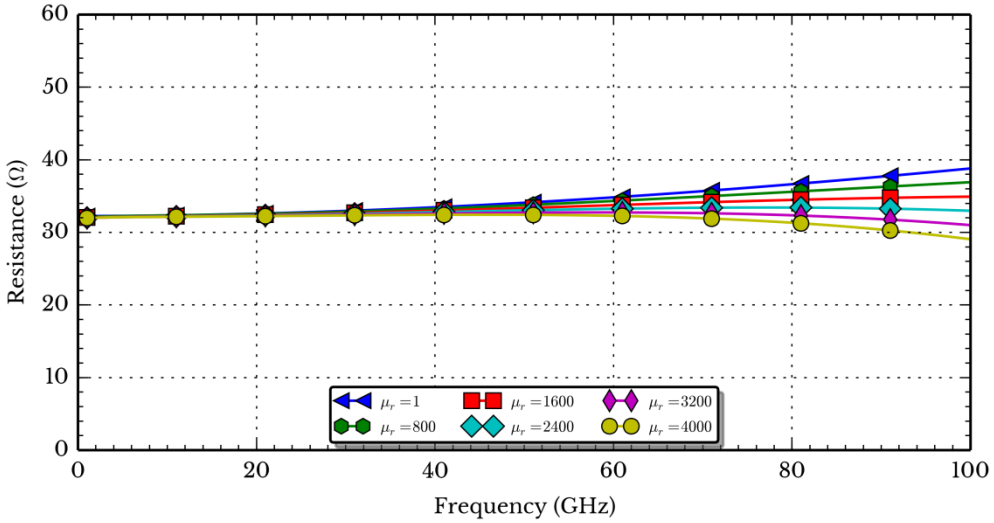


Figure 3.17: Resistance of a single helix in an ideal magnetic material.

To compare these results to the materials studied in the previous sections, bulk nickel has $\mu_r \approx 400$ and bulk iron has $\mu_r \approx 4000 - 6000$ [72]. Nickel and iron both have a high conductivity; however, the effect of increasing the film permeability is shown to increase both the inductance and the quality factor of the entire device.

A ferrite material could be used to fill-in the gaps between the nano-structured helices, to produce a higher quality factor than is available through increasing the helix permeability. Unfortunately,

however, to the author's knowledge, there is no known low-loss ferrite material in the millimetre-wave range.

3.3.3 Finite conductivity material

Section 3.3.2 analyzed the effect of the surrounding material permeability on the performance of the nanostructured helix inductor. However, the material studied in Section 3.3.2 was ideal, meaning that it had a conductivity of 0. This approximation may not be valid because of the nanostructures that make up the film, any real film will have a high conductivity. This conductivity would cause currents in the film material (outside the helix). These currents will have an overall effect of coupling the helix to nearby material.

Due to the fact that the materials produced by thin film processes can differ from their bulk equivalents, the conductivity cannot be assumed to be equal to the bulk value (such as in the case of nickel or iron) [73]. Therefore, assuming a relative permeability of $\mu_r = 600$ (the value of bulk nickel), the effect of a conductive surrounding material was simulated.

Figure 3.18 shows the inductance of the helix structure when surrounded by a conductive material. The inductance is highly dependent on the conductivity of the surrounding material. Figure 3.18 clearly indicates that the inductance of a single helix is highest when the surrounding material is non-conductive or low conductive. For the sake of clarity, low-conductivity simulations are not shown in Figure 3.18 because they overlap very closely with the non-conductive case. As the conductivity is increased above $\sigma = 10^4\ \Omega - \mathrm{m}$, the inductance is decreased. This effect is caused by the shielding of the conductive film that reduces the magnetic field produced by the helix. The shielding effect is also the reason that the more conductive surroundings have a higher inductance at low frequencies, since the shielding is based on the skin effect which is a frequency-dependent behaviour.

Figure 3.19 shows the resistance of the inductor structure with a conductive surrounding material. While the trend is not immediately obvious, the resistance of the device increases (to approximately $\sigma \approx 10^6\ \Omega - \mathrm{m}$) and then decreases as the conductivity is increased. The increase in the resistance is due to increased losses within the surrounding material caused by the magnetic field of the helix as the conductivity is increased. Once the conductivity passes a maximum-loss point, the surrounding material becomes conductive enough to provide an alternate current path through the device, which reduces the overall resistance.

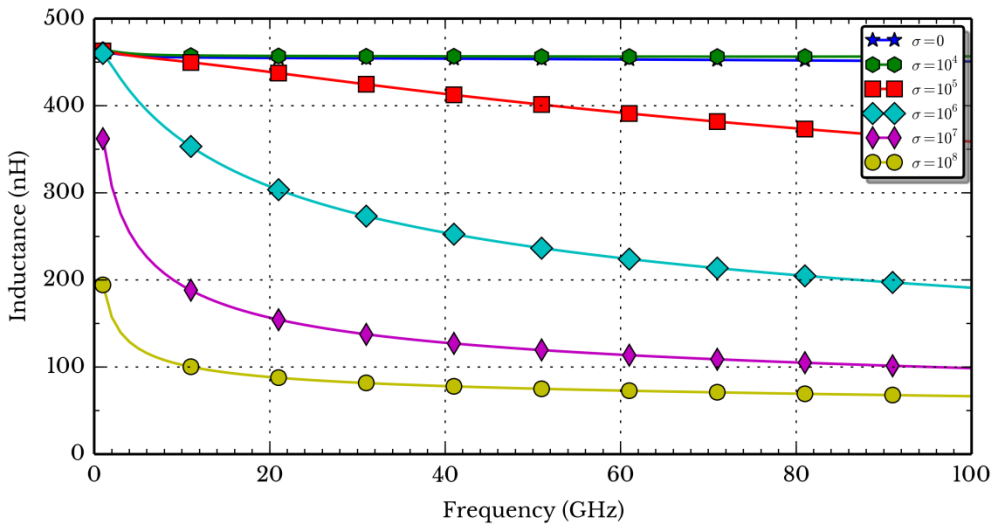


Figure 3.18: Inductance of a single helix embedded in a conducting magnetic material ($\boldsymbol{\mu_r = 600}$)

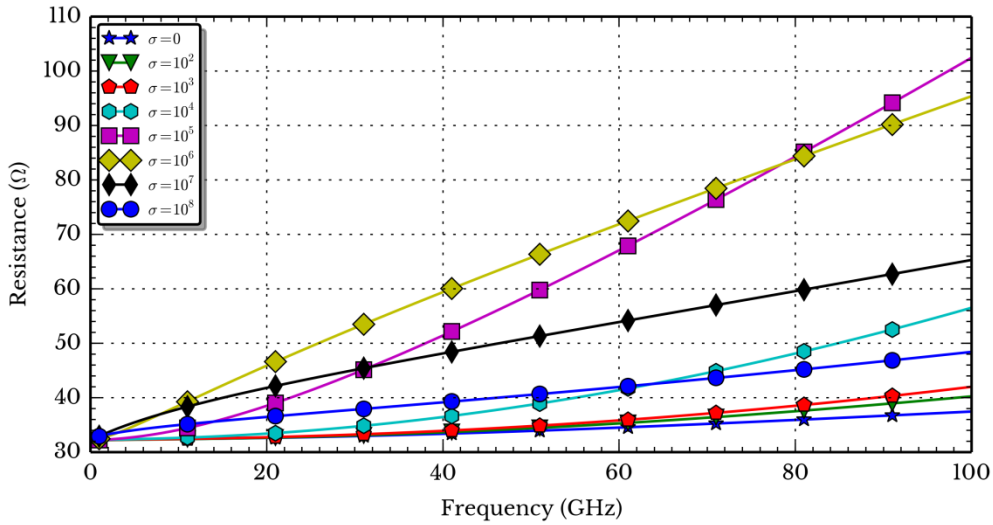


Figure 3.19: Resistance of a single helix embedded in a conducting magnetic material ($\boldsymbol{\mu_r = 600}$)

Finally, Figure 3.20 shows the resulting quality factor as a result of a conductive film. The conductivity reduces the quality factor in all cases, with particularly dramatic reductions between $\sigma = 10^4 - 10^5\ \Omega - \text{m}$. The reduction in quality factor is caused by both the increased resistance at low frequencies and the reduced inductance at high frequencies.

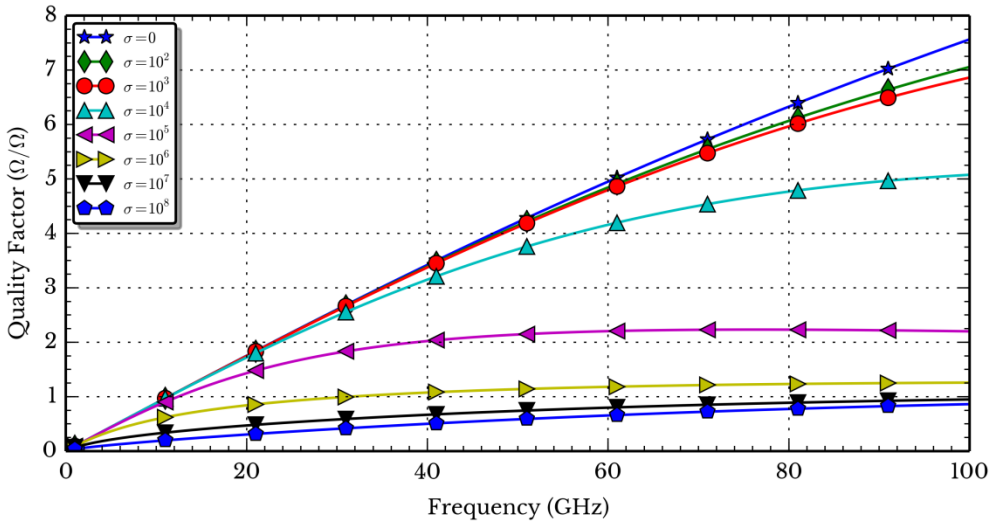


Figure 3.20: Quality factor of a single helix embedded in a conducting magnetic material ($\boldsymbol{\mu_r = 600}$)

A direct comparison between the quality factors shown in Figure 3.20 with the quality factor of the single helix shown in Figure 3.3 shows that the surrounding film increases the quality factor of the helix device. Higher film conductivities reduce the quality from the film towards the quality factor of a single wire. In nanostructured films, the conductivity of the film is expected to be below that of the bulk material used for the film because of the gaps between the nanostructures. These gaps remove conductive material to reduce the average conductivity of the film.

3.4 Anisotropic Media

3.4.1 Anisotropic conductivity

Section 3.3 studied the inductance effects of an isotropic film, meaning that the film has the same properties in every direction. However, this is a poor approximation for nanohelices, such as the ones shown in Figure 3.26[73][74]. Nanohelices have a good connection in the vertical direction, but only a poor connection in the horizontal direction, due to the separation between the helices. The major effect that this structure has is a different conductivity in the vertical direction, along the axis of the helix, than in the horizontal plane. This direction-dependent effect is called material anisotropy, or specifically anisotropic conductivity [74].

Anisotropic materials are materials that have properties that vary depending on direction. Nanostructured films have anisotropic properties due to their structure. The conductivity of nanostructured materials depends on the connectivity of the nanostructures.

For an anisotropic conductivity, the conductivity of the material becomes a tensor quantity as shown in 3.8 [8]. In principle, the conductivity tensor can take any form; however, for vertical

nanostructured films the only conductive direction is the vertical direction (the z-direction). In this case, all values in equation 3.8 are 0 except for σ_{zz}.

$$\overleftrightarrow{\sigma} = \begin{pmatrix} \sigma_{xx} & \sigma_{xy} & \sigma_{xz} \\ \sigma_{yx} & \sigma_{yy} & \sigma_{yz} \\ \sigma_{zx} & \sigma_{zy} & \sigma_{zz} \end{pmatrix} \quad 3.8$$

In the case of perfect vertical anisotropy, substituting the conductivity tensor into the Ohm's law (equation 3.9) results in a single current density term, equation 3.10. The horizontal current density terms are both equal to 0.

$$\mathbf{J} = \overleftrightarrow{\sigma}\mathbf{E} \quad 3.9$$

$$\mathrm{J}_z = \sigma_{zz}\mathrm{E}_z \quad 3.10$$

$$\mathrm{J}_x = \mathrm{J}_y = 0 \quad 3.11$$

The result of equations 3.10 and 3.11 is that the anisotropic reacts to electric fields in the z-direction in the same way that any normal conductor does. However, in the horizontal plane (x and y directions), the material acts as a dielectric material. This property of anisotropic materials means that they can be used in situations that a neither a dielectric nor a metal would be suitable. In this case, it will reduce the eddy currents that are caused by the changing magnetic field in the surrounding material.

3.4.2 Simulation of anisotropic films

HFSS allows for materials to have anisotropic conductivities of the form in equation 3.12. This means that HFSS allows a material to have a different conductivity in the $\hat{\boldsymbol{x}}$, $\hat{\boldsymbol{y}}$, and $\hat{\boldsymbol{z}}$ directions, but does not support other forms of anisotropic conductivity. This formulation allows for the simulation of an anisotropic conductivity in the vertical direction.

$$\overleftrightarrow{\sigma} = \begin{pmatrix} \sigma_{xx} & 0 & 0 \\ 0 & \sigma_{yy} & 0 \\ 0 & 0 & \sigma_{zz} \end{pmatrix} \quad 3.12$$

Using anisotropic materials in HFSS allows for the simulation of structures that are much larger than the nanostructures. Due to the large number of tetrahedrons required to accurately model the nanostructure of these films, accurately simulating large areas of film requires prohibitive amounts of time and computing resources. However, the use of anisotropic media allows HFSS to mesh the film as a single material, which greatly reduces the number of tetrahedrons required.

Figure 3.21 shows the resulting inductance from changing the isotropic film studied in Section 3.3 . The material simulated was a perfect anisotropic material (horizontal conductivity was 0), such that the film was only conductive in the vertical direction. The results show that a perfect anisotropic material (ie. zero horizontal conductivity) completely removes the shielding effects to produce a frequency-independent inductance. This is true regardless of the conductivity of the film, resulting in an increase in the inductance by a factor of 6 for the highest conductivity simulated for the helix in an anisotropic environment.

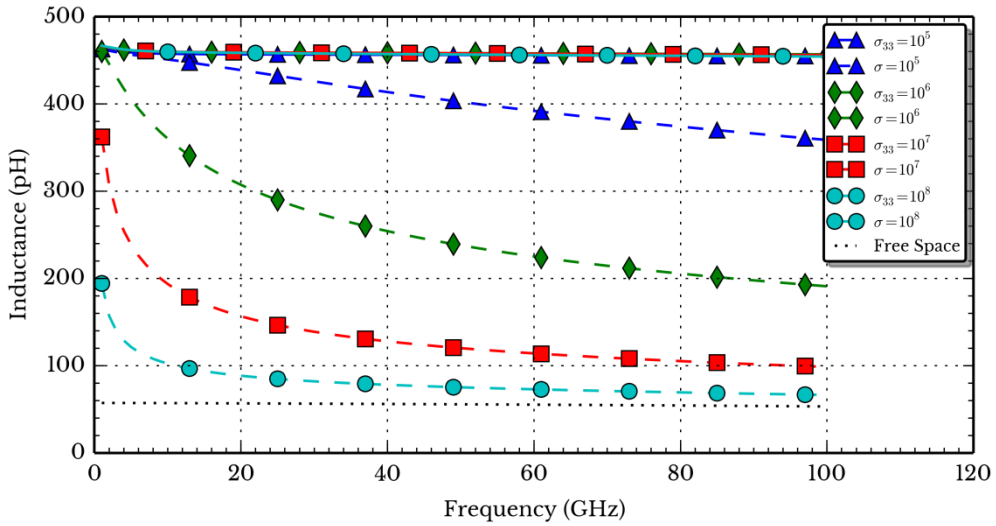


Figure 3.21: Inductance of an anisotropic conductive film compared to the isotropic film.

Figure 3.22 shows the resistance for the anisotropic material compared to the isotropic material. The resistance is also reduced for the anisotropic film, due to the reduction in conductor losses of the restricted conductive film. Again, the conductivity of the anisotropic film does not significantly affect the result because the losses require a horizontal current to have an effect.

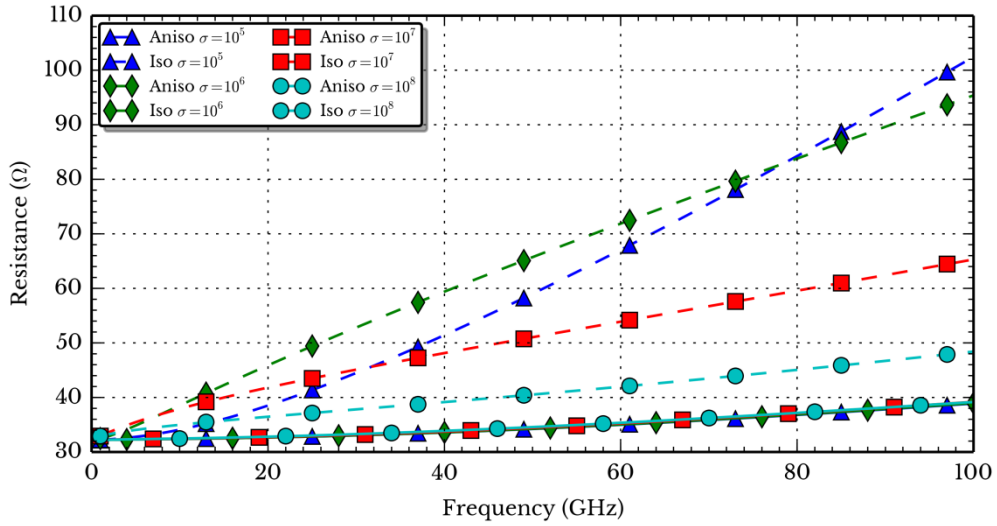


Figure 3.22: Resistance of an anisotropic conductive film compared to the isotropic film.

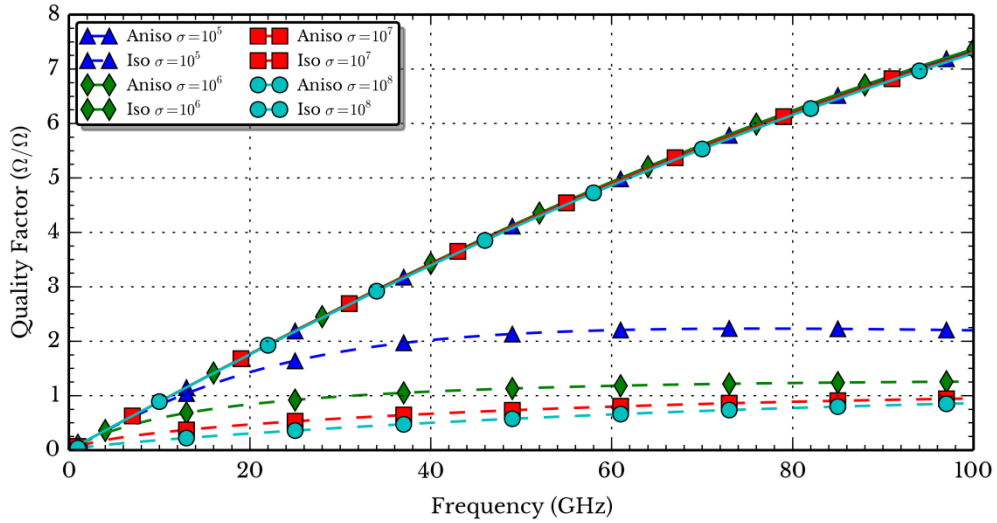
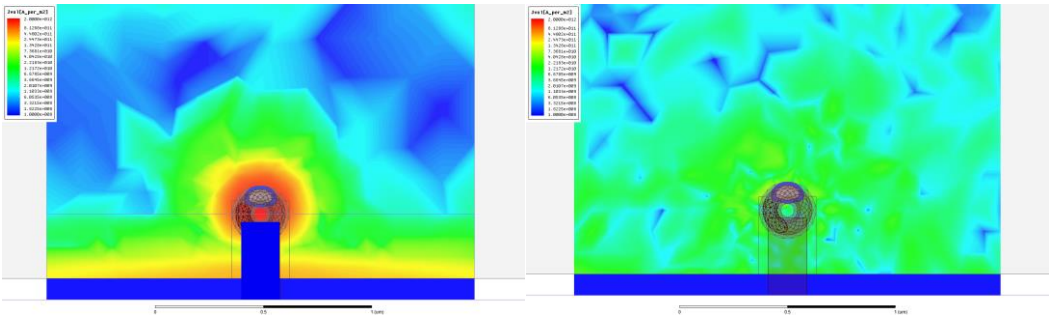


Figure 3.23: Quality factor of an anisotropic conductive film compared to the isotropic film.



(a) (b)

Figure 3.24: Current distribution of the inductor embedded in (a) an isotropic film (b) an anisotropic film of the same conductivity at 70 GHz.

Finally, the resulting quality factor is shown in Figure 3.23. The quality factor of the anisotropic film is significantly better than the isotropic film due to the reduction in restive losses and the increase in inductance. Comparing Figure 3.23 with the isotropic conductive film case in Figure 3.20 shows that the ideal isotropic film performs similarly to the ideal non-conducting magnetic film. This result indicates that real nano-structured helix films will exhibit a quality factor much higher than would have been expected by a solid film of the same conducting material.

An illustrative current distribution of an isotropic and anisotropic film of the same conductivity is shown in Figure 3.24. The isotropic film shows a high current distribution around the inductor (centre), and an additional current on the surface of the film. The combined effect is that the overall inductance is lowered when compared to the isotropic film. The isotropic film shows no leakage through the film at the edge and only small amounts of current inside the film.

3.5 Helix Arrays

3.5.1 Scaling behaviour of nano inductor films

It is important to incorporate the effects of array size on the performance of nanoinductors to incorporate them into systems. The inductor arrays were simulated in a similar fashion to the individual inductor structure: through a direct connection between the top of the array and the bottom of the array. The size of the array was varied to determine the scaling properties of nanostructured film inductors.

Figure 3.25 shows the simulation environment for the helix arrays. The blue box shows the absorbing boundary location and the red area shows the port location with respect to the inductor array. The array is roughly centered in the simulation environment.

Figure 3.26 shows a detailed view of the helix array. Figure 3.26a shows an isometric view of the array showing the square structure array (9x9 in this image). Figure 3.26b shows the same array directly from the side. The lines that are visible on the top and bottom connect the array directly to the port and the completely regular and separated nanostructure is visible.

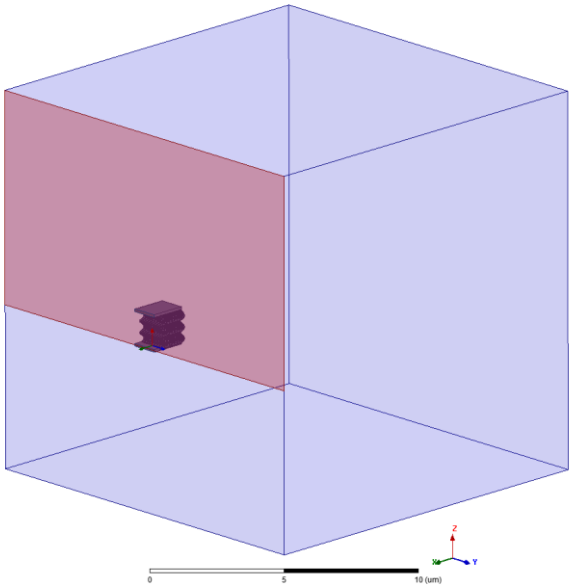
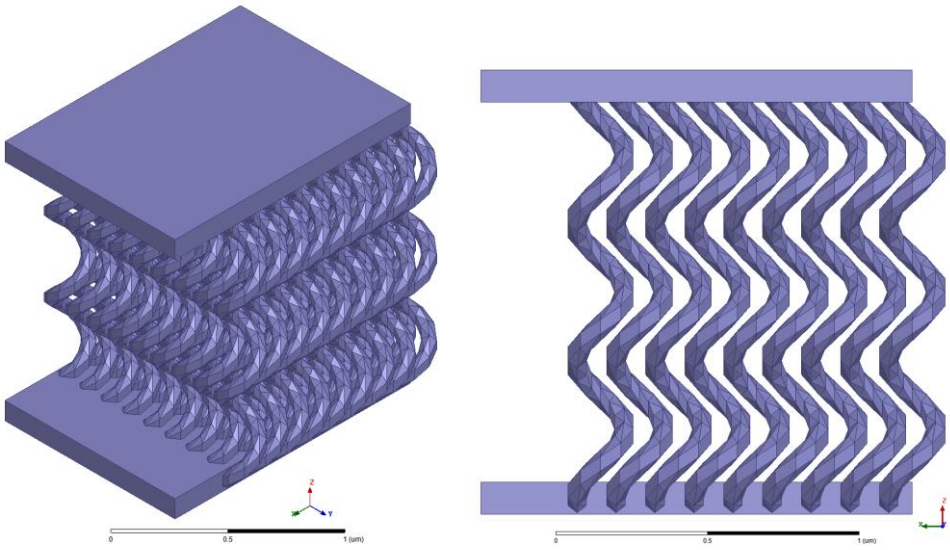


Figure 3.25: Helix array simulation environment.



(a) (b)

Figure 3.26: Detailed view of the **9 × 9** helix array. (a) isometric view of the helix array showing the 2-dimensional square array. (b) side view of the helix array showing the top and bottom lines that connect to the port as well as the completely separated nature of the helices.

The inductance depending on frequency and array size is shown in Figure 3.27. As expected, the inductance decreases slightly as the frequency goes up, similar to the single inductor shown in Figure 3.11. Figure 3.27 shows that the inductance is reduced dramatically as the array size grows. This result is expected since the total inductance is reduced when ideal inductors are placed in parallel and the array is effectively a set of inductors in parallel.

The quality factor, shown in Figure 3.28, varies in value for lower sizes of array but becomes more stable as the number of inductors is increased. For ideal inductor scaling, the quality factor remains the same, regardles whether the inductors are connected in parallel or in series. However, for the helix structure shown in Figure 3.26b, the skin depth and proximity effects cause the quality factor to change from the single-inductor value.

The resistance of the helix array reduces as the number of helices goes up, as shown in Figure 3.29. This is an expected result, because the resistance of a large number current paths is always lower than a smaller number of current paths that individually have the same resistance. This result shows that the variation in quality factor is due to the relative ratio of decrease in inductance and resistance.

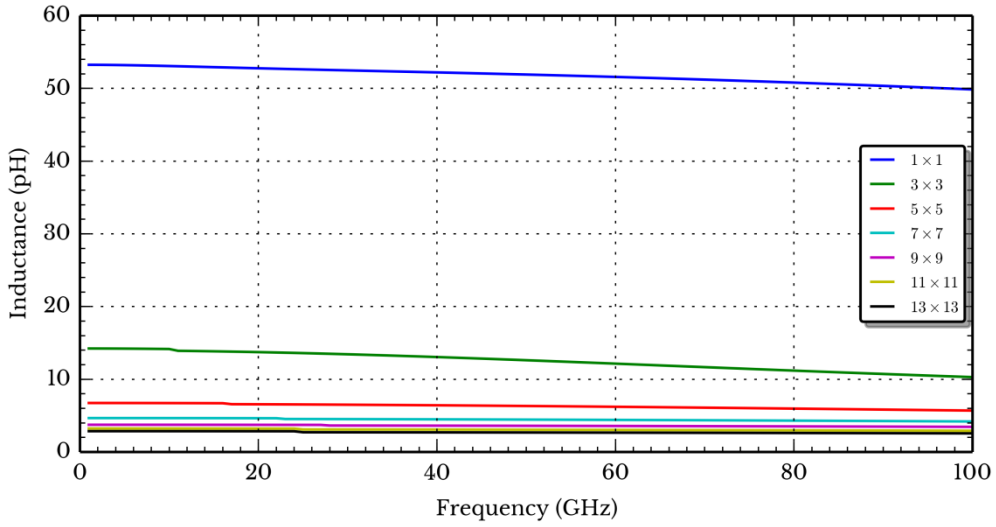


Figure 3.27: Simulated inductance of nickel helix arrays.

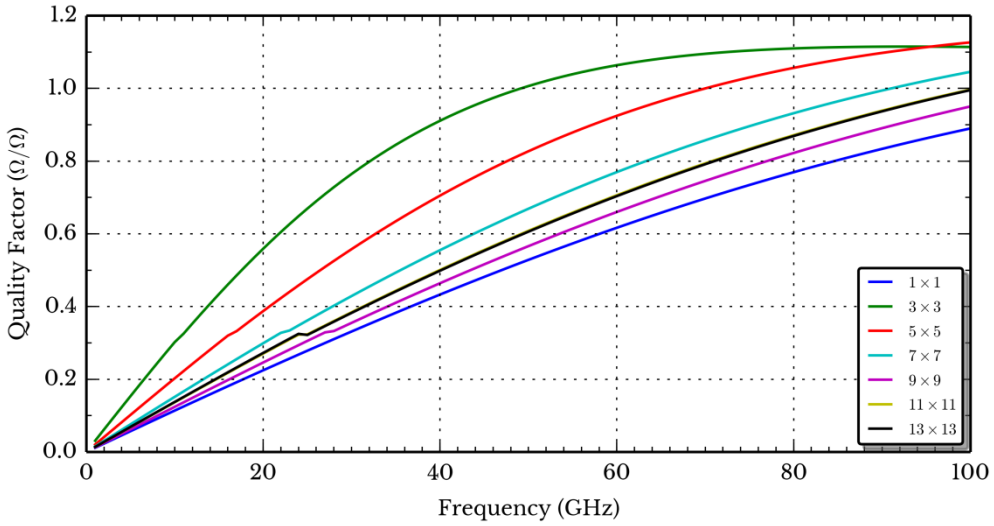


Figure 3.28: Simulated quality factor of nickel helix arrays.

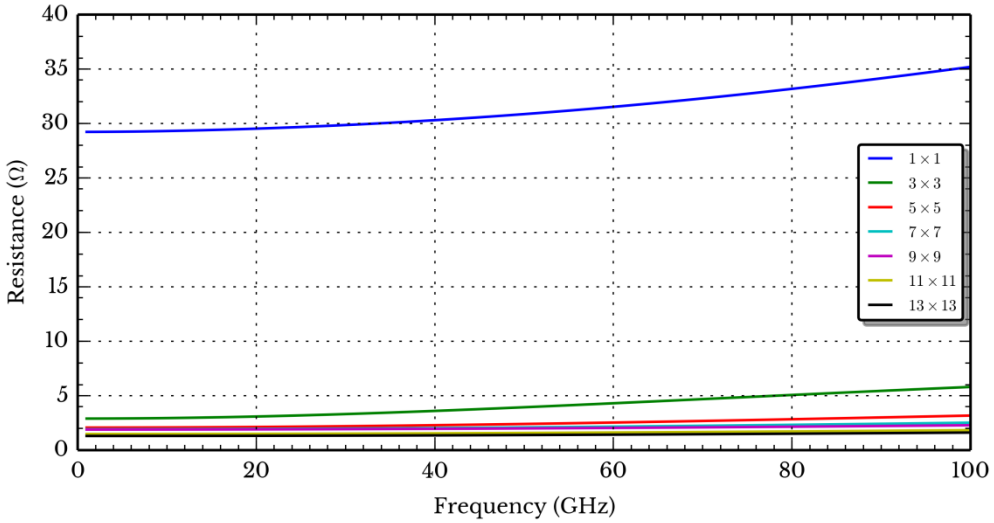


Figure 3.29: Simulated resistance of nickel helix arrays.

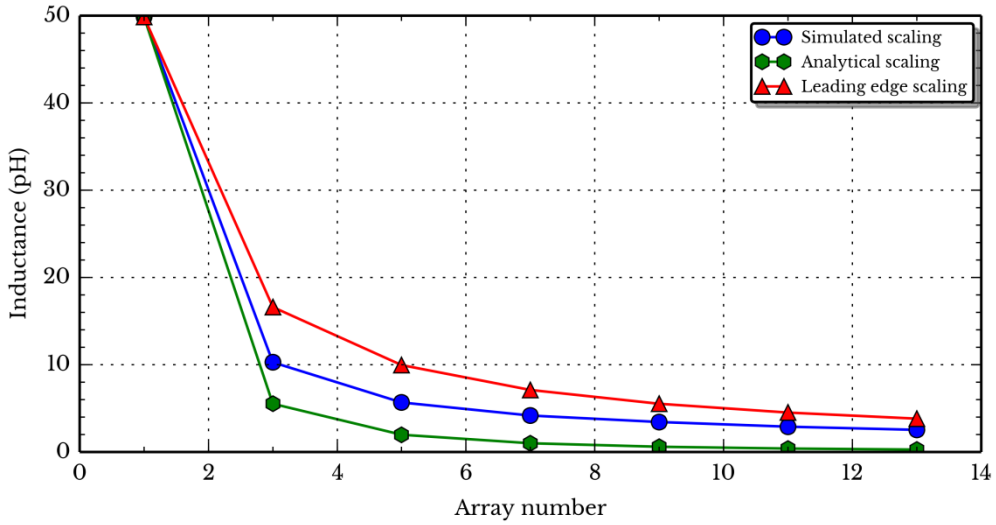
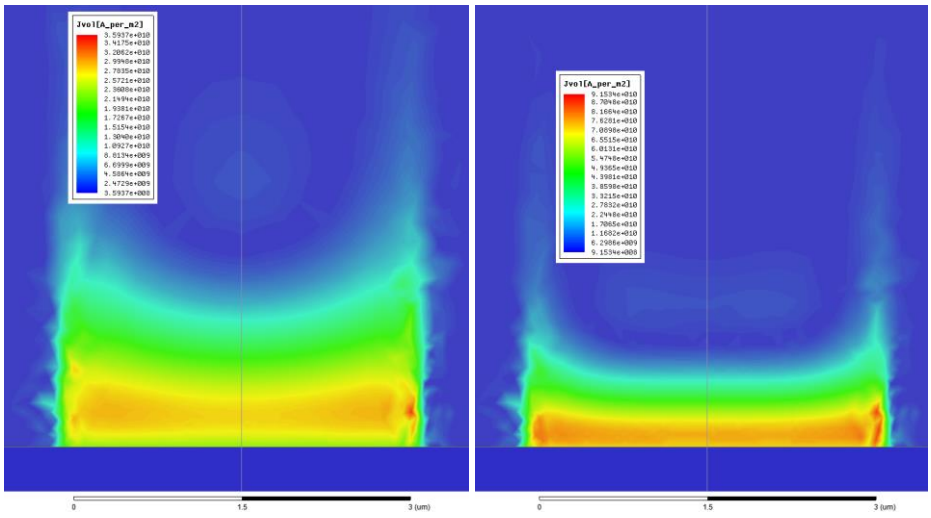
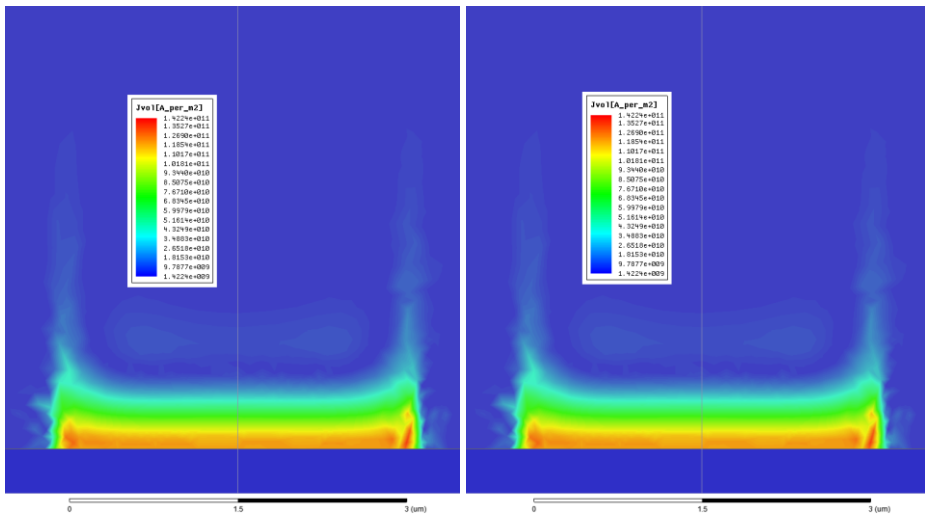


Figure 3.30: Inductance scaling of helix arrays. The array number is the number of helices along each side of the square (eg. an array number of 5 means the simulation is a 5x5 array). The inductances are simulated at 100 GHz.



(a) (b)



(c) (d)

Figure 3.31: Top-down view of the current distribution of an anisotropic nickel film (reduced conductivity, $\sigma = 10^5$) at (a) 10 GHz, (b) 30 GHz, (c) 50 GHz, (d) 70 GHz. The edge of the film is visible as the sudden transition from no current to high current at the bottom of the image. The incoming wave is travelling from the bottom of the image to the top. The skin depth is very small at high frequencies, including depths of less than 1 µm for 50 and 70 GHz. The small skin depth means that fewer inductors are conducting in parallel, increasing the effective inductance.

From the data in Figure 3.27, Figure 3.28 and Figure 3.29, the scaling effect was calculated at 100 GHz and plotted in Figure 3.30 (labeled *simulated scaling*). The inductance of the array drops off dramatically for a small number of inductors, but is reduced less when the number of inductors in an already large array is increased. To compare the simulated scaling performance of the GLAD array, the analytical scaling of an inductor array is plotted as the *analytical scaling*.

The analytical scaling result is the ideal inductor scaling behaviour, given by equation 3.13. The simulated value for the inductance of a single structure is the value of L_0 and the total number of helices is the value of N. In Figure 3.30, the number of inductors is the square of the array number.

$$L = \frac{L_0}{N} \qquad 3.13$$

Figure 3.30 shows that there is a poor fit between the analytical scaling and the simulated scaling. The mismatch is due to the skin effect in the GLAD film at millimetre-wave frequencies. Figure 3.31 shows the current distribution in the GLAD film at various frequencies. The skin depth for the GLAD film prevents the whole array from conducting and reduces the effective number of elements in the array. The skin depth limits the reduction in inductance due to the array size, at high frequencies.

To better approximate the inductance of the film, the analytical scaling relation was modified by only counting the inductors on the outer edge of the film, ie. the first row of inductors. The leading edge assumption accounts for the skin depth by assuming that the bulk of the current passes through the first row of the inductors. Proportionally, the leading edge approximation should become more accurate for larger numbers of arrays, with the singular exception of the 1x1 array, where it is exact. Leading edge is determined by equation 3.13; however, the value for N is just the array number (not squared). Figure 3.30 shows that the simulated inductance approaches the first row scaling approximation for large values of inductors.

The accuracy of the two analytical scaling models was quantified by calculating the percent difference between the approximations and the simulated. The percent difference between the models and the simulations is given by equation 3.14.

$$\text{Percent Difference} = 100 \times \left| \frac{L_{\text{approx}} - L_{\text{simulated}}}{L_{\text{simulated}}} \right| \qquad 3.14$$

The percent difference is plotted in Figure 3.32. Figure 3.32 shows that both scaling models are poor predictors of inductance for small numbers of inductors, but the linear scaling model becomes more accurate for larger arrays.

The low accuracy of the scaling models at low numbers of inductor models indicates that there are non-ideal interactions between the inductors in the array. This result is not surprising, given the closely-packed structure of the array. The increasing error of the analytical scaling model for higher array numbers further indicates that non-ideal interactions occur for large numbers of inductors.

The decreasing error of the linear scaling model indicates that one of the non-linear effects of the inductor scaling is the uneven distribution of current through the array when fed from the side.

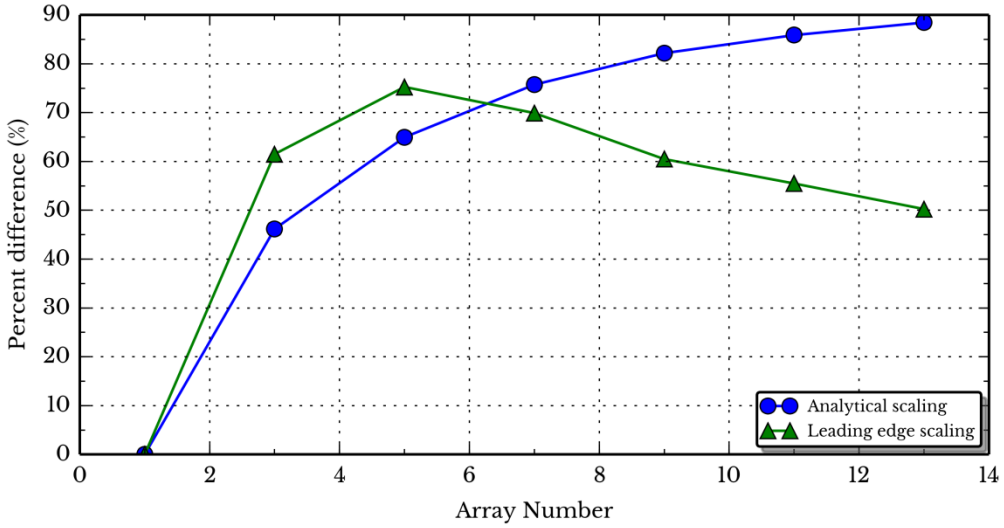


Figure 3.32: Percent difference between the analytical inductor scaling models and the simulated inductor scaling behaviour.

3.5.2 Fabrication defects in helix arrays

Real fabrication processes do not produce ideal structures such as the ones that have been studied earlier in this chapter. Figure 3.2 demonstrates a number of these defects from the GLAD process: widening, terminated posts, and random material defects. These defects were modeled in order to determine their effect on the performance of the nanostructures as inductors.

The first imperfection that was studied was an increase in the helix radius at the top of the film (later in the growth stage). Figure 3.33a shows a 7x7 array of helices and Figure 3.33b shows the same but with a linearly increasing helix radius toward the top of the film. The upper helix radius is 50% greater than the base helix radius. This model shows the crowding and inter-helix contact towards the top of the film that can be seen in Figure 3.2a. This widening effect is seen in many examples of structures grown with the GLAD technique (visible in images in [67][75][55]).

The second type of imperfection that can be seen in Figure 3.2 is terminating helices. These are nanostructures that pre-maturely terminate because of overshadowing by the surrounding helices. Figure 3.33c shows a model of this structural defect added to the model of the widening helices. The defect shown in Figure 3.33c is much worse than the defect shown in the actual films shown in Figure 3.2, this is intended to produce a worst-case scenario for the inductor performance. The lower helices do not make direct contact with both sides of the film, which reduces the average conductivity of the film. The model in Figure 3.33c adds the height defect to the widening helix defect, so that the final model exhibits both defects.

The final type of defect that is shown in Figure 3.2 is the non-uniformity of the helix surfaces. Many of the helices in Figure 3.2 show protrusions to reduce the surface quality and increase contact between the helices in the lateral direction. This imperfection was modeled by pseudo-randomly distributing cubic particles throughout the film model, as shown in Figure 3.33d.

Figure 3.34 shows the inductance of each of the added defects as they are added to the model. Figure 3.34 indicates that the widening of the helices towards the top of the film increases the inductance of the overall film. This effect is reduced by the terminating helices and the additional particle defects in the film. However, the film with all defects added exhibits a higher inductance than the ideal helices.

The resistance of the imperfect array is shown in Figure 3.35. In this case, the ideal helices have the lowest resistance and the expanding helices have the highest resistance. The particle defects increase the resistance of the array slightly, but not significantly.

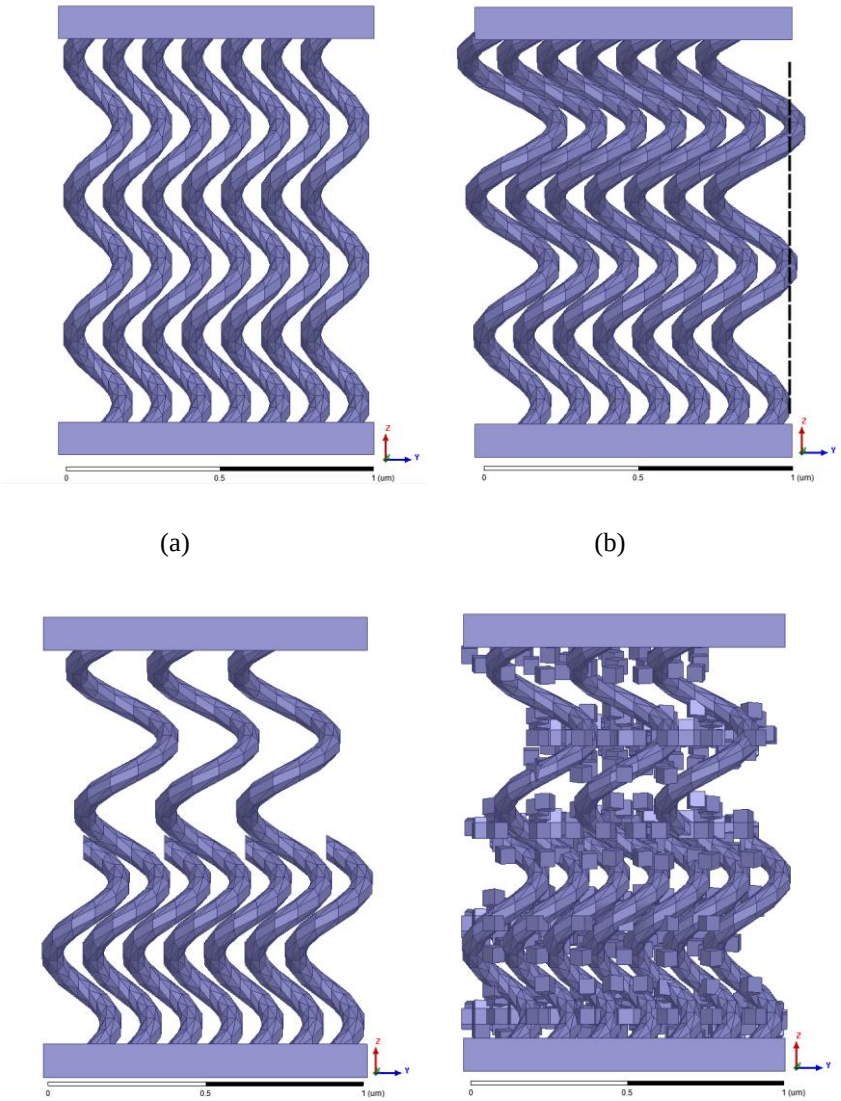


Figure 3.33: Helix width comparison. (a) An idealized helical film. (b) The same film but with a radius change of 50% between bottom and top. The radius change is emphasized by the vertical, dashed line. (c) Addition of helix termination defects to the model in (b). (d) Addition to random growth defects to the model in (c). The defects are modeled as arrays of cubes of material that are placed pseudo-randomly. This model includes all observed defects.

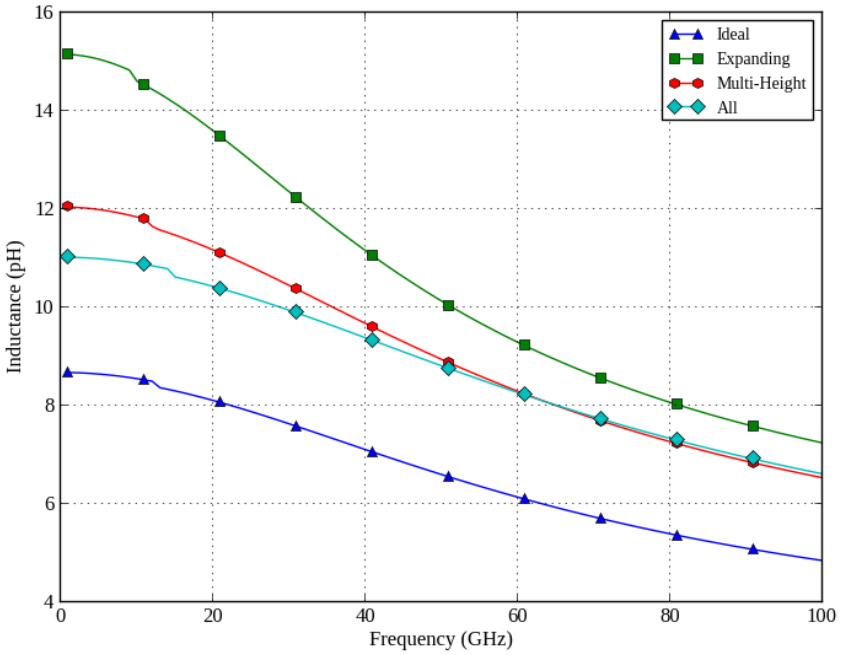


Figure 3.34: Inductance of a **7 × 7** helix array with defects added.

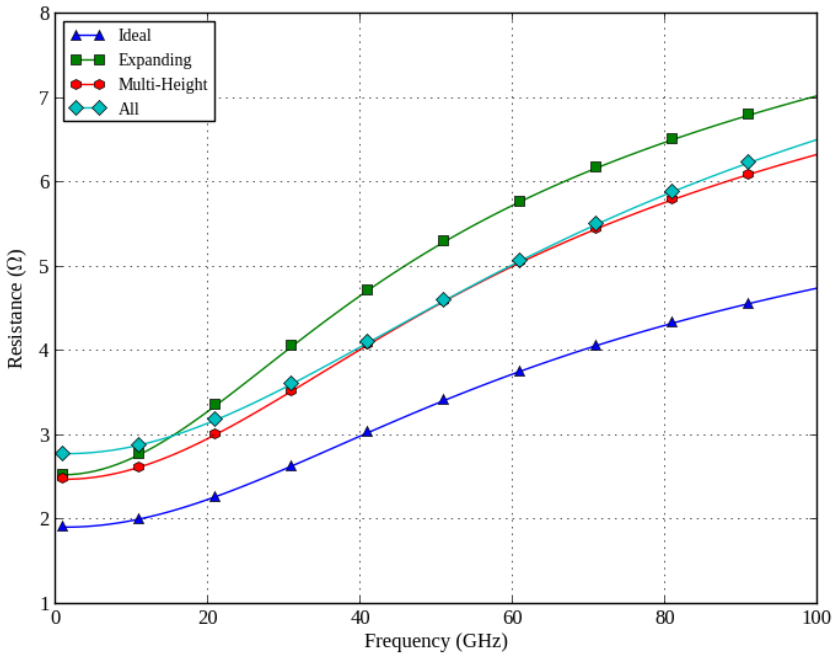


Figure 3.35: Resistance of a **7 × 7** helix array with defects added.

Figure 3.36 shows the resulting quality factor of the imperfections simulations. The overall result is that the quality factors varies as much as 0.1 around 20 GHz; however, the quality factor is largely unchanged for frequencies above 40 GHz. This result indicates that the film defects do not significantly impact the performance of the film at millimetre-wave frequencies.

The relative invariance of the inductance, resistance and quality factor to the defects in a nanostructured film indicates that the film is relatively insensitive to fabrication parameters that affect the structure in this way.

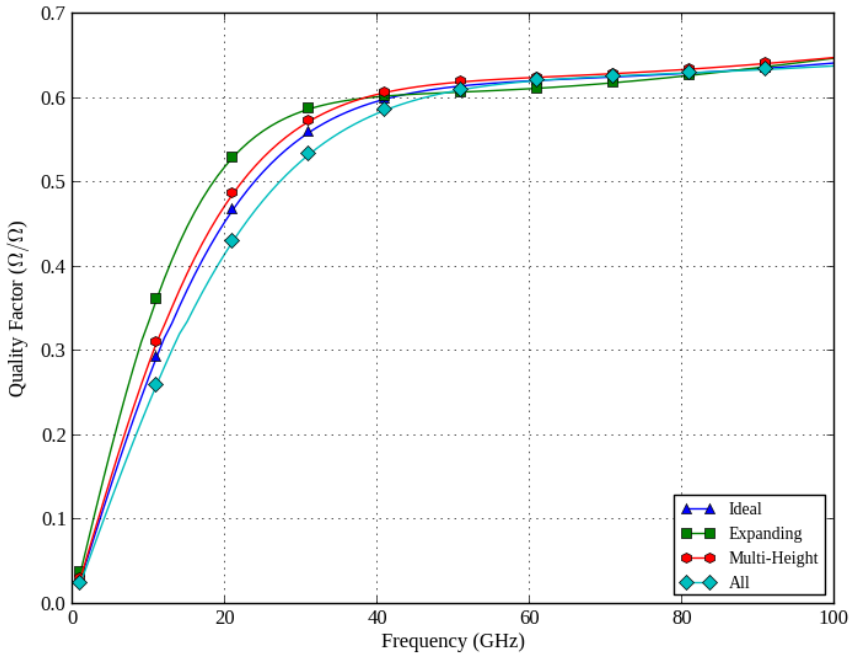


Figure 3.36: Quality factor of a **7** × **7** helix array with defects added.

3.6 Summary

3.6.1 Nanostructured materials as inductors

This chapter has presented compelling simulation-based results for the use of nano-structured materials as inductive devices for on-chip applications. Films of nano-scaled helices have unique properties, such as ferromagnetism combined with anisotropic conductivity, that make them uniquely suited for building on-chip inductor devices. Utilizing nano-structures, the total on-chip area of an inductor can be reduced by several orders of magnitude. This reduced area increases the

utility of on-chip inductors and will make them more desirable integrated components and it will make it possible to integrate large numbers of inductors on a chip, similar to other components.

Chapter 4: **Magnetic Thin Film Inductors by Glancing Angle Deposition**

4.1 Introduction to GLAD Films

4.1.1 Introduction

This chapter will introduce the measurement procedure for creating on-chip inductors using nanostructures created by glancing angle deposition. The chapter will begin by introducing glancing angle deposition before presenting the measurement methodology and measurement results.

4.1.2 Glancing angle deposition

*Gl*ancing *a*ngle *d*eposition (GLAD) is a fabrication technique that utilizes physical vapor deposition (such as evaporation or sputtering [69]) with the substrate at an oblique angle to the incoming vapor to produce thin films that consist of arrays of nano-scaled structures [50]. Figure 4.1 shows a conceptual diagram of the GLAD setup. The GLAD fabrication technique uses the angle of the substrate and the rotation of the substrate to control the exact structures that are produced (posts, helices, or polyhedrons) [50].

GLAD films have high porosity and high surface area [51]. The nanostructure of GLAD films results in a bulk anisotropic conductivity, especially at deposition flux angles greater than 60°, relative to the deposition source [54]. The GLAD technique can be applied to any material that can normally be deposited using physical vapor deposition techniques [51].

Because of the high surface area, GLAD films have applications in a number of devices, such as photovoltaic cells [51] and humidity sensors [53].

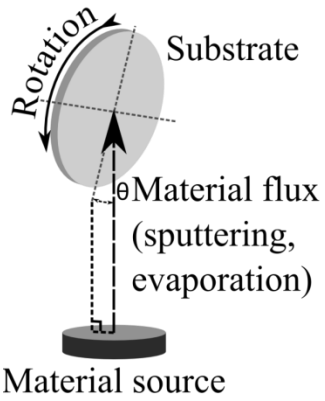
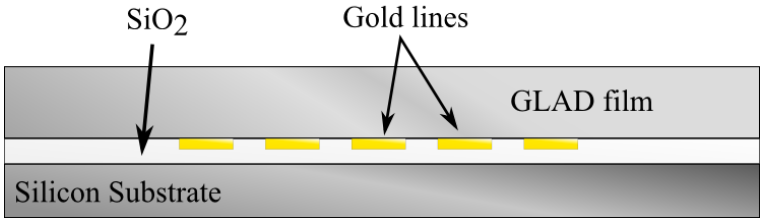


Figure 4.1: Glancing angle deposition setup.

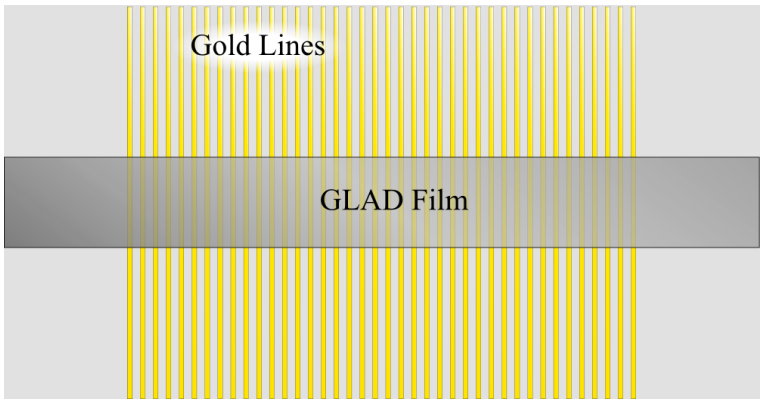
4.1.3 Fabrication

A nickel GLAD film was obtained from Dr. Michael Brett and Dr. Michael Taschuk. The GLAD test structure is shown in Figure 4.2; the film was grown on top gold traces embedded in a silicon dioxide layer as shown in Figure 4.2a. Before deposition, the gold and the oxide layers were planarized to produce a flat surface, which is necessary for GLAD.

Figure 4.2b depicts the test device layout. The gold lines on the substrate were exposed as contacts for DC and RF measurements. The GLAD film was patterned by a lift-off technique, leaving the ends of the gold lines exposed. The test substrate was approximately 2 cm in length and 7 mm in width; however, the substrates were cleaved manually, causing a variation of the substrate width of approximately 1 mm. The gold lines were 3 μm wide and spanned the width of the substrate. The spacing between the gold lines varied between 1.6 μm and 4.2 μm.



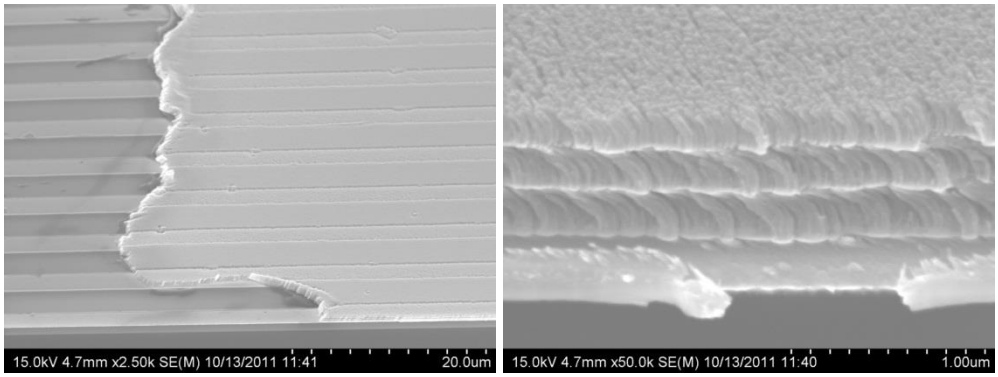
(a)



(b)

Figure 4.2: Test substrate layout for RF measurements of the GLAD film. (a) The cross section of the test substrate. The dimensions are not to scale: the oxide layer is approximately **1 μm** thick, the gold lines are **100 nm** thick, and the GLAD film is about **500 nm** thick. (b) The layout of the film on the substrate. The GLAD film covers the entire length in the long axis, but leaves the gold lines exposed in the short axis. Note that the dimensions are not to scale; the gold lines are closely spaced and approximately **3 μm** in width, compared to a width of about 7 mm (short axis) for the substrate and a length of about 20 mm (long axis).

Scanning electron microscope (SEM) images of the fabricated film are shown in Figure 4.3. Figure 4.3a shows the GLAD film on top of the gold lines and silicon dioxide and the rough edge of the GLAD film patterned by lift off. The nanostructure of the GLAD film is shown in Figure 4.3b. The film consists of closely-packed helices, with spacing between the individual helices of less than 100 nm.



(a) (b)

Figure 4.3: Fabricated nickel film. (a) A portion of the GLAD film with good uniformity. (b) A close-up view of the nano-structure of the film featuring the closely-packed helices.

4.2 Measurement techniques

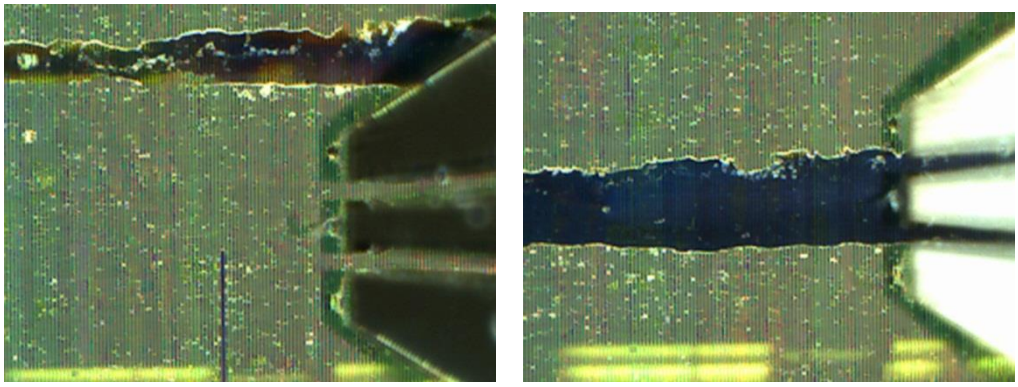
4.2.1 Direct probing

The first testing procedure that was attempted was a simple series connection through the GLAD film, with the probe's signal line directly contacting the top of the GLAD film. If successful, this technique would allow for a simple series subtraction of the results to directly yield the inductance of the film.

This technique was carried out by aligning the probe to the gold lines on the substrate so that there was a short between the ground and signal lines. This measurement characterizes the substrate and test devices. The probe was placed down on the substrate as shown in Figure 4.4a and a measurement was taken. Next the probe was moved to a location on the GLAD film such that only the signal line was touching the substrate as shown in Figure 4.4b.

After the initial measurements were taken, the touchdown spot was observed under scanning electron microscope (SEM) to verify the film integrity. Figure 4.5 shows a touchdown spot after

measurements. It is clear from these images that the GLAD film is completely removed by a touchdown. Repeated attempts to lightly touch down directly on top of the film produced the same destruction of the film. Therefore, a direct contact method of testing the film is not feasible.



(a) (b)

Figure 4.4: Direct touchdown on film for series measurement.

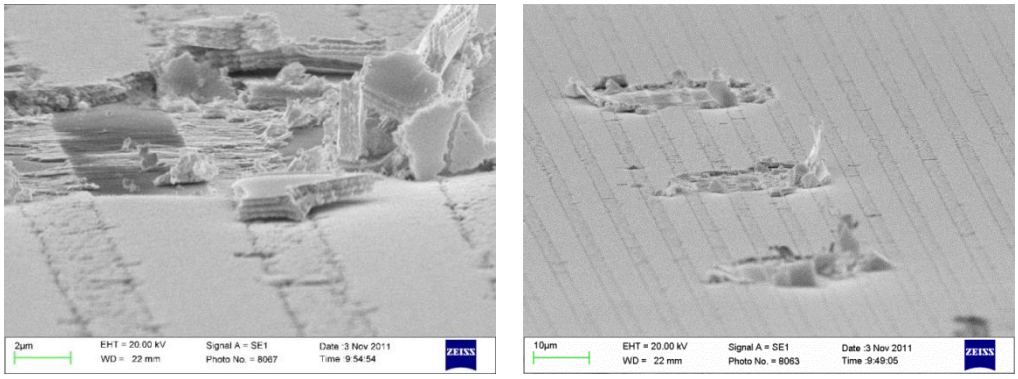


Figure 4.5: SEM image of damage to the GLAD film due to direct contact with the RF probe.

4.2.2 Anisotropic Conductivity

To overcome the touchdown measurement problem, a top capping layer was investigated. SEM images, such as Figure 4.6, show that the film has a different structure, depending on the substrate material that the film was grown on. Particularly, Figure 4.6 shows an apparent gap between the GLAD film grown on the gold lines and the silicon dioxide.

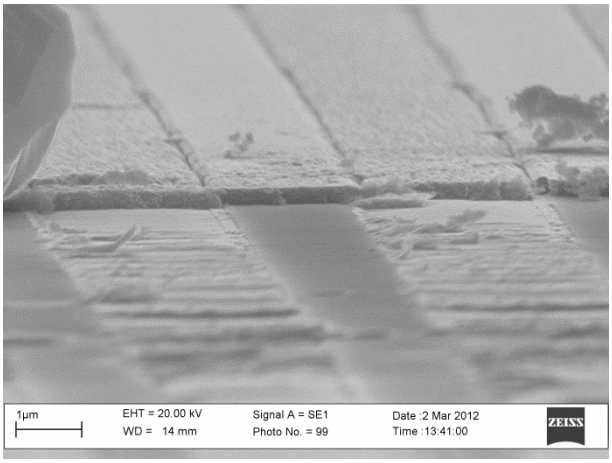


Figure 4.6: SEM image of a non-uniform section of GLAD film. The image clearly shows gaps in the film that are smaller than 2 microns (1 bar in the scale graph).

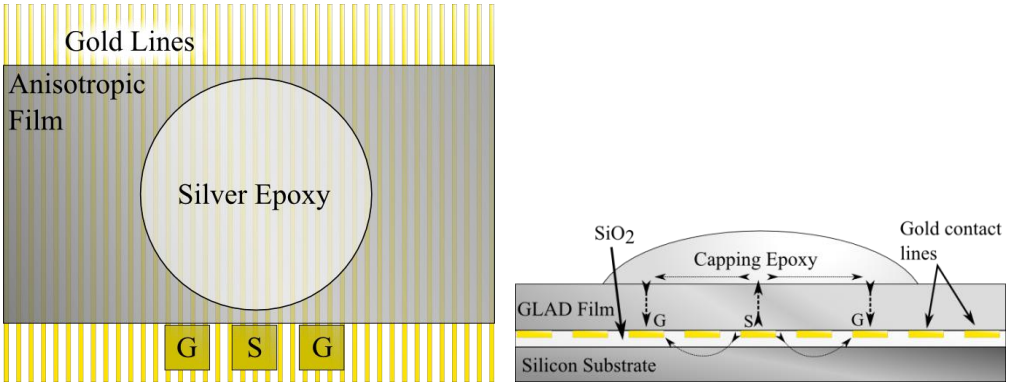
Electrical separation between the lines was verified by DC measurements. Two DC probes were placed on the substrate and the resistance between the two probe tips was measured. It was found that when the DC probes contacted the same gold line a resistance of a few hundred ohms was measured, but when the probes were moved to nearby lines the measured resistance was greater than1 MΩ, which was the limit of the digital multi-meter (DMM) used to conduct the measurements. This result confirms that the film is not conductive in the direction perpendicular to the gold lines. However, vertical conductivity is assumed to be a much lower value due to the composition of the film.

4.2.3 Capping technique

The anisotropic nature of the film's conductivity allowed for a capping technique to be employed to perform measurements of the film's resistance and inductance. Figure 4.7 shows the measurement setup: place a conducting layer directly on top of the film to allow for a DC connection through the film between the signal and ground terminals. This DC connection allows for the current to flow through the film into the capping layer. Once the film-plus-cap has been measured, the film and cap are removed and measured again to calculate the effect of the substrate on the measurements.

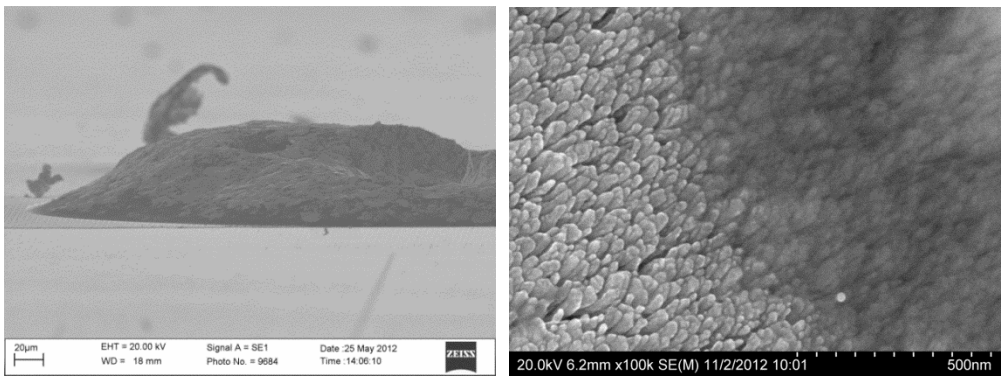
Figure 4.7a shows the layout of the film with the cap layer. The cap layer is labeled as *silver epoxy* in the diagram. It is important to place the cap in such a way that it does not contact both the top of the film and the underlying substrate which would likely cause a short between the cap layer and the substrate. The G-S-G squares in the figure indicate the ground-signal-ground configuration of the RF probes used to conduct the measurement. Figure 4.7 is not to scale; however, each of the terminals of the probe contacts multiple gold lines on the substrate. Figure 4.7b shows the cross-

section view of the test structure. The dashed lines indicate the current paths through the film and the substrate. There is a capacitive coupling between the gold lines and the silicon substrate, resulting in an overall capacitance for the substrate path. This capacitance is subtracted from the total measurement, leaving only the current path through the film and cap layer.



(a) (b)

Figure 4.7: Capping technique measurement layout. (a) Top-down view of the conductive capping material (labeled silver epoxy). The material is placed directly on top of the film. (b) Cross-section view of the capping layer. The dashed lines show the direction of current through the device.



(a) (b)

Figure 4.8: SEM micrographs of the silver conductive epoxy capping layer. (a) Epoxy shown deposited on top of the film. (b) Interface between the epoxy and the film.

The material that was chosen as the capping layer was the conductive silver epoxy product from MG Chemicals, product number 8331. According to the manufacturer, this material has a low resistivity of $0.017\ \Omega \cdot \text{cm}$ [76]. This epoxy is a non-conductive organic material which has silver

particles mixed into it. Figure 4.8a shows the epoxy deposited on top of the GLAD film. The epoxy can be seen to have a small contact angle with the nickel film, indicating that the epoxy adheres well to the film. Figure 4.8b shows the interface between the epoxy and the penetration of the epoxy into the film is visible.

Figure 4.9 shows the silver particles in the epoxy and that the smallest of the particles are approximately 1 μm in diameter, which is too large to penetrate the film. This is an important observation because if the silver particles were able to penetrate the film then the effect of the conductivity of silver would have to be taken into account when modeling the film. From this image it can be concluded that the film is only connected on the top surface.

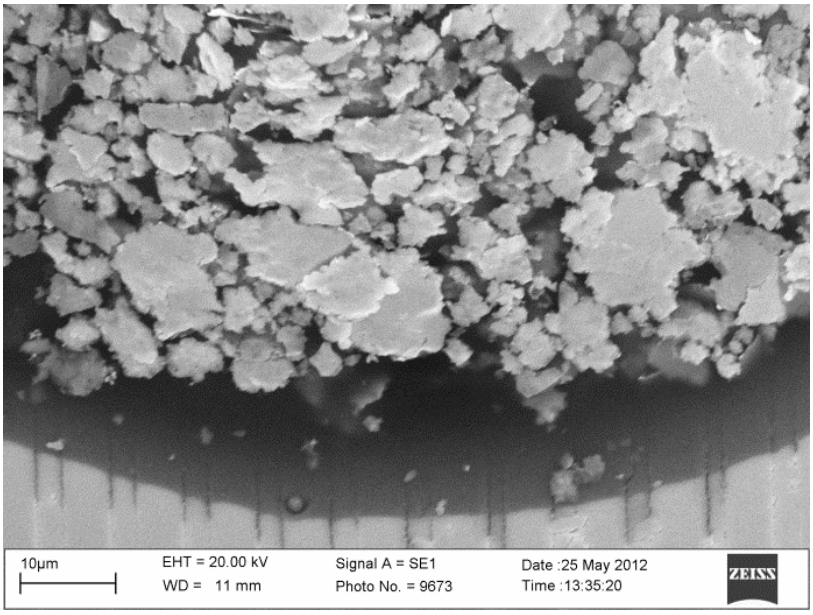


Figure 4.9: Silver particles suspended in the epoxy material.

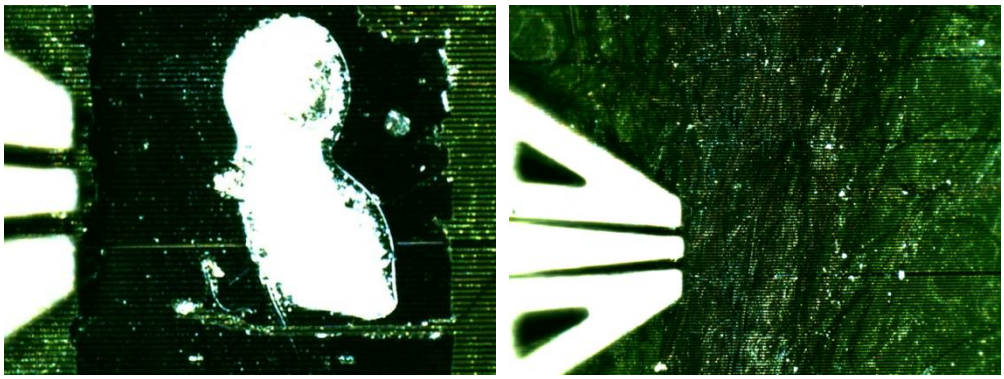
4.2.4 Destructive testing technique

Measurements across the substrate revealed that the measured parameters for the substrate changed dramatically depending on location. This non-uniformity of the substrate was likely due to the variation of the length of the gold lines across the substrate, variations in the thickness of the gold line layer and variations in the anisotropic film thickness.

To account for this variation across the substrate it was necessary to measure both the film and the substrate in the same location to obtain accurate results. To achieve this, the film and capping layer were measured together and then removed with a DC probe and the substrate was measured in the same location. This process is shown in Figure 4.10. Figure 4.10a shows the probe location

with the film and capping layer and Figure 4.10b shows the probe in the same location with the film and cap removed.

Figure 4.10b shows a significant amount of discolouration in the test area after the removal of the film. The film was then observed using a SEM and high-magnification optical microscope to verify that the film was fully removed and that the underlying gold lines were un-damaged. Figure 4.11 shows a SEM micrograph of the gold lines after removal of the film. Figure 4.11 shows that there is a small amount of debris remaining on the substrate but that the film has been removed and that the gold lines remain intact. The observations using the optical microscope confirm that the gold lines are intact.



(a) (b)

Figure 4.10: Measurement setup with: (a) silver epoxy capping layer (white), gold (green) and anisotropic film (black) and (b) with the film removed.

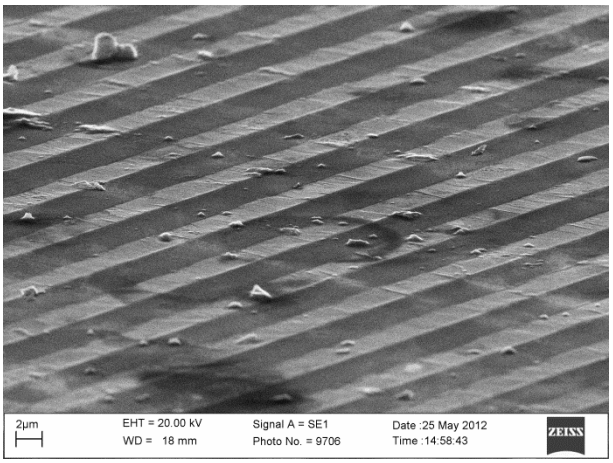


Figure 4.11: SEM image of gold lines after the GLAD film
was manually removed.

4.2.5 Film inductance extraction

An extraction model was developed based on the physical current paths shown in Figure 4.7b. The extraction model consists of generalized impedances that are re-calculated at each measurement frequency. Using frequency-dependent impedances greatly simplified the extraction process because it allowed the effect of the film to be calculated from the measurements of the total structure, the capping layer and the substrate. Since the values for each element are frequency-dependent, equivalent circuit models for the substrate and cap were not necessary.

Figure 4.12 shows the frequency-dependent circuit model. The elements shown in this model were found by tracing the current paths in Figure 4.7b. For example, for the current path through the GLAD film, the current must first pass though the film before branching into two equal current paths through the capping layer and back though the GLAD film to ground.

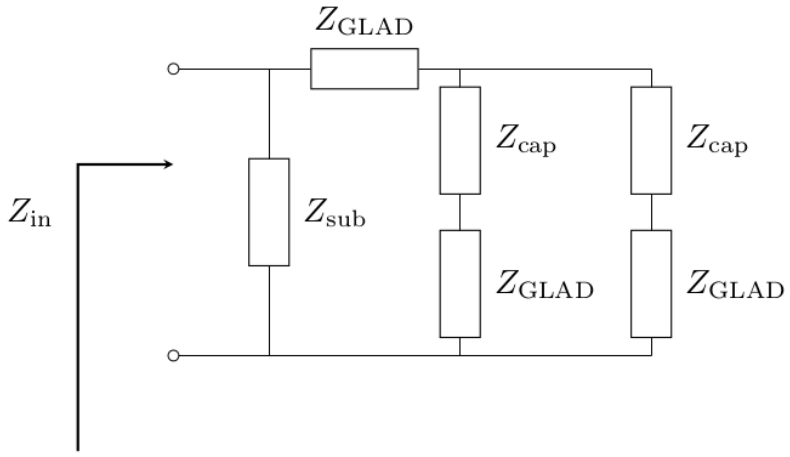


Figure 4.12: Circuit model for extraction of the GLAD film.

4.2.6 Extraction of capping layer

The total film and substrate measurements were performed as described in the above sections. The full testing measurement produced a DC resistance with near-0 reactance at low frequencies; however, measurements of the silver epoxy film deposited directly on the substrate produced an open-circuit response at low frequencies. This resistance was reduced at higher frequencies due to capacitive coupling between the epoxy and the film.

In order to fully extract the inductance of the film from the capping layer, an equivalent model was simulated in HFSS. This model is shown in Figure 4.13. The model consists of a spherical cap of a homogeneous material with the manufacturer's specified values (ie. conductivity) for the silver

epoxy, connected to a wave port by 3 perfect conductor lines that have widths of 20 μm. The simulation uses HFSS' built-in extraction function to extract the value of only the spherical cap. The resulting impedance is then used directly as the Z_{cap} in Figure 4.13.

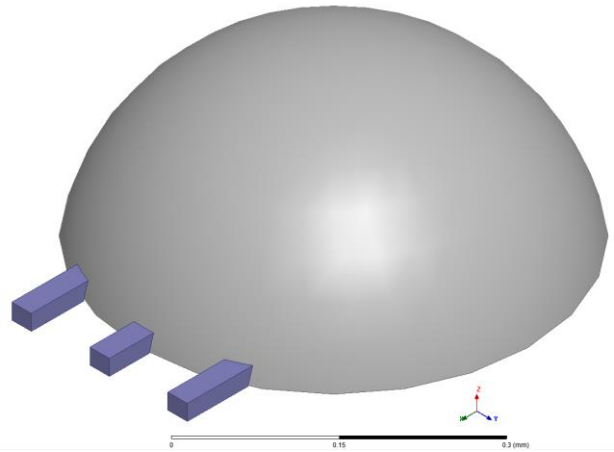


Figure 4.13: Simulation model of the silver epoxy. The blue lines on the left are the GSG probe lines which end on the surface of the silver (grey).

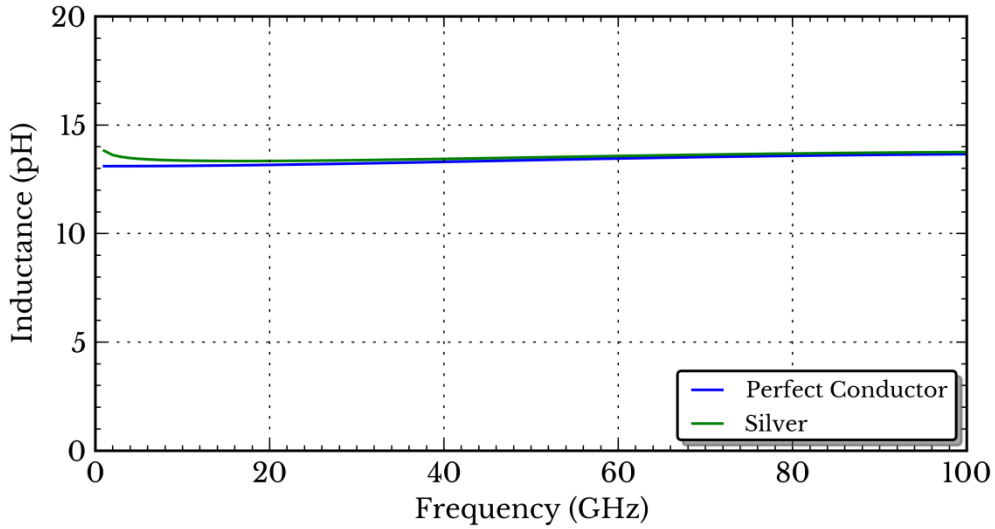


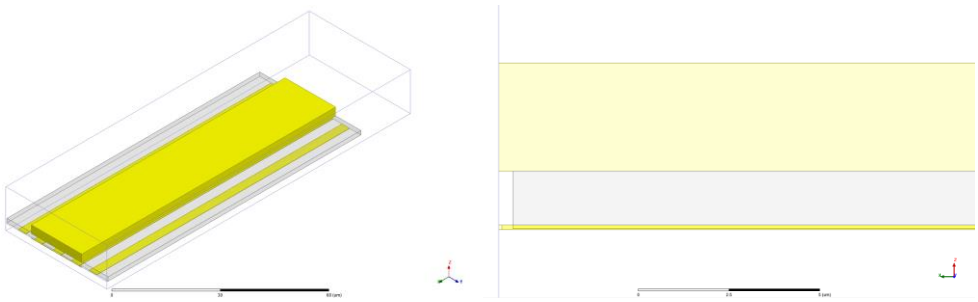
Figure 4.14: Simulated inductance of the silver epoxy.

4.2.7 HFSS simulation of test structure

Simulations of the measured structure were performed to verify the theoretical background introduced in Chapter 3: The simulation used the anisotropic film technique to model the large surface area used by the test device. To perform accurate simulations of the device, the dimensions of the test substrate and nanostructured film were accurately measured using a SEM and then modeled in HFSS.

The simulation structure is shown in Figure 4.15. Figure 4.15a shows the entire simulated structure, including the boundary. The structure consists of evenly spaced gold lines with a thickness of 100 nm, a width of 3 µm and a length of 100 µm. This length is shorter than the physical length of the lines, but is sufficient for simulation purposes due to the skin effect. On top of the gold lines is a conductive anisotropic film with a thickness equal to the GLAD film thickness. On top of the anisotropic film is a gold contact. With the addition of the top contact, the simulation structure models the performance of a current path through the film. The gold contact on top is made large to reduce the simulated resistance of the contact.

Figure 4.16 shows the port field superimposed on the model. The strong field between the signal contact (top) and the ground contacts (bottom) verifies that the main interaction in the structure is directly through the anisotropic material.



(a) (b)

Figure 4.15: One-port simulation model of the measured chip. (a) Full structure including boundary. (b) Side view of the port and layers.

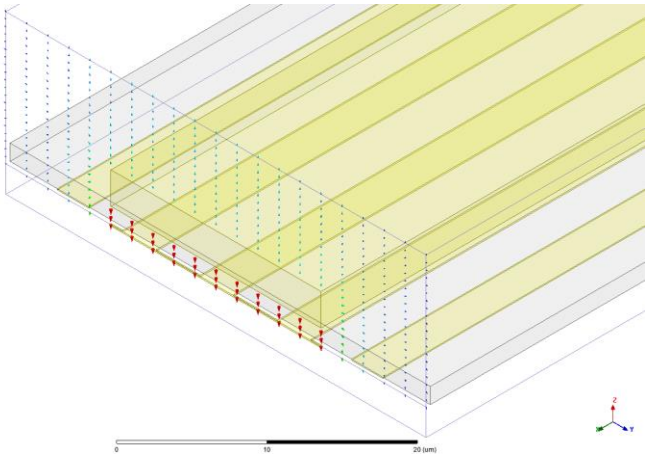


Figure 4.16: One-port model with port field visible.

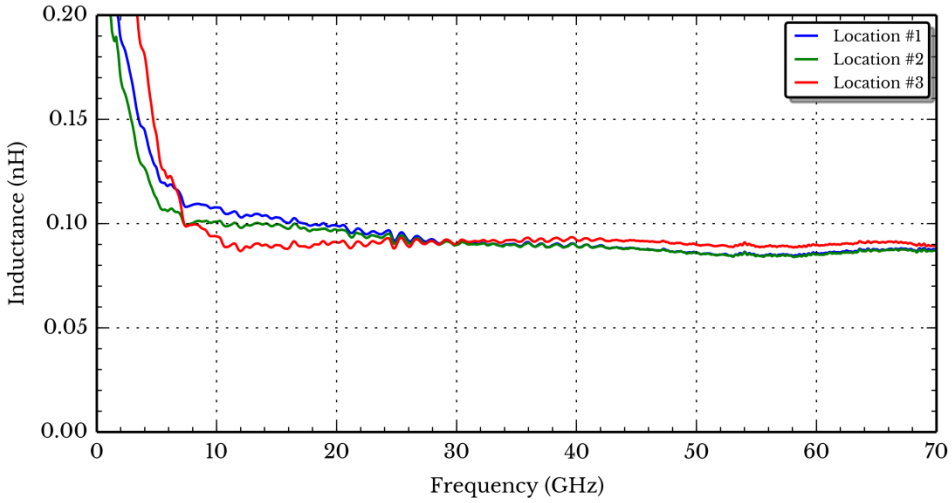
4.3 Extracted Results

4.3.1 Film simulation

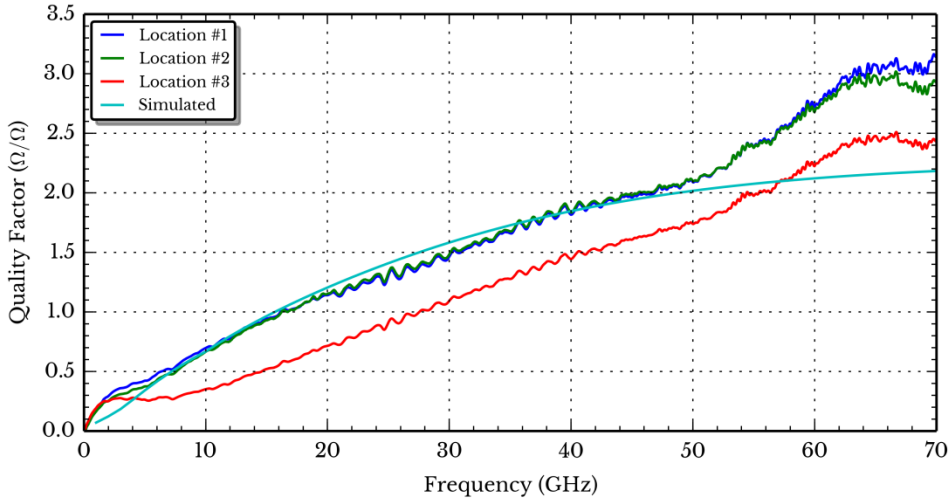
Figure 4.17 shows the fully extracted values for Z_{GLAD} in Figure 4.12. Figure 4.17 shows the inductance, resistance and quality factor of the film in three different locations. The results shown in Figure 4.17 are twice the value extracted for a single current path through the film so that it is equivalent to a full 1-port return path.

The inductance was calculated using equation 3.3 and is approximately constant in the 10 GHz to 70 GHz range. The inductance was found to be higher at low frequencies, which is likely due to the larger skin depth at those frequencies and the increased penetration of the magnetic field into the high-permeability material. Figure 4.17c shows that the resistance increases linearly over the measured frequency range; however, the resistance remains low even at very high frequencies. Finally, Figure 4.17b shows that the resulting quality factor is linear from 0 to 70 GHz, with higher quality factors in the millimetre-wave regime.

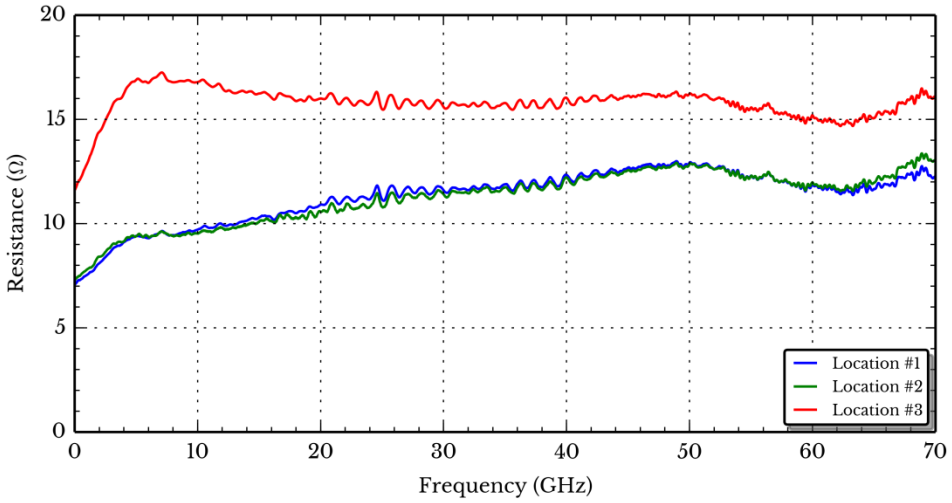
Figure 4.17b also shows the simulated structure from Figure 4.15 with a material conductivity of $75{,}000\ \mathrm{S/m}$. This model is valid for comparing the quality factor because while the model is smaller than the measured structure, the quality factor of inductors is invariant when more inductors are added in parallel; however, this is not true for inductance and resistance so these values are not compared. The quality factor from this model fits well at low frequencies; however, the simulation shows a parabolic behaviour that deviates from the measurements around 50 GHz.


Location #1
Location #2
Location #3
Inductance (nH)
Frequency (GHz)
0.00
0.05
0.10
0.15
0.20
0
10
20
30
40
50
60
70

(a)


Location #1
Location #2
Location #3
Simulated
Quality Factor (Ω/Ω)
Frequency (GHz)
0.0
0.5
1.0
1.5
2.0
2.5
3.0
3.5
0
10
20
30
40
50
60
70

(b)



(c)

Figure 4.17: Measured film inductance with return path results. (a) The inductance of a single return path. (b) The quality factor of a single return path. (c) The resistance of a single return path.

4.4 Measured Power

4.4.1 Measured Power

Microwave and RF inductors can operate at a wide variety of powers depending on their function. The function of the films presented in this chapter depend on the magnetic permeability of film which changes with large magnetic fields (or currents) [9][15]. To ensure that the inductance remains constant with power, a power measurement was performed.

The power handling characteristics of the film were measured from -30 dBm to 17 dBm. The devices were measured from 1 GHz to 75 GHz. Figure 4.18 shows the raw measured inductance for one of the devices at three frequencies (50, 60 and 70 GHz). The inductances presented in Figure 4.18 are extracted from the substrate with the same destructive technique as used in the previous sections to determine inductance. Corresponding to this technique, approximately the same inductance was measured as the previous device. In addition to the power measurement demonstrated here, this also indicates that the devices behaved in a uniform fashion. The magnetic nickel film is the only power-sensitive structure on the chip; any change in the measured inductance is due to a change in the inductive film.

The measured inductance is constant across the measured powers, with slight increases in inductance at 50 and 60 GHz at higher powers. However, the change in inductances across measured powers is small, indicating that no significant changes in magnetic performance were

observed. Overall, since the inductor shows little to no dependence on power in the range measured, the inductors can be designed to operate over a variety of powers as well as frequencies.

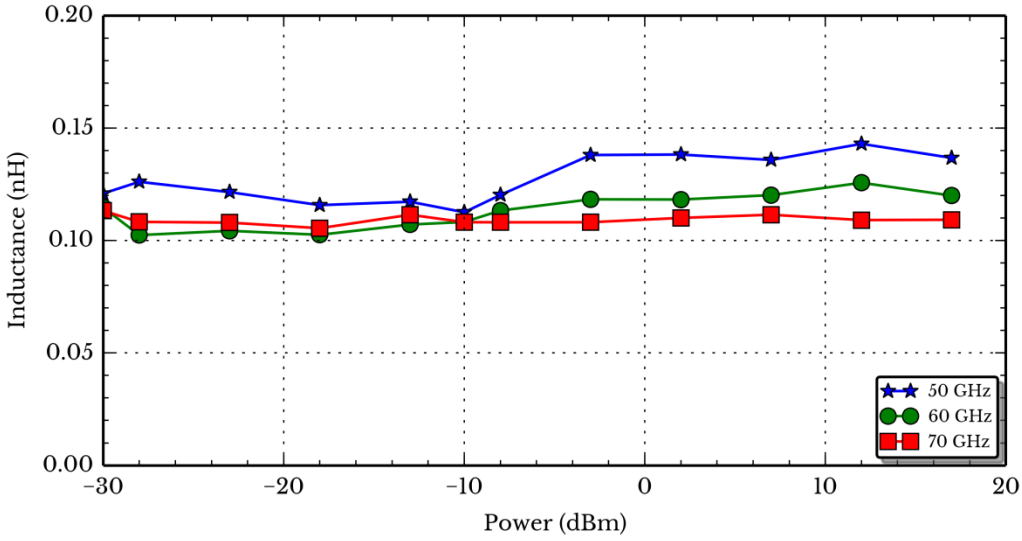


Figure 4.18: Measured inductance at 50, 60, and 70 GHz over a range of powers from -30 dBm to 17 dBm.

Chapter 5: **Thin Film Inductors Utilizing Carbon Nanotubes**

5.1 Introduction to Carbon Nanotubes

5.1.1 Introduction

This chapter introduces vertically-aligned carbon nanotube films as possible inductor structures. Carbon nanotubes have been extensively studied and experiments have demonstrated the use of CNTs as Schottky Diodes [77], super-capacitor electrodes [78], liquid sensors [79], mixers [80], and gas sensors [81]. Proposed applications of CNTs also include on-chip interconnects [82] and inductors [83]. While individual carbon nanotubes have previously been studied in the literature , this chapter will introduce the use of vertically-aligned arrays of carbon nanotubes as inductors. This chapter will build on the measurement techniques presented in the previous chapter to measure the inductance of carbon nanotubes.

5.1.2 What are carbon nanotubes?

Carbon nanotubes are molecules are fullerene carbon allotropes, meaning that they are constructed of π-bonded sheets of carbon atoms [84]. Due to the nature of the bonds in carbon nanotubes, in its pure form there are no dangling bonds and the structure is completely made out of carbon atoms [84]. Carbon nanotubes can be metallic or semiconducting materials depending on the exact way that the sheet of carbon atoms is wrapped to form the tube [84]. While the specific quantum mechanical mechanism is not important for this research, it is important to note that CNTs that are grown using chemical vapour deposition (CVD) have a 1:2 ratio of metallic to semiconducting tubes [84].

In addition to the quantum mechanical properties of carbon nanotubes, they also exhibit a large classical contact resistance. The contact resistance of a single carbon nanotube to pure silver contacts is $\rho_c = 0.020\ \Omega \cdot \text{cm}^2$ [85]. Chemical methods can be used to treat carbon nanotubes to dope carbon nanotubes, which increases their resistivity; however, despite a lowered bulk resistance, these techniques can increase the contact resistance significantly [85].

5.1.3 Quantum effects

The unique structure of CNTs means that different allotropes have different conduction band structures, resulting in some CNTs exhibiting metallic behaviour and others exhibiting semiconducting behaviour [40]. In addition to the band-structure differences, CNTs have a minimum resistance called the quantum resistance, given by equation 5.1; h is Planck's constant, and e is the electron charge. This resistance is a lumped value for a short CNT; long CNTs have additional resistance due to the finite conductivity along their length [40].

$$R_{Quantum} = \frac{h}{4e^2} = 6.45\ \text{k}\Omega \quad (5.1)$$

For carbon nanotubes that have lengths longer than the mean free path of the electrons, additional scattering resistances come into effect. The scattering resistance is a length-dependent phenomenon that is equivalent to the classical resistivities of other materials. The additional scattering resistance is given by equation 5.2 [40], where l is the length of the wire and λ_{CNT} is the mean free path of electrons in the CNT.

$$R_s = \frac{h}{4e^2}\frac{l}{\lambda_{CNT}} \quad (5.2)$$

The mean free path of a CNT can be estimated by equation 5.3, where D is the diameter of the CNT [40].

$$\lambda_{CNT} = 1000D \quad (5.3)$$

In addition to a quantum resistance, CNTs also have a quantum capacitance and inductance. These are self-capacitances and inductances that are due to the quantum mechanical nature of the conduction in a carbon nanotube. The quantum capacitance is a capacitance between quantum electron states in the CNT, however this value can be neglected because it only has a small effect on the total capacitance of a CNT [40].

Unlike quantum capacitance, quantum inductance is a significant effect in carbon nanotubes and is significantly larger than the magnetic inductance for a single tube. The kinetic inductance is due to the quantum mechanical effect of the kinetic energy of the moving electrons in a current though a carbon nanotube [40]. This means that the physical origin of kinetic (quantum) inductance is completely different than magnetic (classical) inductance and the two phenomena are not related. Despite this different origin, the kinetic inductance has an identical effect on circuit behaviour as classical inductance and can be expressed as part of a total inductance for a carbon nanotube.

The kinetic inductance for a carbon nanotube is given by equation 5.4, where h is Planck's constant, e is the electron charge and v_F is the Fermi velocity of a carbon nanotube [40]. The number of channels in a carbon nanotube varies depending on its diameter, and metallic or semiconducting structure.

$$L_{K/channel} = \frac{h}{4e^2 v_F} = 8\ \text{nH} \cdot \mu\text{m}^{-1} \quad (5.4)$$

While the kinetic inductance is significant for a single carbon nanotube, placing the CNTs in a bundle reduces the overall effect of the kinetic inductance when compared to the magnetic

inductance [40]. This reduction is due to the scaling nature of inductors; since the kinetic inductance is a particle effect, it is not affected by surrounding CNTs in the same way as magnetic inductance. The scaling behaviour for an ideal inductor is given by equation 5.5, where L_{Total} is the total inductance, L_0 is the inductance of a single device and N is the number of devices.

$$L_{Total} = \frac{L_0}{N} \qquad 5.5$$

Due to this scaling, for a 1 μm wide line, the kinetic inductance is negligible compared to the magnetic inductance for a single walled CNT and only about 10% of the overall inductance for a multi-walled CNT for a long interconnect of 500 μm [40].

5.1.4 Single walled carbon nanotube transmission line simulation

Existing circuit models for carbon nanotubes model them as distributed RLC resonators [40] or as transmission lines [60]. While large bundles have been simulated for on-chip interconnect applications [40], short vertical CNTs might be used as integrated inductors using the capping technique presented in the previous chapters.

To evaluate the performance of CNTs for on-chip interconnects, the transmission line parameters were calculated and the input impedance of a 1-port device was considered.

The important transmission line parameters are the distributed resistance and inductance along the transmission line length and the distributed conductivity and capacitance to ground [8]. With these parameters, along with the electrical length, it is possible to calculate the characteristic impedance and propagation constant of a transmission line.

The propagation constant of an arbitrary transmission line is given by equation 5.6, where α is the attenuation constant, β is the propagation constant, R is the resistance per length, L is the inductance per length, G is the conductance to ground per length and C is the capacitance to ground per length [8].

$$\gamma = \alpha + j\beta = \sqrt{(R + j\omega L)(G + j\omega C)} \qquad 5.6$$

In the CNT model, the CNT parameters are dominated by the quantum scattering, kinetic inductance and quantum capacitance, which become the values input into equation 5.6 [60]. Since a free-standing carbon nanotube is considered, the conductance to ground is negligible and set to 0. Similarly, the electric capacitance is considered to be small and also set to 0. The quantum capacitance, however, represents the energy required to insert an electron into the CNT at the Fermi-level and so remains a capacitance to ground to represent this energy [40][60].

From the propagation constant in equation 5.6, the wavelength can be calculated by equation 5.7, where λ is the wavelength in meters [8].

$$\lambda = \frac{2\pi}{\beta} \tag{5.7}$$

The wavelength for a SWCNT with multiple diameters is shown in Figure 5.1. The CNT length shown in Figure 5.1 is 20 μm, which is the approximate length that was fabricated and discussed in the following sections. The SWCNT exhibits an extraordinarily short wavelength such that the CNT is always a distributed element at GHz frequencies.

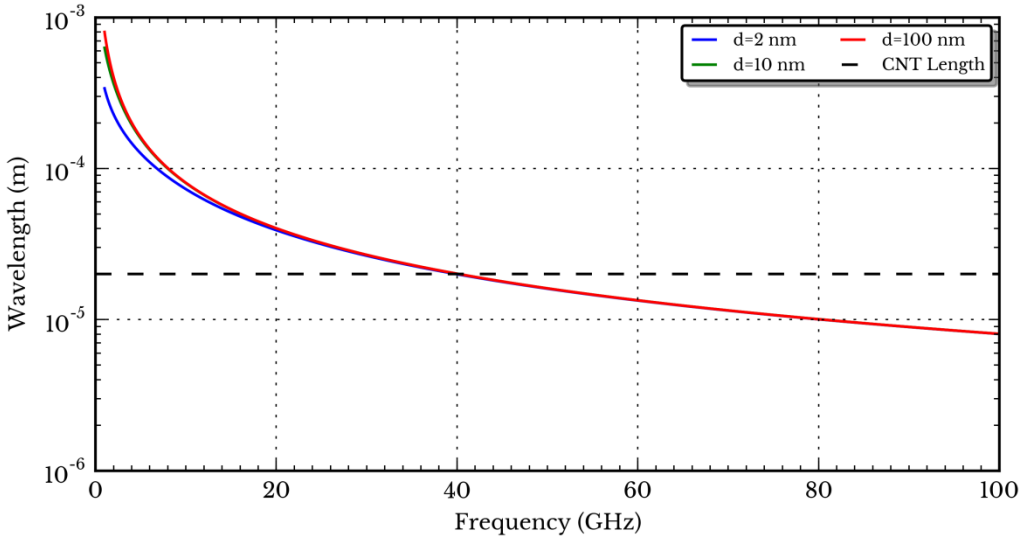


Figure 5.1: Wavelength of a SWCNT of varying diameters and 20 um in length. As the frequency increases, the CNT length becomes close to the wavelength and the CNT length is equal to the wavelength around 40 GHz. This ultra-short wavelength for a CNT transmission line causes even short CNT devices to act as distributed elements.

The other parameter required to calculate the input impedance of a CNT transmission line is the characteristic impedance, which is given by equation [8]. Once the characteristic impedance is known, the input impedance to a loaded transmission line of a known length is given by equation 5.9.

$$Z_0 = \sqrt{\frac{R + j\omega L}{G + j\omega C}} \tag{5.8}$$

$$Z_{in} = Z_0 \frac{Z_L + Z_0 \tanh \gamma l}{Z_0 + Z_L \tanh \gamma l} \tag{5.9}$$

The quantum resistance (not including the scattering portion) can be considered to be a lumped element effect at the ends of the CNT, similar to a contact resistance [40]. However, the quantum resistance is the quantum mechanical lowest resistance of a carbon nanotube and not an actual resistance. The calculations in this section assume a perfect contact with no resistance. The quantum resistance can be separated into two parts so that half is present at one end of the CNT and the other half is present at the other end. Similarly, the magnetic inductance can also be viewed as a lumped element that is present at each end. In this case, the load impedance is equation 5.10.

$$Z_L = \frac{R_Q}{2} + \frac{L_M}{2} \tag{5.10}$$

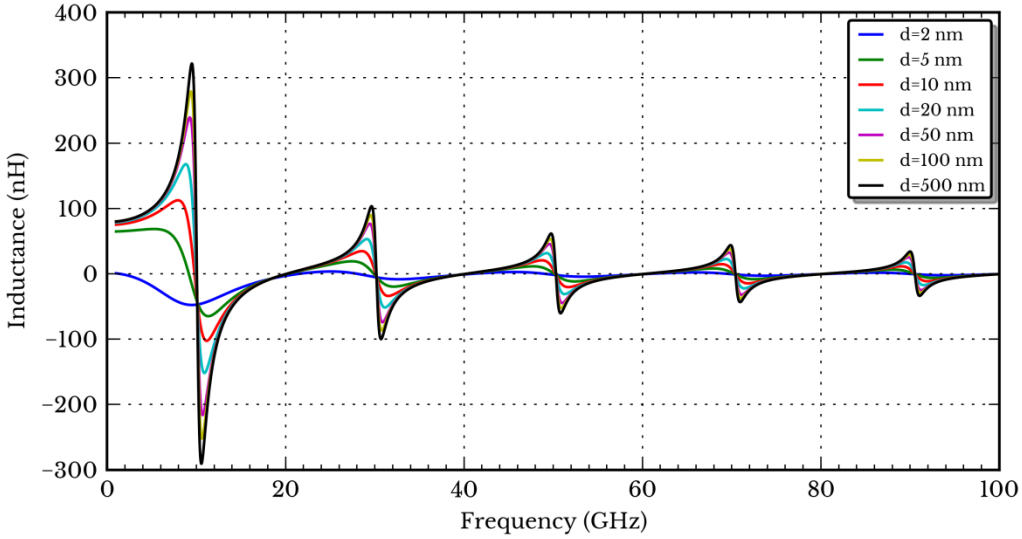
Using the load resistance from equation 5.10, the characteristic impedance from equation 5.8 and the propagation constant from 5.6, the input impedance can be calculated directly by equation 5.9. Finally, the near-end of the CNT lumped elements must be added to produce a total impedance for the CNT as given by equation

$$Z = Z_0 \frac{Z_L + Z_0 \tanh \gamma l}{Z_0 + Z_L \tanh \gamma l} + \frac{R_Q}{2} + \frac{L_M}{2} \tag{5.11}$$

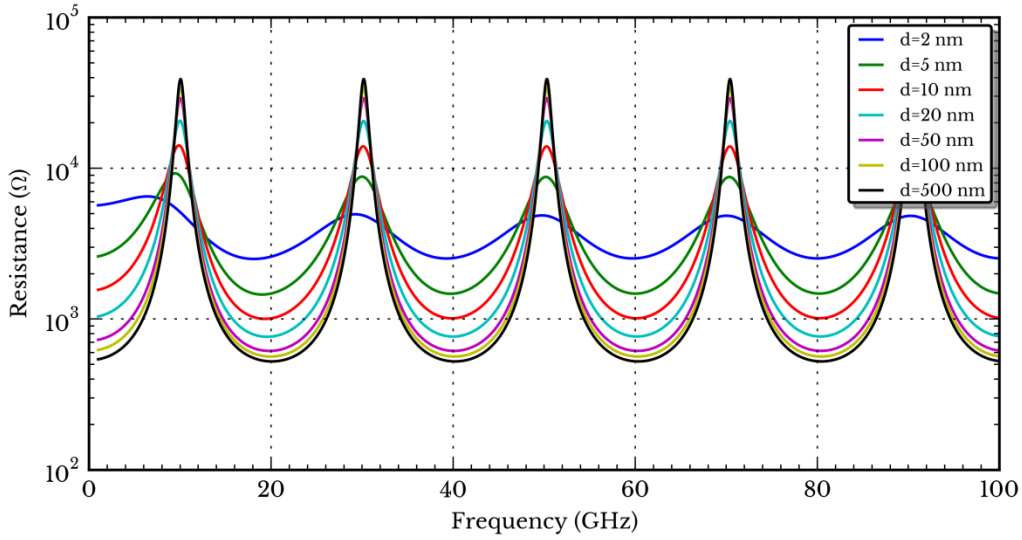
The resulting inductance is shown in Figure 5.2a. The CNT exhibits the classical input impedance for a long transmission line. The impedance switches from inductance to capacitance at the quarter wavelength frequency of 10 GHz and back again at the half-wavelength frequency of 20 GHz. Higher order modes are present with a resonance present every 20 GHz after 10 GHz (30 GHz, 50 GHz, etc.). The inductance present is extremely large, in the tens to hundreds of nanohenries, depending on frequency.

The resistance of the CNT inductor is shown in Figure 5.2b. The resonances noted in Figure 5.2a are clearly visible as resistance peaks above 10 kΩ. The lowest resistance present in the CNT inductor is approximately $500\ \Omega$, which could be reduced by lowering the length of the CNT.

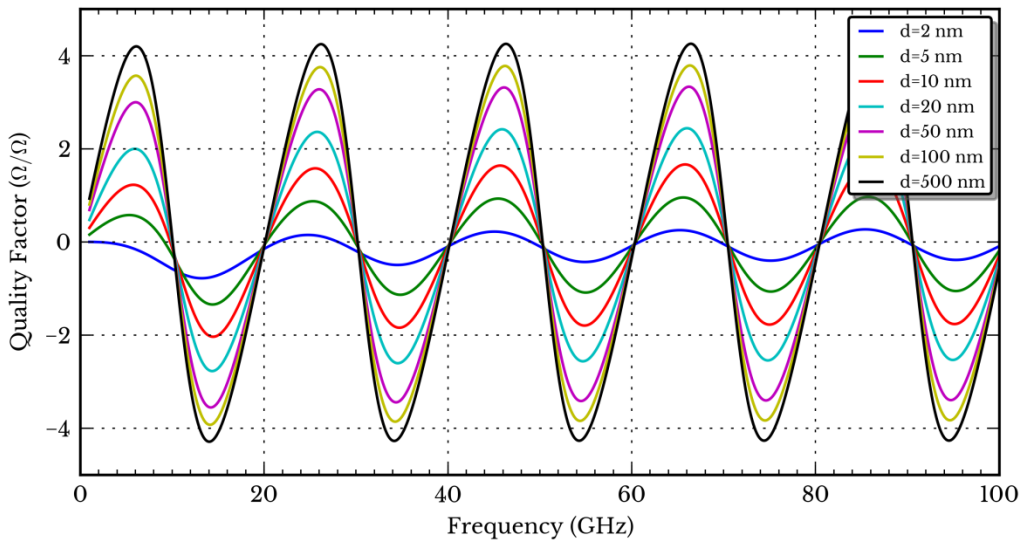
Finally, the resulting quality factor is shown in Figure 5.2c. The peak quality factor is only just above 4 for the widest CNT and only about 0.5 for a 5 nm CNT. Peaks in the quality factor occur halfway between the half-wavelength and quarter-wavelength resonances (including integer multiples of these resonances), with the quality switching between positive and negative as the frequency is increased.


Inductance (nH)
Frequency (GHz)
d=2 nm
d=5 nm
d=10 nm
d=20 nm
d=50 nm
d=100 nm
d=500 nm

(a)


Resistance (Ω)
Frequency (GHz)
d=2 nm
d=5 nm
d=10 nm
d=20 nm
d=50 nm
d=100 nm
d=500 nm

(b)



(c)

Figure 5.2: Circuit performance of a SWCNT. In all cases the CNT length was 20 μm (a) The inductance of the SWCNT using a transmission line model for the CNT. (b) The resistance of the CNT using the transmission line model, and (c) the resulting quality factor for the CNT.

The above results for a single SWCNT demonstrate enormous inductances and resistances with only low quality factors. The high impedance of a SWCNT is difficult to interface with typical 50 Ω matched networks. However, bundles of SWCNTs have dramatically reduced impedances, due to the increased number of conducting channels [40].

The analytical scaling behaviour of SWCNT bundles is shown in Figure 5.3. Multiplying the scaling factor shown in Figure 5.3 with the resistance and inductance shown in Figure 5.2 will give the total impedance of a bundle of the given area. For example, the measured device indicated in Figure 5.3 has an impedance that is approximately 10^{-5} times the impedance of a single SWCNT. This dramatically reduced impedance makes the use of SWCNTs as connecting materials feasible. Unfortunately, this scaling also reduces the effect of the quantum inductance of the SWCNT, dramatically reducing its desirability as an inductor.

Even though this analysis of CNT behaviour has been treated through analytical analysis and simulation [40][60], to the author's knowledge there has never been experimental verification of the inductance of large bundles of CNTs. A recent publication does present a measured value for the inductance of a bundle of CNTs, however, no frequency-dependent behaviour or analysis of this inductance is performed [86]. The following sections will discuss the fabrication of a CNT test-chip and the measurement results.

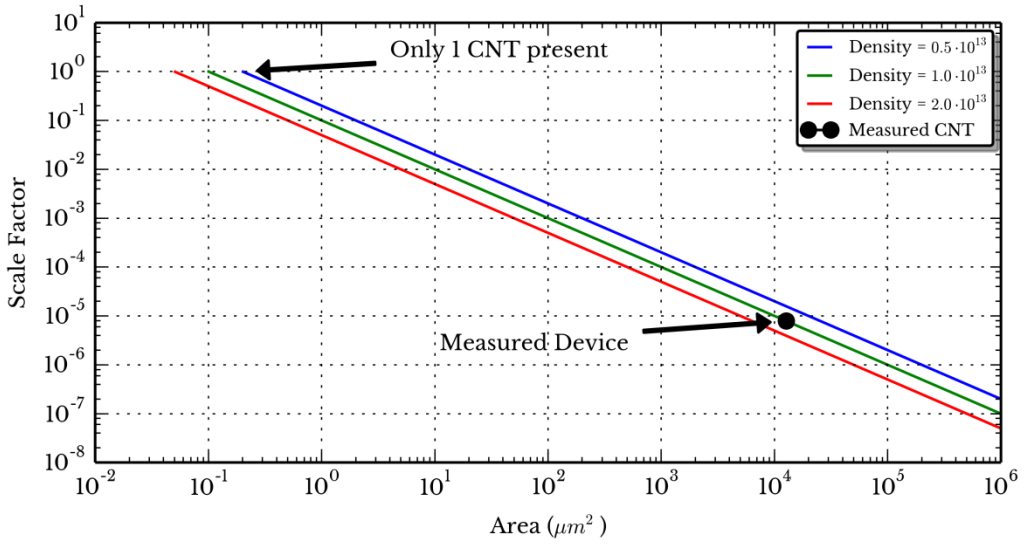


Figure 5.3: Scaling behaviour of CNT bundles by area.

5.1.5 Planar inductors composed of carbon nanotubes

Carbon nanotubes can be bundled together to form bulk materials which can be used to make on-chip interconnects [87] or classical planar inductors [88]. Replacing copper with carbon nanotubes in planar inductors has a negligible increase

5.1.6 Fabrication of carbon nanotubes

Chemical vapor deposition (CVD) can be used to grow aligned CNT arrays in parallel [61][89]. The CVD growth method utilizes a high temperature reaction between a catalyst and methane gas at high temperatures (1000°C) [90]. Since the carbon nanotubes only grow on the catalyst, it is possible to selectively pattern the carbon nanotubes [90]. While various catalysts exist, the most common is a pure nickel film [89].

The CNTs that were grown for this work are multi-wall, conically-shaped tubes with a hollow core. These tubes were grown using NanoLab's PECVD growth process [91].

5.2 Carbon nanotubes as inductors

5.2.1 Testing technique

To verify the utility of CNTs for use as on-chip inductors, test devices were designed and fabricated. The testing technique used was the same as described in Section 4.2 : test devices were designed and CNTs were fabricated in an integrated, vertical structure. The structure was then capped with a conductive silver epoxy and the S-parameters were measured. From the S-parameters the inductance, resistance and quality factor were calculated.

5.2.2 Test substrate design

The primary test devices for carbon nanotube testing are shown in Figure 5.4. The basic structure is a 2-port device with terminals suitable for Cascade's Z-Probe (100) probes. To fully extract the parasitic and substrate effects, the CNT test device (right) was accompanied by a through (left) and a bare device (centre). The measurements of these two devices were used to de-embed the device characteristics to the carbon nanotube interface. The CNT test device is shown on the right and it has a gap between both the gold and the catalyst layer.

The test substrate contained an array of devices with varying gaps between the terminals. These gaps were placed on the substrate to ensure that a device was available with a usable gap (ie. no cross linking between the CNTs on either side).

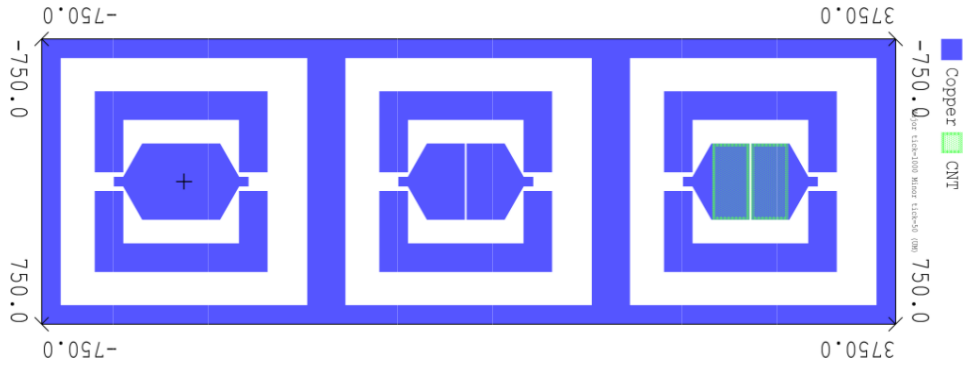


Figure 5.4: CNT test structures (short, open, CNT)

5.2.3 Test Results

The CNT PE-CVD process was performed by NanoLab Inc. on the designed substrates. Two substrates were processed with differing heights, labeled by NanoLab as 10-15 µm (designated short) and 20-30 µm (designated tall). Both devices have an estimated density of 10^9 CNTs/cm^2.

Scanning electron microscope (SEM) images were taken of the resulting CNT films, as shown by Figure 5.5. Figure 5.5 shows the near-perfect selectivity between CNT growth areas with patterned nickel and the non-growth areas that contain no nickel. The height of the CNTs is around 20 µm and they stand rigid without support from the surrounding devices. Due to their rigidity, there is a clean separation between CNT features.

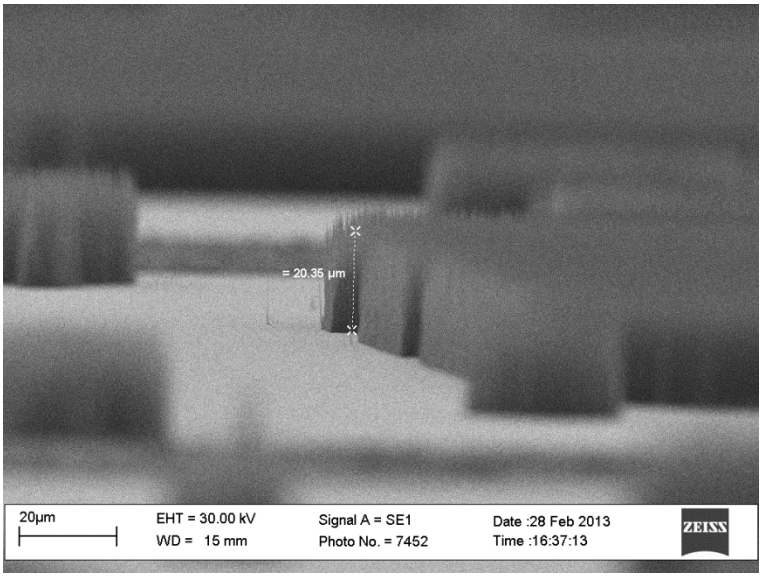
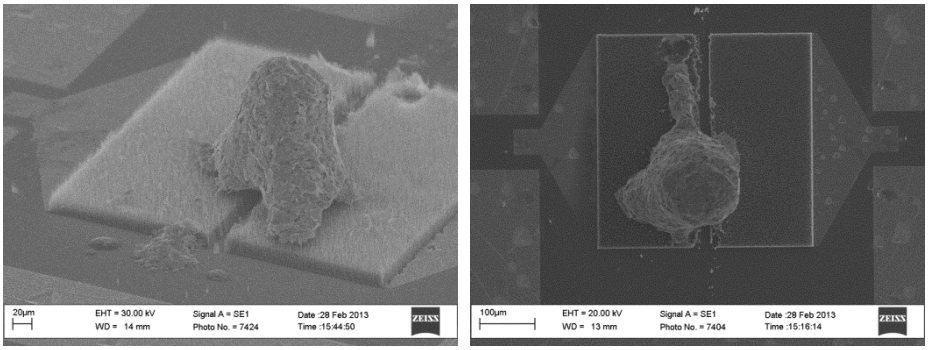


Figure 5.5: Carbon nanotube growth on substrate.

The testing procedure for the CNT devices was identical to the GLAD testing procedure outlined in section 4.2 the device was measured as-is with the CNTs and then silver epoxy was deposited on top of the CNTs and the measurements were repeated. This technique, in addition to the other on-chip testing devices allows for a full extraction of all device parasitics from the CNT results.

Figure 5.6 shows two devices with silver expoxy deposited on top. The silver epoxy adhered poorly to the CNT films, creating the predominantly vertical epoxy structures. Figure 5.7 shows a close-up of the interface between the silver epoxy and the CNTs. The tops of the CNTs are connected to the epoxy and the epoxy is sitting on top of the CNT film with no visible deformaiton or indentation of the film. The integrity of the film is important because it verifies that the RF measurements of the film are measuring the performance of the devices and not a direct connection between the underlying metal and the epoxy. As well, the interface between the epoxy and the CNTs is important because it determines the overall performance of the device.

Figure 5.8 shows the gap between the two CNT device layers in the 2-port test device. This image shows that the silver epoxy did not penetrate the gap between the two layers. This ensures that the devices are not shorted by a connection between the silver epoxy and the underlying metal layers.



(a) (b)

Figure 5.6: Two-port CNT test device with silver epoxy cap.

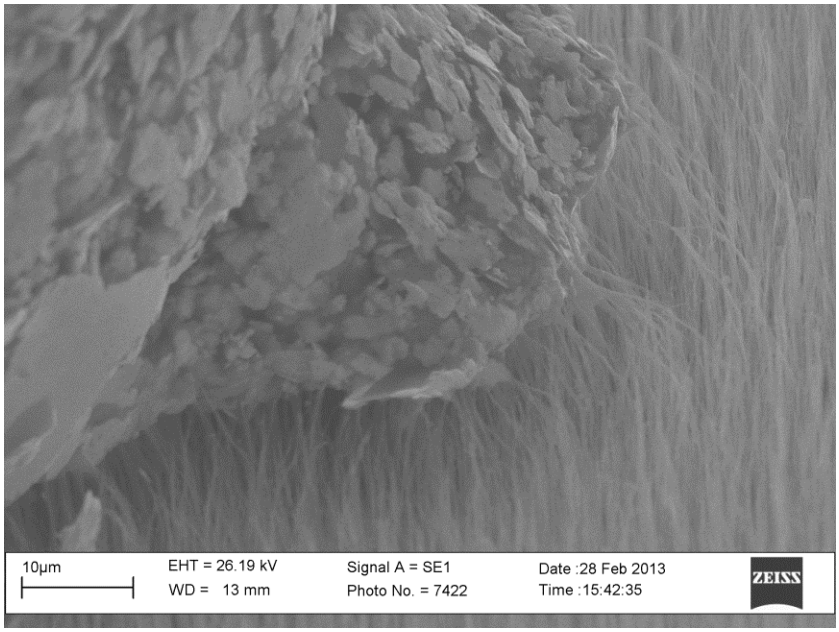


Figure 5.7: CNT adhesion to silver epoxy.

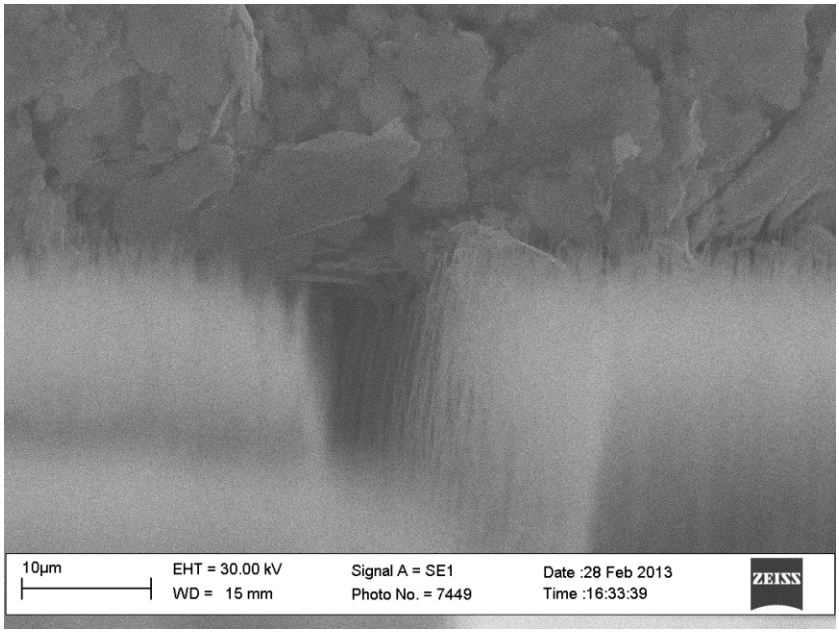


Figure 5.8: Epoxy bridge over CNT gap. The integrity of the gap between the CNTs as well as the structure of the CNTs under the silver epoxy is clearly visible.

Once the structure was validated by SEM measuments, it was measured using a 2-port VNA setup, similar to the test setup for the GLAD films. The 2-port setup required a slightly more involved extraction method than the 1-port model. To extract the result of the CNTs, it was necessary to start from a generic 2-port model.

The π-model was chosen as the generic 2-port model because it has a single through element, shown in Figure 5.9a (Z_3). This element ignores losses to ground through the substrate, which are not the object of this study. This model is convenient because the value of Z_3 is readily calulable from the measured ABCD parameters of the circuit. Specifically, the relation is given by equation 5.12. The ABCD parameters of a 2-port circuit are simple to calculate from the measured S-parameters using well-known relations [8].

$$Z_3 = B \tag{5.12}$$

Once the value for Z_3 was extracted, a physically-based model was assumed for the sub-network, shown in Figure 5.9b. From the left-hand side to the right-hand side, there is a resistance expected from the gold lines on the substrate ($R_{SubLine}$). The gap at the centre of the device will have some capacitance (C_{gap}) and a possible resistance (R_{gap}). The vertical branch in Figure 5.9 contains the total resistance (contact and per-length) of the CNT as well as the inductance of the CNT. The vertical branches are connected together with the silver epoxy, which also has an associated

resistance and inductance. Finally, a reduced model that combines duplicate elements is shown in Figure 5.9c.

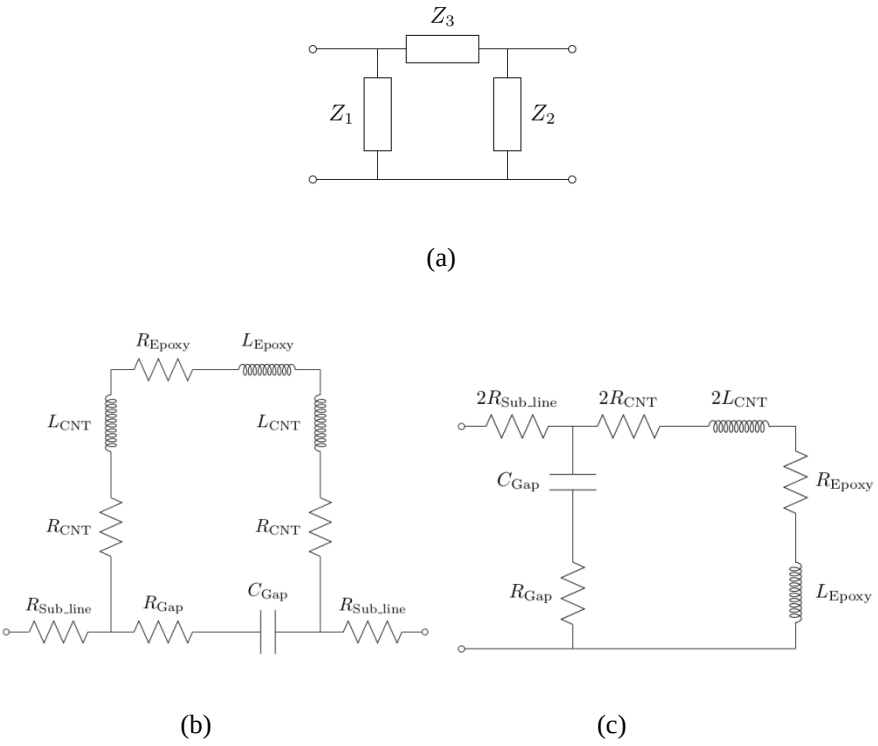


Figure 5.9: Circuit extraction models. (a) The generic $\boldsymbol{\pi}$-model for a 2-port network. (b) An expanded model for $\boldsymbol{Z_3}$ from (a), including the capacitance of the gap and the resistance of the gold connecting traces. (c) The same model as shown in (b), with duplicate elements combined.

Using the circuit model shown in Figure 5.9c, the resistance and inductance of the CNT devices was extracted. The resulting extracted impedance of the measured devices was extremely high (kΩ). DC measurements of the device gave varying results, but were also typically in the kΩ range. Since carbon nanotubes have a high intrinsic conductivity, the large resistance is due to the contact resistance. The highest contact resistance is likely present in the connection between the silver epoxy and the carbon nanotubes. The poor physical adhesion of the silver epoxy on the CNTs is likely a strong contributing factor to the high contact resistance. Further testing indicates that the contact resistance between the epoxy and a variety of other materials (including gold) is quite high.

Since CNTs can't be capped as simply as nanostructured films created using the GLAD technique, further processing using different materials would be required to cap the CNTs. The additional

steps to fabricate CNT devices and the resulting high contact resistance means that small integrated CNT inductors are not currently feasable.

5.3 Summary

5.3.1 Quantum Materials

CNTs are unique materials in that they have material properties that are directly dependent on quantum mechanical properties of lower-dimensional structures. These properties give CNTs theoretical advantages in many potential application areas. However, despite these theoretical advantages, practical CNT devices have proven difficult to realize. Key challenges to applications include the mix of metallic and semiconducting tubes in bulk material and the high contact resistance of CNTs to themselves and other materials. Also, CNT devices are difficult to integrate with silicon-based CMOS devices due to the high temperatures required in their fabrication.

5.3.2 Measurement Results

The CNT devices presented in this chapter suffered from high contact resistances, in the range of kΩ, which prevented accurate measurement of their impedance and is too high to integrate usefully in microwave devices. The contact resistance was confirmed by DC measurements in addition to RF measurements.

Overall, the CNT inductor devices perform poorly when compared to the GLAD-based films. Due to the high contact resistance, CNT inductors have practical limits on their quality factor which are not present in ferrometallic films. In addition, CNT devices are more difficult to manufacture than GLAD films and they require higher thermal budgets, which limits their usefulness in integrated CMOS devices. While the CNTs have theoretical advantages over modern planar inductors in terms of their quantum inductance, this inductance is not realizable until the issue of contact resistance is resolved.

Chapter 6: **Conclusion**

6.1 Thin films as Inductors

6.1.1 Summary

This thesis studied novel structures and materials for applications as integrated, on-chip inductors. The electromagnetic performance of the inductor devices was simulated and the devices were fabricated and directly measured.

Chapter 2 provided an introduction to the physical meaning of inductance and its application to RF circuits. Inductance is derived from Maxwell's equations and shown to be a direct consequence of the magnetic field produced by a current. The permeability of magnetic materials was introduced and discussed with application to inductors. Chapter 2 then introduces the partial inductance method for calculating the inductance of arbitrary structures. The specific case of the partial inductance of a straight wire in free space is discussed as a starting point for the analysis of physical inductors and is re-visited in Chapter 3. Chapter 2 ends by discussing the current state of the art in on-chip inductor technology and proposes technologies to study for on-chip inductor applications.

Chapter 3 begins with a definition of the structures of interest for this thesis. The simulations for a single nano-scale helix are presented and the inductance is shown to be highly dependent on material parameters. Specifically, magnetic materials were found to produce the best inductance and quality factors of all the simulated materials. Because of the array-nature of the nano-scale structures, the helix simulation is expanded upon by analyzing the effect of the material surrounding the helix. The surrounding material was also shown to have a significant impact on the performance of the helix; once again, magnetic materials greatly improved the performance of the helix. The effects of both conductivity and permeability were considered for the simulations presented including a study on the effect of anisotropic conductivities in the surrounding medium on the expected performance of the structure. It was found that anisotropic materials greatly reduced the eddy currents that limit the performance of classical magnetic materials in the RF and microwave frequency domains. Chapter 3 ends with a study on the scaling behaviour of the nano-scale inductors, showing that the active area in high permeability, anisotropic materials is quite small, theoretically producing extremely high inductances realizable in a given area.

Chapter 4 introduces the glancing angle deposition (GLAD) technique as one method of creating on-chip vertically-aligned nanostructures. Using the GLAD technique, nanostructures made of nickel were produced. Nickel was chosen due to its high conductivity and high permeability. The

nickel films demonstrated good inductive and quality-factor performance up to 110 GHz, with possible performance improvements above this frequency. The highest observed quality factor for these films was shown to be approximately 3 and an inductance around 0.1 nH, demonstrating that these films do perform as inductors. The estimated area consumed by these inductors is in the square microns, which is several orders of magnitude better than commercial planar inductors. This small area allows for these inductors to be cascaded, i.e. connected in series, to make large-inductance inductors.

Chapter 5 discusses the use of carbon nanotubes as inductive elements, similar to the GLAD structures demonstrated in chapter 4. CNT inductors have a number of fabrication-related drawbacks, including their need to be grown on specific materials and conductive substrates or at high temperatures. CNTs are interesting for on-chip applications due to their high conductivity and their quantum mechanical inductance, called the kinetic inductance. This kinetic inductance can be a significant portion of the total inductance of a CNT device in certain circumstances.

To test CNT devices, a test chip was designed and built. CNT-based inductor implementations suffer from a high contact resistance that was also observed in this work. Despite the high contact resistance, theoretically the CNTs produced a useful quality factor, indicating that if the contact resistance can be reduced, then CNTs may be a candidate for on-chip integrated inductors. The fabrication method utilized here demonstrates a controllable growth pattern that can be easily implemented with existing fabrication technologies. Once the CNT contact issue has been solved, this method can be used to create vertical CNT devices on-chip.

Altogether, this thesis introduces the formal definitions and theory of inductance and proposes new devices to overcome problems with existing on-chip inductor implementations. Two specific materials were used to create devices to test the theoretical performance of the proposed vertically-aligned structure. The magnetic materials produced through GLAD demonstrated promising qualities and is a candidate for future research. The carbon nanotube devices fabricated here suffered from high contact resistance that will need to be overcome before CNTs can be usefully integrated into on-chip devices.

6.2 Highlighted contributions

The following list highlights some of the achievements documented in this thesis.

- High-pitch (non-ideal) helices
    - Determined that the inductance of high-pitch helices is primarily dependent on the permeability of the wire material and permeability of the surrounding material.

- The surrounding material was found to contribute significantly to the total inductance of the structure. Simulated results determined that a nickel material ($\mu_r = 600$) increases the total inductance an order of magnitude.
- Determined that using an anisotropic surrounding medium greatly increases the overall inductance.

- Magnetic thin films
  - Measured the inductance and quality factor to demonstrate a proof of concept vertical inductor.
  - Determined that the measured inductance of the films is independent of power and nearly constant over wide bandwidths.
  - Demonstrated that the skin effect changes the scaling behaviour of the thin films, resulting in much higher inductance than would have otherwise been expected.
  - Demonstrated that the anisotropic nature of magnetic thin films reduces shielding effects in the material to provide a higher inductance than isotropic material.
- Carbon nanotubes
  - Designed and built CNT test devices which were measured on-chip.

6.3 Future Work

6.3.1 Nanostructured thin films

Nanostructured thin films produced through GLAD show significant promise as the inductor technology of future microwave and millimetre-wave electronics. The high inductance per area of the devices observed here were found to be strongly affected by material parameters, such as permeability. Future work should explore the use of various high-permeability materials, including composite materials such as Permalloy [92] and Mu-metal. In addition to these high-permeability film materials, nanostructured films include the possibility of using filling materials to further increase the permeability of the overall film.

Future work should also include an analysis of the advanced GLAD techniques used to create these films, including varying the nanostructure of the film to produce films of different densities, heights and coiling characteristics. These properties, especially in conjunction with filling materials may further increase the on-chip inductance and quality factor. Finally, a study on the patterning abilities of GLAD films should be conducted to produce small-area inductors with integrated capping. Once a suitable high-yield process has been perfected, the GLAD films will be ready for integration into repeatable on-chip applications.

6.3.2 Carbon nanotubes

Despite the poor experimental performance, there are a number of theoretical advantages (i.e. quantum inductance and high conductivity) of CNTs over other known materials. For this reason, the further pursuit of on-chip CNT technologies is valuable. Primary research towards CNT applications must be focused on the contact resistance problem and CMOS integration. Materials may be discovered which reduce the contact resistance between CNTs and other metallic materials. In addition to materials which have a favorable contact resistance, specific chemical bonds may allow for direct electron transport between the CNT material and external materials. Once the contact resistance problem is resolved, integration with CMOS devices must also be considered because CNT fabrication techniques require high temperatures and have significant impacts on the thermal budget. For this reason, a fabrication process that is compatible with doped-silicon transistor devices is extremely important. If the two problems of contact resistance and integration can be overcome, then CNTs hold promise in both inductor and interconnect applications.

Appendix A: Carbon Nanotube Substrate Fabrication Process

The carbon nanotube growth process used by NanoLab required a nickel seed layer separated from other device layers by a chrome adhesion layer. A gold layer was used to connect the CNT devices to the VNA probe. The full test devices were fabricated in the University of Alberta Nanofab.

A high-resistivity silicon wafer was used as the substrate. The wafer was a <111>, $1000\ \Omega \cdot \text{cm}$, 100 mm diameter from University Wafer [93].

The wafer was first cleaned with Piranha (H2S04:H2O2) and then a layer of chrome (50 nm) and a layer of gold (200 nm) was sputtered onto the substrate (Figure A.1a). The gold and chrome layers were then patterned by contact photolithography.

HPR504 photoresist was used as the photoactive layer. Approximately 5 mL of photoresist was spun on with a two-step spin: first the photoresist was spread at 500 RPM for 10 seconds and then it was spun at 4.00 kRPM for 40 seconds to obtain an even spread. The photoresist was then baked in a Solitec vacuum oven at $115℃$ for 120 seconds. The substrates were then cooled to room temperature over 15 minutes.

The pattern was transferred using an ABM contact-mode mask aligner with peaks at 405 and 365 nm wavelengths. The substrate was exposed for 2.7 seconds and then developed for 25 seconds in Microposit 351 developer.

After development, the substrate was dipped into gold etch for approximately 10 seconds until the gold visibly removed. Following the etch, the wafer was washed with de-ionized water and dried with nitrogen. The substrate was then dipped into chrome etch, followed by a wash and dry. After the gold and chrome layers were patterned, the remaining photoresist was stripped by rinsing the wafer in acetone and the wafer was washed with DI water and dried. The substrate is shown in Figure A.1b after the photoresist is removed.

The carbon nanotube seed layer was patterned by lift-off to ensure that the nickel layer was uncontaminated by photoresist or etchants. HPR504 photoresist was used as the lift-off layer. Photolithography was performed using the second mask and the same process as outlined above. After development, the photoresist was hard baked for 2 minutes at $130℃$.

After the hard bake, a 100 rm layer of chrome was sputtered onto the substrate, followed by 32 nm of nickel. The wafer with photoresist and seed layer is shown in Figure A.1c. To lift-off the unwanted material, the wafer was placed in an acetone bath and sonicated for 15 minutes. After the sonication, the wafer was washed with clean acetone, isopropyl alcohol (IPA), DI water and then dried. The substrate cross-section is shown in Figure A.1d.

The substrate was then diced and shipped to NanoLab [94] for carbon nanotube growth. The carbon nanotubes were grown with NanoLab's plasma-enhanced chemical vapour deposition (PECVD) process. The final substrate with carbon nanotubes is shown in Figure A.1d.

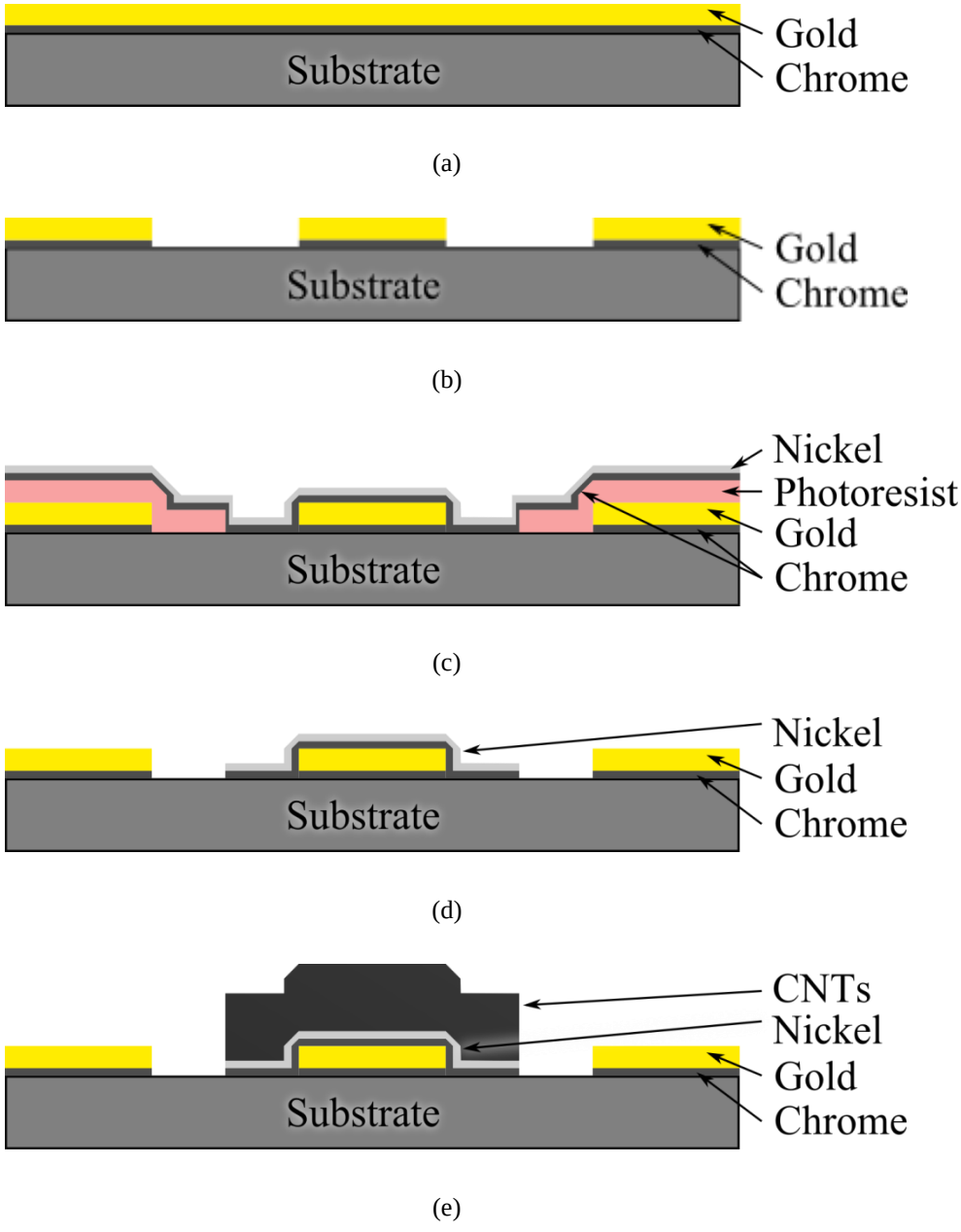


Figure A.1: Process flow for the carbon nanotube test substrate showing cross-sections at key process steps.

Appendix B: Definition of a Helix

A classical inductor structure is an ideal helix. A helix is mathematically described by the set of parametric equations in equation B.1 [95] and shown in Figure B.1.

$$\begin{aligned} x(t) &= A\cos(\omega t) \\ y(t) &= A\sin(\omega t) \\ z(t) &= Bt \end{aligned} \qquad \text{B.1}$$

Where t is the parametric parameter, A is the radius of the helix, ω is the angular frequency of the coil with respect to t, and B is the height of the helix with respect to t. Equation B.1 describes a curve through 3D space that extends to infinity in the z-axis, but is bounded by the distance $|x|, |y| < A$ in the x-y plane as shown in Figure B.1.

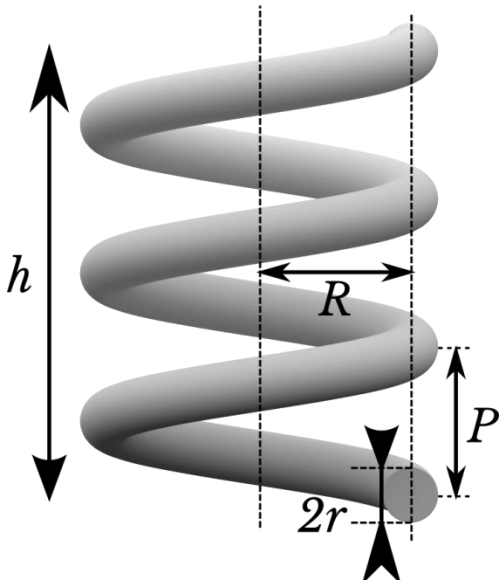


Figure B.1: Parameters of a helix; h is the helix height, R is the helix radius, r is the radius of the wire, and P is the helix pitch.

To describe helices, it is more convenient to use the parameters of helix height (h), radius (R) and pitch (P) than the parameters in equation B.1. The pitch of a helix is defined as the vertical distance between two adjacent turns of the helix [67]. These parameters are shown in Figure B.1.

If the parametric parameter is assumed to start at 0, then the height of the helix is given directly by z. By making the substitution $B = 1$, the parametric parameter becomes the height of the helix. Substituting for the value of t and noting that A is equal to the radius of the helix results in equation B.2.

$$x(h) = R\cos(\omega h) \qquad \text{B.2}$$

$$y(h) = R\sin(\omega h)$$

Next, the period of the sinusoid determines the pitch of the helix (P) or the *number of turns per length* (T) as shown in (B.3).

$$\omega = \frac{2\pi}{P} = 2\pi T \tag{B.3}$$

The units of the pitch and the number of turns per length are dependent on the units of h, eg. if h is the height in micrometers then T is the number of turns per micrometer.

For comparison of the inductance of a helix against an equivalent wire, it is useful to know the length of wire that constitutes the helix. The length of the wire is a line integral over the helix height as shown in equation B.4.

Expanding the derivatives by substituting in equation B.2 gives equation B.5, which simplifies to equation B.6. Integrating equation B.6 and substituting the relations for ω and t gives equation 3.5, which is the final relation between the wire length, helix radius, turns-per-height and height properties.

$$l_{wire} = \int_C \sqrt{\left(\frac{dx}{dt}\right)^2 + \left(\frac{dy}{dt}\right)^2 + \left(\frac{dz}{dt}\right)^2}\, dt \tag{B.4}$$

$$= \int_0^t \sqrt{(-R\omega\sin(\omega t))^2 + (R\omega\cos(\omega t))^2 + B^2}\, dt \tag{B.5}$$

$$= \int_0^t \sqrt{(R\omega)^2 + 1}\, dt \tag{B.6}$$

$$\therefore\ l_{wire} = h\sqrt{(2\pi RT)^2 + 1} \tag{B.7}$$

Appendix C: HFSS Simulation Details

The HFSS helix models shown in Figure 3.3 were modeled with a low number of polygon sections. This was done to reduce the computer resources required to simulate the structures. The parameters used in HFSS to describe the discretization of the model were *cross section polygons* and *sections per turn*. Cross section polygons is the number of polygons around the circumference of a single section of wire. The parameter *sections per turn* is the number of polygon sets around one turn of the helix. Together, these two parameters control the resolution of the inductor model.

Larger numbers of polygons, as determined by sections per turn and cross-section polygons, are desirable because they increase the accuracy of the simulation model. However, high resolution models (large numbers of polygons) require long simulation times and large amounts of random access memory (RAM) so the values were kept low. The models shown in Figure 3.3 have a cross-section polygon count of 10 and 20 sections per turn. These values produced a visibly accurate model that could be simulated quickly.

All of the HFSS simulation models presented in this thesis were simulated with radiation boundary conditions, which is a type of absorbing boundary condition. All of the models were stimulated with a wave port excitation with a solution frequency set to the highest frequency simulated. HFSS uses the solution frequency during its mesh creation step. Using the highest solution frequency generally resulted in the finest mesh and the most accurate results.

Appendix D: Microwave.py

Analysis of measured results in this thesis was performed using a small collection of useful functions created for this work. The functions were written in the Python programming language due to its robust and increasingly comprehensive libraries for scientific numerical analysis and plotting [96].

The benefit of using a programming language for data extraction is that the extraction process is repeatable and each step can be separated from the process and verified separately. A typical extraction routine is shown in the code below:

```
from microwave.vna import read_data
from microwave.data import *

S_Parameters = read_data('File_Name.csv')
ABCD = S_to_ABCD(S_Parameters)
Z3 = ABCD[:,1]
```

This code first reads the S-parameters saved by an Agilent VNA into an array structure, converts the S-parameters to ABCD parameters and extracts the B parameter from the ABCD parameters as the through element from a 2-port represented by the pi model.

Using the simple extraction methodology above, an arbitrary 2-port pi-model circuit was defined and then extracted. Figure 5.9a shows the generic pi-model and the specific functions chosen for the elements Z_1, Z_2, and Z_3 are given in equations D1, D2, and D3. These functions were chosen as arbitrary values that were non-linear and produced complicated S-parameters.

$$Z_1 = 100 + 25\sin\left(\frac{f}{10^9}\right) + j\left(\omega L_1 - \frac{1}{\omega C_1}\right)$$
$$L_1 = 40\ \text{pH}$$
$$C_1 = 60\ \text{pF} \qquad \text{D1}$$

$$Z_2 = 75 - \frac{(f - 50\times 10^9)^2}{5\times 10^9} \qquad \text{D2}$$

$$Z_3 = 10 + j\omega(0.5\ \text{nH}) \qquad \text{D3}$$

The S-parameters for the 2-port model were calculated and saved into a text file. The file was then loaded using the above script, the S-parameters were converted to ABCD parameters and the

element values were extracted using equation D4. The real and imaginary parts of the impedance are plotted in Figure D.1 and are exact matches within numerical precision.

$$Z_1 = \frac{A-1}{C}$$
$$Z_2 = \frac{D-1}{C} \qquad \text{D4}$$
$$Z_3 = \frac{1}{C}$$

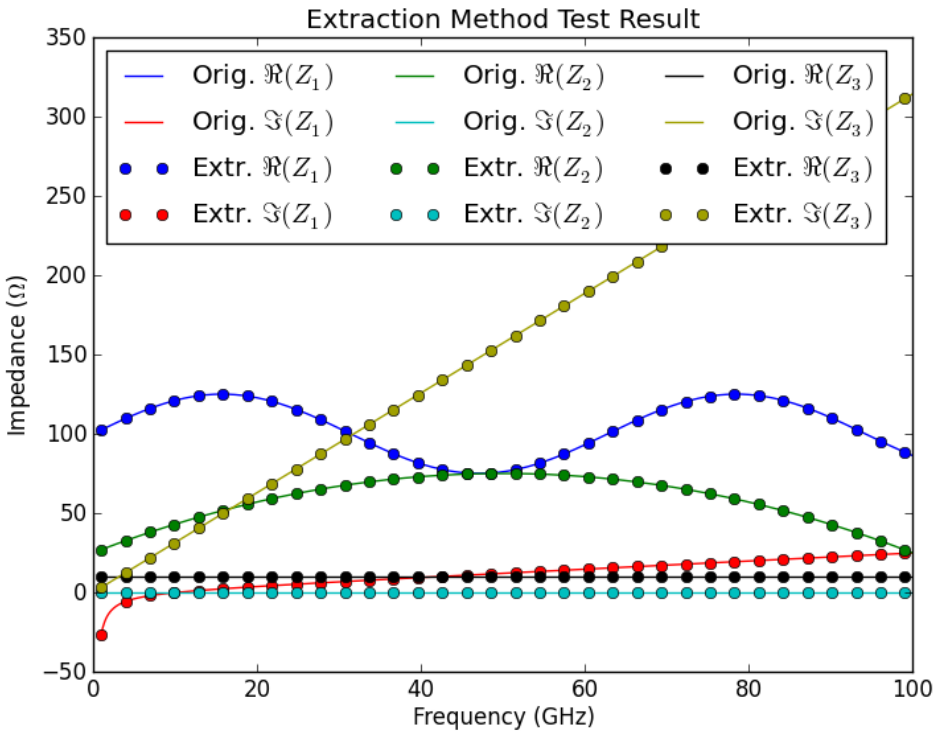


Figure D.1: Extracted impedance values for an arbitrary 2-port pi-model circuit plotted along the analytical values. The extraction process produced an exact match for the extracted devices.

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