Power Engineering Letters

Impact of DG Interface Controls on the Sandia Frequency Shift Antiislanding Method

Xiaoyu Wang, Walmir Freitas, Wilsun Xu, and Venkata Dinavahi

***Abstract*—This paper investigates the impact of two types of inverter-based distributed generation (DG) interface controllers on the Sandia frequency shift (SFS) antiislanding method. The antiislanding detection performance of the constant power-controlled DG and the constant-current controlled DG are compared and analyzed when the inverters are equipped with the SFS scheme. The comparison results show that the power regulator of the constant power-controller can degrade the SFS efficiency.**

***Index Terms*—Distributed generation (DG), inverter, islanding, positive feedback.**

I. Introduction

INVERTER-BASED distributed generation (DG) is commonly connected to the secondary distribution system due to its relatively small size. The inverter is actually an interface between the power system and the generator. Thus, different inverter interface control strategies may have distinctive impact on the DG operation when it is operated in grid parallel mode. The problem of the interaction between the inverter interface controls and the most commonly used DG antiislanding methods has been reported recently [1], [2].

The objective of this paper is to investigate the impact of the inverter interface controls on the antiislanding performance of the Sandia frequency shift (SFS) method for the inverter-based DG. The sensitivity of the SFS parameters to the constant power control and the constant current control is studied through dynamic simulations in Matlab/Simulink, and the islanding detection times of the SFS scheme for the two cases are compared based on the simulation results.

II. DG System Component Models

An inverter-based DG system is set up to simulate the dynamic process of the DG islanding phenomenon. The single-line diagram of the system is shown in Fig. 1 where R_0 and L_0 are the resistance and the inductance of the power system line, respectively, and L_s represents the inductance of the inverter filter. The output power of the DG is $P+jQ$, $\Delta P+j\Delta Q$ is the imbalance power between the load and the DG, and CB is the circuit breaker. The constant power controller and the constant current controller are implemented for the inverter-based DG. The structures of these two controllers can be found in [2].

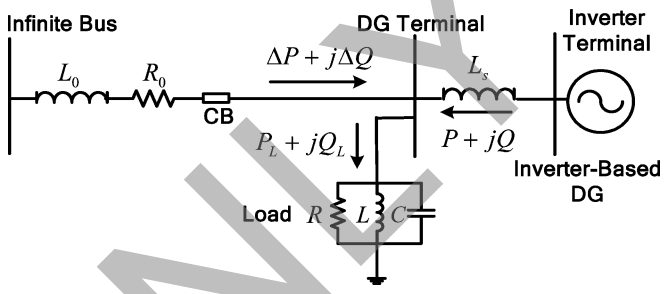

Fig. 1. Single-line diagram of an inverter-based DG system.

III. Antiislanding Scheme

The SFS scheme is a positive feedback antiislanding method that uses the deviation of frequency from normal value as the feedback signal to influence the operation of the inverter [3]. The feedback signal θ_f can be represented by

$$\theta_f = \frac{\pi}{2}\left(cf_0 + K\left(f - f_0\right)\right) \tag{1}$$

where f is the DG terminal voltage frequency, f_0 is the base frequency (60 Hz), K is the positive feedback gain of the scheme, and cf_0 is the initial chopping fraction. The SFS scheme was originally proposed to single-phase systems; however, it can readily be extended to three-phase systems. In this case, a phase angle transformation is used to realize the frequency shift, which is shown in Fig. 2 where the constant power controller is also displayed. The inverter *dq* reference currents i_{dref} and i_{qref} are obtained from the power regulator, in which P_{ref} and Q_{ref} are the inverter output active and reactive power references, respectively. Then, i_{dref} and i_{qref} are transformed to i^*_{dref} and i^*_{qref} by applying the matrix in the phase-angle transformation block. Thus, i^*_{dref} and i^*_{qref} are set as the new current references in the inverter current regulator, where v_d, v_q and i_d, i_q are the DG terminal voltages and the inverter output currents, respectively. The outputs of the current regulators v_{sd} and v_{sq} are the inverter terminal voltages. The constant current controller with the SFS control is similar to the controller shown in Fig. 2, except that there is no power regulator.

Manuscript received September 26, 2006; revised February 5, 2007. This work was supported by Natural Resources Canada through the Technology and Innovation Program as part of the Climate Action Plan for Canada. Paper no. PESL-00075-2006.

X. Wang, W. Xu, and V. Dinavahi are with the Department of Electrical and Computer Engineering, University of Alberta, Edmonton, AB T6G 2V4, Canada (e-mail: wangxy@ece.ualberta.ca; wxu@ualberta.ca; dinavahi@ece.ualberta.ca).

W. Freitas is with the Department of Electrical Energy Systems, State University of Campinas, 13083-852 Campinas, Brazil (e-mail: walmir@ieee.org).

Digital Object Identifier 10.1109/TEC.2007.902668

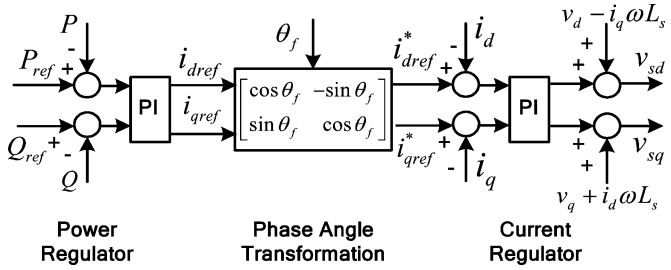

Fig. 2. Block diagram of the constant power controller equipped with the SFS scheme.

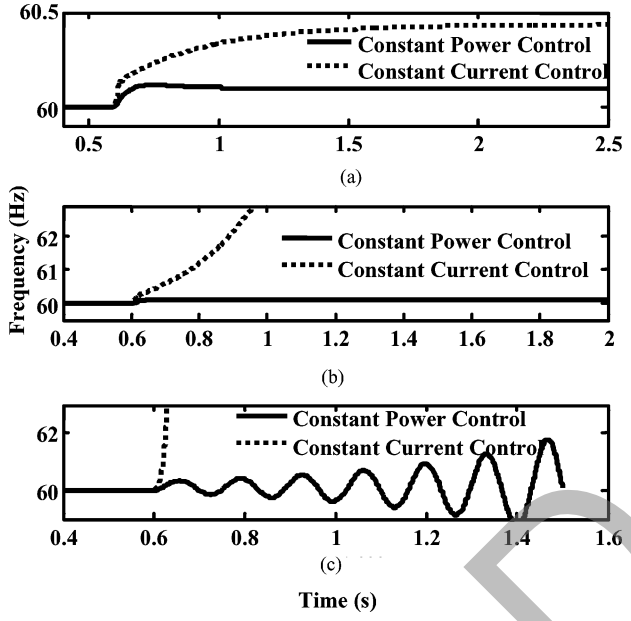

Fig. 3. Inverter voltage frequency changes for the two interface controls. (a) $K = 0.001$. (b) $K = 0.01$. (c) $K = 0.032$.

IV. Impact of the Inverter Interface Controls

The interactions between the two types of inverter interface controllers and the SFS scheme are compared through electromagnetic transient simulations. Fig. 3 shows the inverter voltage frequency before and after the islanding for the two types of inverter controllers. In the simulations, the inverter is operated at unity power factor and Δ P is zero for both the types of controllers. Consequently, the active power of the load is only supplied by the DG; the resonant frequency of the *RLC* load is set as 60.1 Hz; the load quality factor is 1.8; cf_0 is equal to 0.01; and the islanding occurs at the instant of 0.6 s. Three scenarios are presented in Fig. 3. In Fig. 3(b), K is 0.001. It is seen that for this scenario, the islanded DG system converges to a steady-state operating point for both interface controls. The inverter steady-state frequency after the islanding is 60.1 Hz for the constant power control and 60.4 Hz for the constant current control. The former frequency is the resonant frequency of the *RLC* load, and the later one is the steady-state frequency predicted by the phase criteria of the SFS scheme [3]. In Fig. 3(b), K is increased to 0.01. The steady-state frequency of the constant-power controlled inverter goes to 60.1 Hz again after the islanding, whereas

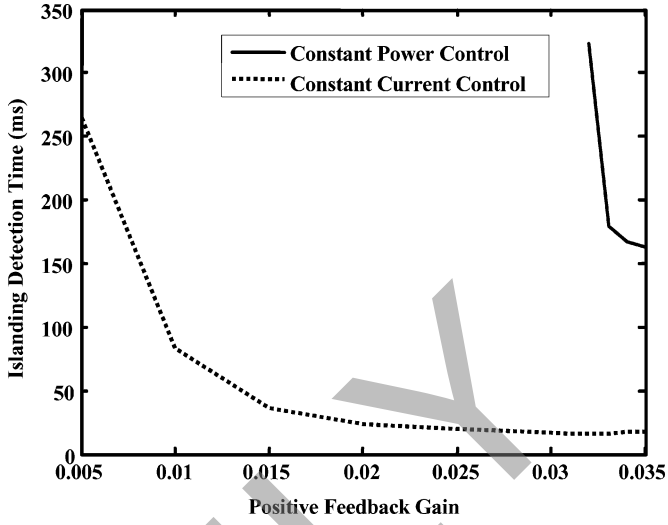

Fig. 4. Positive feedback gain versus islanding detection time curve of the SFS.

the constant current-controlled inverter loses its stability when the islanding is formed. This phenomenon is because the SFS gain is relatively large, which makes the positive feedback strong enough to destabilize the islanded DG system. On the other hand, the constant power-controlled inverter can maintain the stability after the islanding at the same positive feedback level. This indicates that the SFS antiislanding method does not work for the constant-power controlled inverter when the positive feedback gain of the SFS scheme is small. The reason is that the power regulator of the constant power controller counteracts the positive feedback control. In Fig. 3(c), K is further increased to 0.032, and the DG system is destabilized for both interface controls. For the constant power-controlled inverter, the strength of the power-control state cannot beat that of the SFS scheme when the main grid is disconnected. The inverter frequency begins to oscillate after the islanding, and the DG will be tripped by the frequency relay ultimately. However, it is to noted that the islanding detection takes longer to be detected if compared to the constant current-controlled inverter.

The impact of different inverter interface controllers on the antiislanding performance of the SFS scheme can be analyzed by using the positive feedback gain versus islanding detection time curve, which is shown in Fig. 4. This curve permits to obtain a generalized understanding. From this figure, it can be observed that when K is varied from 0.005 to 0.035, the islanding detection time for the constant current-controlled inverter is decreased from 265 to 18 ms (the frequency limits for the islanding detection adopted here are 59.3 and 60.5 Hz). However, the islanding condition cannot be detected by the SFS scheme for the constant power-controlled inverter when K is smaller than 0.032, and the islanding detection time for this type of inverter interface control is generally much longer than that obtained for constant current-controlled inverter. Therefore, one can conclude that the SFS scheme is more effective to the constant current-controlled inverter than to the constant power-controlled inverter.

V. Conclusion

This paper has revealed the characteristics of the interactions between the inverter interface controls and the SFS antiislanding method. It was found that the power regulator of the inverter controller can degrade the positive feedback control. As a result, the SFS scheme is much more efficient for constant current-controlled inverters than for constant power-controlled inverters.

References

[1] Z. Ye, A. Kolwalkar, Y. Zhang, P. Du, and R. Walling, "Evaluation of antiislanding schemes based on nondetection zone concept," *IEEE Trans. Power Electron*., vol. 19, no. 5, pp. 1171–1176, Sep. 2004.

[2] H. H. Zeineldin, E. F. EI-Saadany, and M. M. A. Salama, "Impact of DG interface control on islanding detection and nondetection zones," *IEEE Trans. Power Del.*, vol. 21, no. 3, pp. 1515–1523, Jul. 2006.

[3] M. E. Ropp, M. Begovic, and A. Rohatgi, "Analysis and performance assessment of the active frequency drift method of islanding prevention," *IEEE Trans. Energy Conv.*, vol. 14, no. 3, pp. 810–816, Sep. 1999.

[4] M. E. Ropp, M. Begovic, A. Rohatgi, G. A. Kern, R. H. Bonn, and S. Gonzalez, "Determining the relative effectiveness of islanding detection methods using phase criteria and nondetection zones," *IEEE Trans. Energy Conv.*, vol. 15, no. 3, pp. 290–296, Sep. 2000.