LCC-HVDC Bipole System with MMC-Based DC Tapping Stations

by

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A thesis submitted in partial fulfillment of the requirements for the degree of

Master of Science

in

Energy Systems

Department of Electrical and Computer Engineering

University of Alberta

Abstract

Line Commutated Converter based High Voltage DC (LCC-HVDC) is the dominant technology of HVDC power transmission worldwide. LCC-HVDC has lower cost of implementation and lower power losses, accompanied by higher voltage capabilities and higher power levels, in comparison to Voltage Source Converter based HVDC (VSC-HVDC) technology. However, VSC-HVDC has technical superiorities such as independent control of active and reactive powers, elimination of the risk of commutation failures, and drastically reduced size of harmonic filters. Combining the advantages of both the existing LCC-HVDC systems and newer VSC-HVDC technology, hybrid LCC-VSC HVDC transmission systems are being developed. As LCC-HVDC lines span very long distances, one particular hybrid system of interest is HVDC line power tapping where a small amount of power is tapped using VSC technology. To date, most systems level research studies on HVDC tapping have focused on using DC-AC VSC stations implemented on monopole systems with simplified controls Moreover, few works explore HVDC tapping using DC-DC converters that can create intermediate medium-voltage DC (MVDC) output buses, which offer increased flexibility for connection to downstream DC-AC VSCs or even for renewable energy integration.

This thesis develops a comprehensive tapping study system in RSCAD on an RTDS Novacor simulator, which consists of a ±500 kV 3 GW LCC-HVDC bipole system, designed based on the existing 3-Gorges HVDC system, and includes two DC-DC tapping converters using modern Modular Multilevel

Converter (MMC) technology, one connected at the middle of the HVDC line on each pole. The LCC-HVDC bipole system is modeled on the processor cores of the simulator. The two DC-DC MMCs are implemented using both processor and GT-FPGA based valve models: averaged MMC5 and detailed U5-MMC models for positive and negative pole tapping stations, respectively. The firing controls for the DC-DC MMCs are also modeled using the GTFPGA units.

The LCC-HVDC bipole is rated at 500 kV, 1500 MW per pole and each DC-DC MMC is rated at 75 MW, designed with a 500/40 DC step ratio to create a bipolar ±40 kV MVDC output bus. Controls are provided to operate each tap independently. The resulting hybrid LCC-VSC system therefore offers significant flexibility for systems level tapping studies, owing both to its independent pole design but also the realistic LCC-HVDC controls and modes of operation. Simulations are carried out to study independent pole power tapping feasibility as well as bidirectional power flow scenarios involving the tapping stations and their effects on existing LCC systems. Fault Studies were also carried out. Different types of AC and DC line-to-ground faults were triggered on the rectifier and inverter AC networks and HVDC links respectively. In all fault scenarios, the whole hybrid LCC-VSC HVDC system recovers to its pre-fault operating modes once they are cleared.

Preface

This thesis is an original work by Manish Persand under the supervision of Dr. Gregory Kish. Chapters 2 and 3 form part of a conference digest that has been submitted and provisionally accepted for presentation at the 2022 Cigre Canada Conference & Expo held in Calgary.
Chapters 2 & 3 provisionally accepted as:

- M. Persand, Y. Li, G.J. Kish, "Hybrid LCC-VSC Bipolar HVDC System for DC Power Tapping Studies", CIGRE Canada Conferene, Calgary, Alberta, Canada, November 2022

Acknowledgements

I would like to express my deepest appreciation and gratitude to my supervisor, Professor Gregory J. Kish for his invaluable guidance, expertise, knowledge and support throught my MSc degree.

I would also like to extend my sincere thanks to the members of the examination committee, Professor Hao Liang and Professor Marek Reformat for sparing their time and providing invaluable feedback.

Furthermore, I would like to thank my colleagues in the PEPST labs for their support and guidance.

I would like to express my appreciation to my parents, sibling and friends for their unwavering support, encouragement and understanding.

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Glossary of Terms

AC	Alternating Current
BBPC	Balance Bipole Power Control
CCA	Current Control Amplifier
CFC	Converter Firing Controls
CIGRE	Conseil International des Grands Réseaux Électriques
CMC	Current Margin Compensation
CSC	Current Source Converter
DC	Direct Current
DER	Distributed Energy Resources
EMT	Electromagnetic Transients Program
FBSM	Full Bridge Submodule
FFT	Fast Fourier Transform
HBSM	Half Bridge Submodule
HVDC	High Voltage Direct Current
IGBT	Insulated-Gate Bipolar Transistor
LCC	Line Commutated Converter
M2DC-CT	Modular Multilevel DC-DC Converter with Integrated Center-Tapped Transformer
MMC	Modular Multilevel Converter
MVDC	Medium Voltage Direct Current
PI	Proportional Integral
PR	Proportional Resonant
RAML	Rectifier Alpha Minimum Limiter
RMS	Root Mean Squared
RTDS	Real Time Digital Simulator
SM	Submodule
TCC	Transformer Tap Controls
THD	Total Harmonic Distortion
UBPC	Unbalanced Bipole Power Control
VCA	Voltage Control Amplifier
VDCOL	Voltage Dependent Current Order Limiter
VSC	Voltage Source Converter

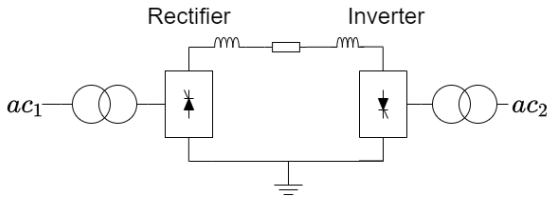
N	Number of Submodules
V_{SM}	Voltage across Submodule
V_C	Submodule Capacitor Voltage
I_{tap}	Tapping Current
I_{DC}	DC Current
V_{tap}	Tapping Voltage
V_{DC}	DC Voltage
P_{tap}	Power Tapped
f	Fundamental Frequency
i_{u1}, i_{u2}	Upper Arm Currents
i_{l1}, i_{l2}	Lower Arm Currents
$P_{dc,rated}$	Rated Power of M2DC-CT
V_{dci}	Input DC voltage
V_{dco}	Output DC voltage
V_{cap}	Nominal Cap Voltage
N_P	Number of SMs in upper arms
N_S	Number of SMs in lower arms
L_P	Upper arm inductance
L_S	Lower arm inductance
C_P	Upper arm capacitance
C_S	Lower arm capacitance
G_v	Voltage Step Down Ratio of M2DC-CT
p, n	Variable Subscripts to denote positve pole and negative pole
$I_{DC,R}, I_{DC,I}$	Rectifier and Inverter DC Currents
$V_{DC,R}, V_{DC,I}$	Rectifier and Inverter DC Voltages
Z_{line}	HVDC Link Line Impedance
Z_{filter}	Input Filter of M2DC-CT Tapping Stations
$V_{DC,tap}$	Voltage across Tapping Stations
$I_{DC,tap}$	DC Tapping Currents
$I_{DC,out}$	Tapping Stations Output DC Currents
P_{dc}	Power Demand of Tapping Stations
v_{ac_R}, v_{ac_I}	Rectifier and Inverter AC line-to-line Voltage
α_R	Rectifier Firing Angle
γ_I	Inverter Extinction Angle
$I_{dc,margin}$	Nominal DC Link Current Margin
Tap_R, Tap_I	Rectifier and Inverter Sides Transformer Tap Position

Chapter 1

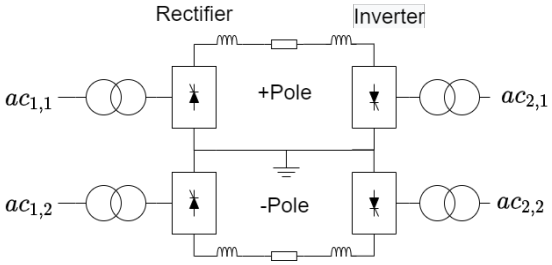
Introduction

1.1 Background

Line commutated converter based high voltage DC transmission (LCC-HVDC) is the dominant technology of global direct current (DC) power transmission given its lower cost, lower losses along with higher voltage capabilities and power levels relative to newer voltage source converter based high voltage direct current (VSC-HVDC) technology [1]–[3]. The first commercial HVDC system was implemented in 1954 between the island of Gotland and sweden using mercury arc valve technology [2] spanning over 98 km with a voltage rating of 100 kV and a power rating of 20 MW [2]. LCC based HVDC technology using thyristors emerged in the 1970s and has come a long way. Most recently, 1100 kV lines carrying 13 GW of power has been constructed in China at the Changji-Guquan LCC-HVDC system [2]. HVDC technology has been used in the majority of applications requiring bulk power transfer in transmission grids over long distances [4]. HVDC systems are separated into two main categories, namely, monopole systems and bipole systems as shown in Figure 1.1. Here, the LCC-based rectifier and inverter stations are denoted by the blocks with the thyristor symbol.



(a) Monopole HVDC System



(b) Bipole HVDC System

Figure 1.1: Typical LCC-HVDC Systems

The majority of HVDC systems across the world are LCC-based [5]. For example, multi-infeed HVDCs have surfaced in China where multiple inverters are being utilized in certain power grid, where Shanghai is being supplied by four HVDC lines and three of these lines connect to 500 kV ac buses while the remaining one connects to a 220 kV ac bus [6].

After a normal commutation operation in LCCs, the valve that just conducted current is turned off within a specific period of time. If the valve fails to restore its reverse current blocking ability, it will conduct again during the next cycle [7]. Commutation failure is said to occur when this phenomenon happens [7]. With the use of a high number of inverters close to each other along with the risk of AC faults, the chances of having multiple commutation failures are increased and system stability will be greatly affected [6]. These systems come with numerous challenges especially when connected to weak AC grids. One such challenge is the issue of harmonic current and voltage amplification which negatively affects AC networks and these arise from the resonance frequency produced by the "combination loop" of the different components in the multi-infeed HVDC such as transformers, reactors and even AC filters [6].

Since the late 1990s, newer voltage source converter (VSC) based HVDC systems have emerged as the preferred technology due to their advantages over LCCs. Some of these benefits are listed below [8]:

1. Power transmission can be maintained without the risk of commutation failures during AC faults
2. Reactive power can be supplied to AC system increasing its stability properties
3. Active and reactive power can be controlled independently, as opposed to LCCs that have onerous reactive power absorption requirements
4. Harmonic filters are designed to operate at higher frequencies thus reducing size and costs

Nowadays, VSCs are being adopted on newer long distance power transmission systems due to the aforementioned advantages [9]. With "wind power being the fastest growing electricity generation technology" and wind farms being established further out in the sea, VSC based HVDC transmission system is the best solution for power transmission from the wind farms to existing power grids [9]. In HVDC lines using VSC technology, losses are as low as 3% per 1000 km [9]. Today, several wind farms have been developed in Germany where the maximum transmission distance and power transfer capacity level has reached 200km and 900MW,respectively, at voltage levels up to $\pm 320kV$ [9].

The dominant class of VSCs used in modern offshore wind integration HVDC systems is the modular multilevel converter (MMC) [9], [10]. MMCs (and, in general, other VSCs such as the classical 2-level VSC) work without the risk of commutation failure; this is a major advantage over LCCs along with increased quality in output waveforms and better fault handling capabilities as compared to LCCs [10], [11]. Over the last few years, MMCs have become the

go to option for medium and high power applications in VSC based HVDC systems due to having several advantages over traditional 2-level and other multilevel converter topologies with the most important ones being [10], [11]:

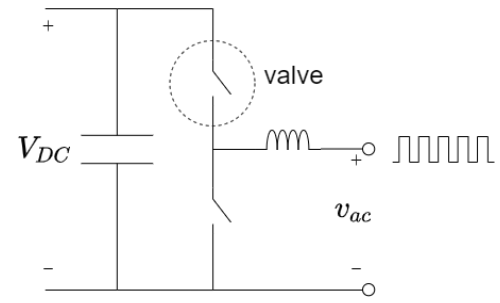
1. Any voltage level requirement can be met due to its "modularity and scalability" arising from the use of many identically rated submodules (SMs).

2. Having a high efficiency due to relatively low switching losses promotes its usage in high power applications

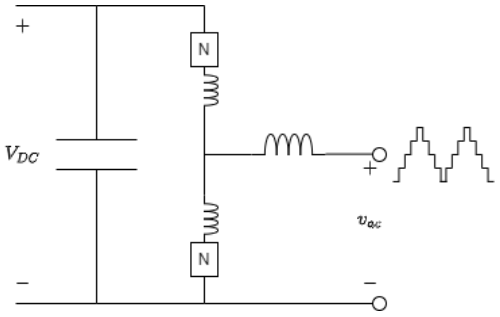
3. AC filter sizes can be greatly reduced, especially in high power applications, since SMs used have low voltage ratings and thus AC waveforms with hundreds of levels can be obtained, leading to superior harmonic performance

4. No central DC-link capacitors are required; but rather, capacitive energy storage is distributed amongst the individual SMs.

Along with the advantages that come with the MMCs, the control becomes more complex due to the large number of SMs (i.e switching cells) and also, circulating currents inherent to the MMC structure need to be suppressed [11]. Figure 1.2 contrasts the dc-ac operating principles of the classical two-level VSC and the MMC, for a single phase leg. Each valve in the MMC is comprised by the series connection of N submodules, which yields an $N+1$ ($N = 4$ is shown for illustrative purposes) ac level output. As N increases, the output voltage waveform gets closer and closer to an actual sinusoidal waveform and thus improving the output voltage quality.



(a) Classical two-level VSC system



(b) MMC system

Figure 1.2: VSC operating principle for single phase leg

MMCs are highly modular converters with N low-voltage submodules that are stacked to meet the voltage requirements for each valve [11]. The two most common SM topologies are the half bridge submodule (HBSM) and full bridge submodule (FBSM). HBSMs consist of two IGBTs with a capacitor in parallel that is either inserted or bypassed. When inserted, the voltage across the HBSM (V_{sm}) is equal to the capacitor voltage (V_C) and when it is bypassed, the voltage is zero [11]. As for FBSMs, the output voltage V_{sm} can be either zero or $\pm V_C$.

The first MMC implementation for HVDC transmission occured in 2010 when the Trans Bay cable project was built to transfer 400MW of power from Pittsburg to the San Francisco through an underwater cable with a length of 88km [12]. This project showed the practical advantages of the MMCs and was no longer only theoretical topologies [12]. The MMC is designed with $N = 200$ SMs per converter arm, producing a 201 level AC output, which in turn provides low voltage harmonics, operating at a voltage of $\pm 200kV$ while at the same time having smaller size components especially when it comes to

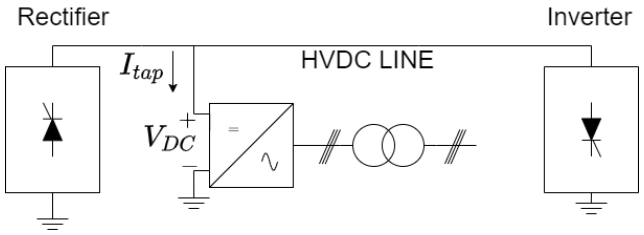
AC filters [12].

Combining the advantages of both the existing LCC-HVDC systems and newer VSC-HVDC systems, hybrid LCC-VSC HVDC transmission systems are being developed [13], [14]. Such systems combine the best traits of each converter technology. As mentioned in [13], several coastal regions of China have existing LCC-HVDC systems and with the rapid increase of wind power generation along with the creation of more offshore wind power farms, the performance of hybrid LCC-VSC HVDC technology have to be evaluated and tested under several conditions to ensure proper functionality and control schemes. Several hybrid topologies have been studied in HVDC systems such as LCCs being used on the rectifier side and MMCs used at the inverter side [15], VSCs used to connect renewable energy sources to existing ac grids and LCC HVDC lines [16], and MMCs being used in power tapping applications irrespective of whether the main HVDC system is an LCC based system or VSC based system [17]. Examples of real world hybrid LCC-VSC HVDC systems include the Skagerrak HVDC system, established between Norway and Denmark, and the Luxi back-to-back HVDC system established in China [18]. The Luxi back-to-back system functions at $\pm 500kV$ initially having a 2GW transmission capacity with an end goal of 3GW when the project is completed in the China Southern Power Grid, which is supposed to be five years long [19]. Skagerrak was commissioned in the 1970s with two LCCs rated at $\pm 250\ kV$, 500 MW [20]. In 1993, a third LCC was added, rated at $\pm 350\ kV$, 500 MW [20]. In 2014, a VSC was added to the three LCC Skagerrak terminals, rated at rated at 500 kV, 700 MW, thus making the Skagerrak HVDC transmission system a hybrid LCC-VSC HVDC system [20].

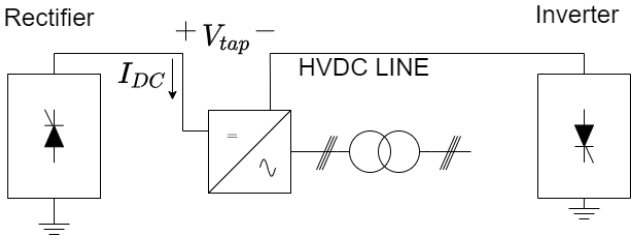
1.2 HVDC Line Power Tapping

As existing LCC-HVDC lines span very long distances, one particular type of hybrid system of interest is HVDC line power yapping where a small amount of power (typically $\leq 5\%$) can be tapped using VSC technology to feed re-

mote communities or even allow for power injection from nearby renewable sources with ideally negligible effect on the existing LCC-HVDC system [17], [21], [22]. The two ways of tapping include parallel tapping and series tapping. Figure 1.3 shows the basic idea of parallel and series tapping of power from HVDC lines.



(a) Parallel Tapping



(b) Series Tapping

Figure 1.3: Concept of Series and Parallel Tapping [21]

During parallel tapping, a current reduction occurs in the HVDC link current by the amount corresponding to I_{tap}. The power being tapped in this case is equivalent to:

$$P_{tap} = V_{DC} \times I_{tap} \tag{1.1}$$

where V_{DC} corresponds to the voltage at the node where the tapping station is connected to the DC link of the LCC-HVDC system. Parallel tapping can be broken down into two main methods: the single stage configuration and the two-stage configuration [21]. Single stage parallel tapping only requires one DC-AC converter and is traditionally known as AC tapping. Two stage parallel tapping consists of an intermediate medium voltage DC stage and thus has a DC-DC-AC conversion setup [21]. Single stage parallel tap topologies

include forced-commutated VSCs and dual-square wave VSCs, while two-stage parallel tap topologies include MMC-based parallel output pole taps, MMC-based parallel and series connected transformer taps as well as MMC-based series output pole tap [21].

Compared to parallel tapping, series tapping typically operate in HVDC systems with lower power ratings and the power variation is done through varying the DC link voltage and thus instead of a current drop there is a voltage drop equivalent to V_{tap} and the power tapped is [21]:

$$P_{tap} = V_{tap} \times I_{DC} \tag{1.2}$$

The current flowing from the rectifier to the inverter through the tapping station will be the same at all the stages. Only the line voltage is affected and this can cause the losses in the valves of the rectifiers and inverters to increase [23]. During series tapping, the tapping station must be rated for the full current of the LCC system and the voltage insulation must be done according to the full voltage swing of the LCC system as well [23]. Series tap topologies include twelve pulse current source converters (CSCs), forced-commutared CSCs and series capacitor commutated inverters among others [21].

1.2.1 AC Tapping vs DC Tapping

Traditionally, the main approach is to use three-phase DC-AC converters directly which is known as the conventional AC tapping method as shown in Figure 1.4. The DC-AC converter is usually followed by a three-phase transformer to obtain the required AC output voltage. However, these converters need to be rated for the full voltage swing of the HVDC bus and three phase legs are required, thus making it expensive to design and implement [24].

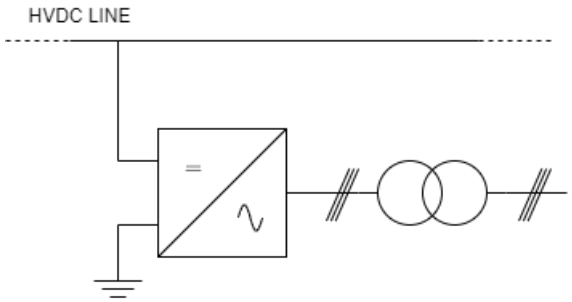


Figure 1.4: AC Tapping using parallel connection [24]

One of the first proposals of tapping was done in 1981 where a synchronous machine was used to implement a series tap [25]. As mentioned in [26], the first implementation of parallel tapping happened on the monopole HVDC system connecting Sardinia to Italy where a 50MW station was set up in Corsica to tap power in 1988, although this tap represents 25% of the line rating ($50MW$ tap on a $200MW$ line). Therefore, the tapping station would more accurately be referred to as a third terminal with reduced power rating. The Quebec-New England DC Link was the first bipolar HVDC system designed for multiterminal operation in 1986. More recently, newer topologies have been proposed for AC tapping such as the use of capacitor-commutated thyristor modules which remove the issues of commutation failure as well as allowing for independent frequency control [27]. Other studies have shown the use of series-input parallel-output DC-AC 2-level VSCs stacked as multi modules to extract a small amount of power from existing HVDC lines [28].

A more recent concept known as DC tapping or two-stage parallel tapping has been proposed in which a medium voltage direct current (MVDC) bus is created at the output of a DC-DC converter, and then DC-AC converters are connected to MVDC bus and tap the required amount of power as shown in Figure 1.5 [17], [21], [22], [24]. Such a topology requires a DC-DC converter with a high step DC voltage ratio between the HVDC side and the MVDC side [24].

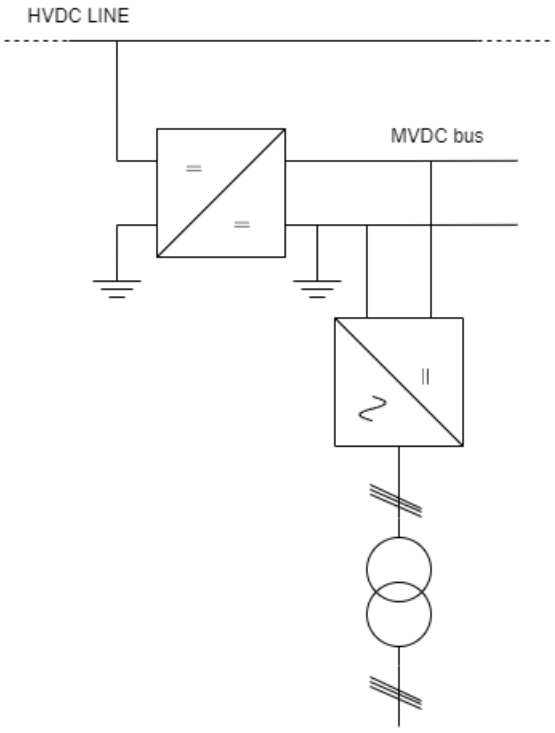


Figure 1.5: DC Tapping using parallel connection [24]

With MVDC voltage and power levels more suitable for distribution applications as compared to HVDC which is more suitable to bulk power transfer over long distances), interconnecting these two systems through a high voltage ratio is suitable for tapping but it comes with its challenges [24]. With DC tapping being a very recent technology, more studies are being carried out when it comes to high voltage ratio DC-DC converters [24]. One such converter has been proposed in [17] where one MMC based DC-AC converter is connected to a VSC based AC-DC converter through a transformer operating at a frequency of $350Hz$. In [22], a resonant DC-DC converter is proposed which consists of numerous identical submodules using a controllable switch, two diodes and one capacitor. Stacking the submodules provides a high step down ratio suitable for DC tapping across bipole systems with the converter connected between $\pm V_{DC}$ the positive and negative poles. In [29], another high voltage step down ratio MMC based DC-DC converter is proposed where the upper arms and lower arms of the MMC are connected through a center tapped transformer to minimize internal converter current stresses.

1.3 Thesis Motivation

Most researches regarding tapping that have been carried out involve single stage AC tapping on exisiting LCC systems. Over the last few years, with the prominent rise of VSC based converters such as the MMC, DC tapping has become a growing point of interest and the two stage implementation offers some benefits over the single stage implementation, such as:

1. a more efficient utilization of installed semiconductors thus leading to a more compact implementation of the converters, particularly the dc-dc stage.

2. the availability of intermediate MVDC buses providing a flexible DC distribution bus, making it easier for renewable energy integration which is growing in popularity.

However, in the few existing studies that have been done on DC tapping, relatively simple monopole implementations were carried out and are typically limited to unidirectional power flow. In [22], an LCC bipole system was modeled, however, the DC tapping was done across the poles and therefore true bipolar operation was not explored. In previous studies, whether it was AC tapping or DC tapping, the simulations and studies were carried out using HVDC benchmark systems available in EMT softwares such as PSCAD. The CIGRE HVDC benchmark system and variations of the system have been used in several studies [30]–[32] with different tapping setups whether it is AC or DC tapping in a series or parallel configuration. However, this is a relatively basic monopolar system with simplified controls. Utilizing a full bipolar HVDC model with detailed controls, reminiscent of an actual real world installation, would enable a much deeper study of DC tapping on individual poles and the behaviour of the systems in different test cases.

1.4 Thesis Contribution

Hybrid LCC-VSC systems combine the advantages of both LCC and VSC systems. Existing HVDC lines can be expanded into multi-terminal HVDC

systems where both power tapping and renewable energy integration is feasible. A bipole system based on the 3-Gorges was developed by RTDS technologies and was made available through their RSCAD software which can be used on their real time simulator platform. The detailed 3GW, $\pm 500kV$ bipole LCC is augmented in this work on an RTDS NovaCor real-time simulator with two MMC-based DC-DC converters to study DC tapping. This system provides flexibilty to investigate the effect of AC and DC faults throughout the entire system, whether it is on the LCC system or the VSC-based DC tapping stations, as well as to reverse the direction and amount of power being tapped. This is especially important when it comes to renewable energy integration. It will be shown how the tapping stations operate, and their effects on the existing LCC HVDC Bipole system, in several test scenarios in terms of power demands and location of AC and DC faults.

Chapter 2

Modeling and Control of Bipole LCC-HVDC System with MMC-Based DC Tapping Stations

In this chapter, the basics of LCC systems and MMCs are described along with the adopted hybrid system architecture being studied with the corresponding models and controllers implemented on the RTDS NovaCor real-time simulator.

2.1 Line Commutated Converter

Traditionally, LCCs use conventional thyristors. Due to the low cost of thyristors along with high voltage and current capability, they have become the backbone in the implementation of HVDC. To build up the required voltage in the DC link, low voltage thyristors (usually $1 - 2kV$) are stacked in series. Figure 2.1 below shows the typical setup of a six pulse LCC which is considered as the building block of classical HVDC systems and implementation. A six pulse LCC consists of six thyristor valves arranged in a three-phase configuration.

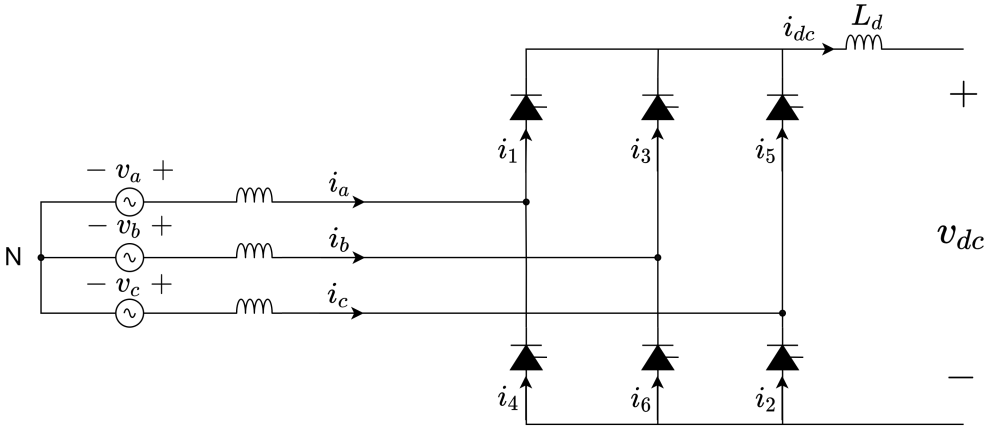


Figure 2.1: Classical Six Pulse LCC [33]

Each pair of thyrsitor valves conduct during one third of a cycle sequentially, i.e 120°, as shown in Figure 2.2. As a result of this sequential firing, six ripples will be present in the DC output voltage during every AC cycle. The DC link current (i_{dc}) directly affects the magnitude of the average DC voltage at both the rectifier and the inverter. The firing angle of the rectifier is defined by α where $0° \leq \alpha \leq 90°$.

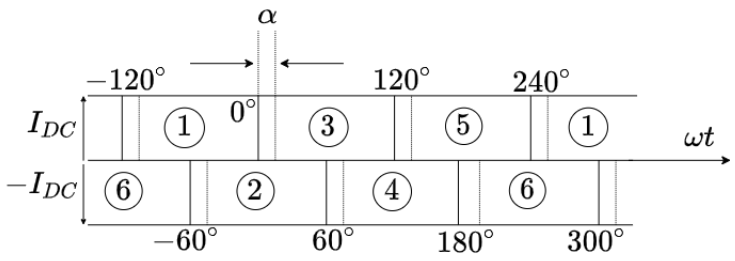


Figure 2.2: LCC Commutation Process [33]

With zero firing angle ($\alpha = 0°$), the output DC voltage with no load is given by:

$$V_{dc0} = \frac{3\sqrt{2}}{\pi} V_{LL} \tag{2.1}$$

where, V_{LL} is the AC line-to-line rms voltage. Varying α (i.e $\alpha \neq 0$) at the rectifier causes the average voltage to change as follows:

$$V_{dc,r} = V_{dc0,R} cos\alpha_R - R_{c,R} I_{dc} \tag{2.2}$$

Similarly, at the inverter side, varying α directly affects the average DC voltage as follows:

$$V_{dc,I} = V_{dc0,I} cos\alpha_I - R_{c,I} I_{dc} \tag{2.3}$$

However, for inverter operation, $90° \leq \alpha \leq 180°$. The inverter firing angle is more commonly denoted as β where:

$$\beta = \pi - \alpha_I \tag{2.4}$$

$R_{c,R}$ and $R_{c,I}$ are virtual commutation resistances used to quantify the voltage drop during the commutation process at the rectifier and inverter stations respectively. These virtual(abstract) resistances consume no real power, and are directly related to the equivalent inductances at the AC sources as follows:

$$R_{c,R} = \frac{3}{\pi} \omega L_{c,R} \tag{2.5}$$

and,

$$R_{c,I} = \frac{3}{\pi} \omega L_{c,I} \tag{2.6}$$

Under normal convention, the inverter commutation process is described by the extinction angle, γ, where:

$$\gamma = \pi - \delta \tag{2.7}$$

and δ is the extinction angle at the rectifier station. The overlap angle μ is defined as:

$$\mu = \delta - \gamma \tag{2.8}$$

The commutation current and the average DC voltage at the inverter, as a function of γ is given by:

$$I_{dc} = \frac{\sqrt{3} V_{LL}}{2\omega L_{c,I}} (cos\gamma - cos\beta) \tag{2.9}$$

$$V_{dc,I} = V_{dc0,I} cos\gamma - R_{c,I} I_{dc,I} \tag{2.10}$$

LCCs also always consume reactive power and thus reactive power compensation procedures need to be implemented. Modern LCC systems make use of twelve pulse LCCs that consist of multiple six-pulse thyristor bridges.

A twelve-pulse LCC is shown in Figure 2.3, which consists of two sets of six thyristor valves connected in series. The resulting V_{dc} now contains twelve-pulse ripple. With more pulses, most of the low order AC harmonics are eliminated (3^{rd},7^{th},17^{th},19^{th}) except for 11^{th} and 13^{th}.

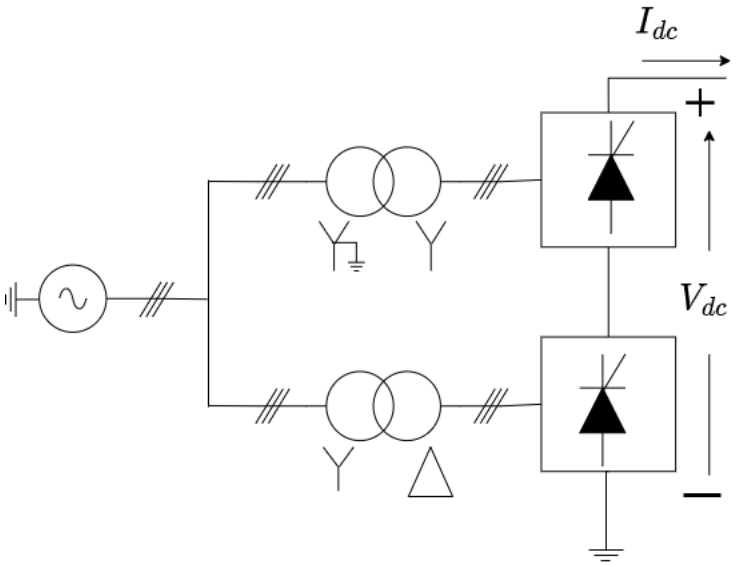


Figure 2.3: Classical 12-Pulse LCC arrangement

2.2 The Conventional DC-AC Modular Multilevel Converter

The MMC is the most popular solution for VSC-based HVDC systems. Single phase MMCs consist of one or two legs while three phase MMCs have three phase legs. Each phase leg has 2N submodules. Figure 2.4 shows a single phase MMC implemented with two phase legs.

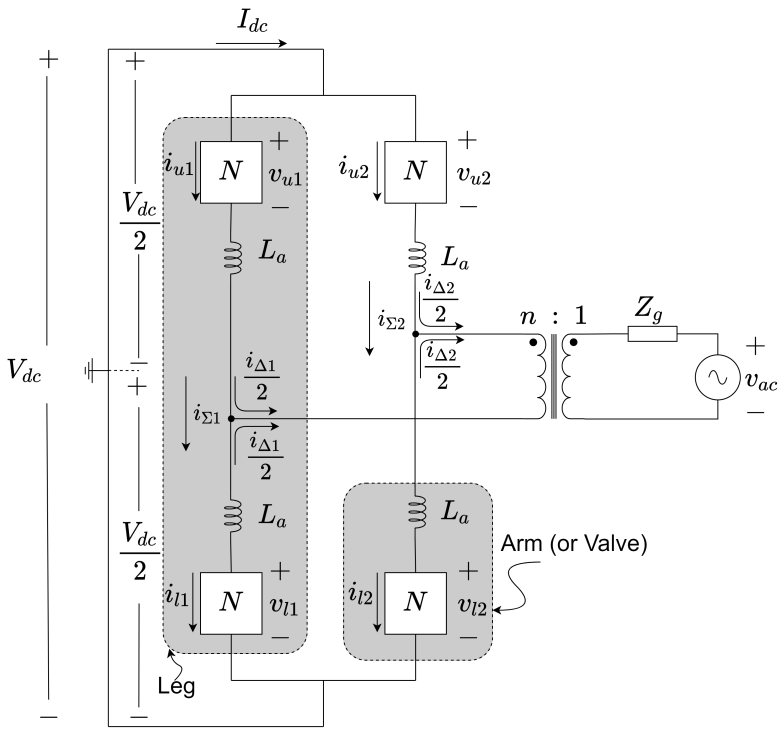


Figure 2.4: Single Phase MMC using Two Phase Legs

The following relationships for the arm currents can be derived:

$$i_{u1} = \frac{1}{2}(I_{dc} + \sqrt{2}I_{rms}cos(\omega t + \theta_i)) = i_{l2} \tag{2.11}$$

$$i_{l1} = \frac{1}{2}(I_{dc} - \sqrt{2}I_{rms}cos(\omega t + \theta_i)) = i_{u2} \tag{2.12}$$

Observe arm currents i_{u1}, i_{u2}, i_{l1}, i_{l2} contain both dc and fundamental frequency components. During an ideal operation, using abstract Σ and Δ quantities provides frequency decoupling. The Σ and Δ current quantities in Figure 2.4 can be obtained from equations (2.11) and (2.12) as follows:

$$i_{\Sigma 1} = \frac{i_{u1} + i_{l1}}{2} \tag{2.13}$$

$$i_{\Sigma 2} = \frac{i_{u2} + i_{l2}}{2} \tag{2.14}$$

$$i_{\Delta 1} = i_{u1} - i_{l1} \tag{2.15}$$

$$i_{\Delta 2} = i_{u2} - i_{l2} \tag{2.16}$$

The decoupling of the ac and dc components results in the ideal Σ and Δ quantities being as follows:

$$i_{\Sigma 1} = i_{\Sigma 2} = \frac{I_{dc}}{2} \tag{2.17}$$

$$i_{\Delta 1} = -i_{\Delta 2} = \sqrt{2} I_{rms} cos(\omega t + \theta_i) \tag{2.18}$$

Therefore, the physical arm currents ($i_{u1}, i_{u2}, i_{l1}, i_{l2}$) consist of both dc and fundamental frequency components while the quantities $i_{\Sigma 1}$, $i_{\Sigma 2}$ and $i_{\Delta 1}$, $i_{\Delta 2}$ contain only dc and fundamental frequency components, respectively. This is beneficial from a control perspective. The arm voltages are:

$$v_{u1} = \frac{1}{2}(V_{dc} - 2\sqrt{2} V_{rms} cos(\omega t + \theta_v)) = v_{l2} \tag{2.19}$$

$$v_{l1} = \frac{1}{2}(V_{dc} + \sqrt{2} V_{rms} cos(\omega t + \theta_v)) = v_{u2} \tag{2.20}$$

The ac voltage output is therefore defined as:

$$v_{ac} = \frac{1}{n} 2\sqrt{2} V_{rms} cos(\omega t + \theta_v) \tag{2.21}$$

Equations (2.17)-(2.21) show the DC and AC components of the current flowing through each arm and at the output. The current loops created causes a purely AC current to flow at the output under ideal conditions. If the upper left arm and lower right valves are conducting in Figure 2.4, the current follows the arrowed path in a counterclockwise loop. Similarly, if the other two valves are conducting, the current follows the arrowed path in a clockwise loop. These two current loops oppose in directional flow at the transformer causing an alternating current at the output side.

The AC output voltage will consist of N+1 levels which is why the higher the number of SMs the better the output voltage profile will be. The two most common cells are the half bridge SMs (Figure 2.5) and the full bridge submodule (Figure 2.6). For both HBSMs and FBSMs, the current through the capacitor is given by:

$$v_c = \frac{1}{C} \int_0^t i_C(\tau)\, d\tau \tag{2.22}$$

2.2.1 The Half Bridge Submodule

The capacitors in Figure 2.5 are either inserted or bypassed to get the required output voltage, V_{SM}. When the capacitors are inserted, the voltage V_{SM}, is equal to the capacitor voltage (V_C) and when it is bypassed, the voltage V_{SM} is zero [34].

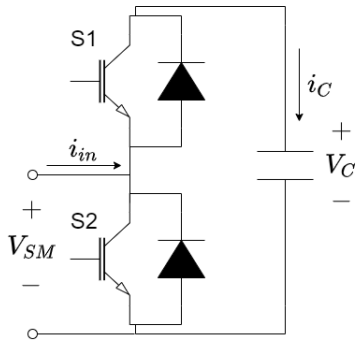


Figure 2.5: Half Bridge Submodule [34]

S_1	S_2	V_{SM}
1	0	V_C
0	1	0

Table 2.1: HBSM Switching States [34]

As shown in table 2.1, when switch S1 is on and a positive current (i_{in}) is flowing through the switch, V_C increases. As long as switch S1 is ON, the current flowing through it will directly affect V_{SM}. When switch S2 is ON, V_{SM} is always zero, irrespective of current direction. Therefore: [34]

$$V_{SM} = S_1 V_C \tag{2.23}$$

and,

$$i_C = S_1 i_{in} \tag{2.24}$$

2.2.2 The Full Bridge Submodule

For FBSMs, the voltage V_{SM} can be either zero or $\pm V_C$. The switching states of a full bridge submodule is given in table 2.2

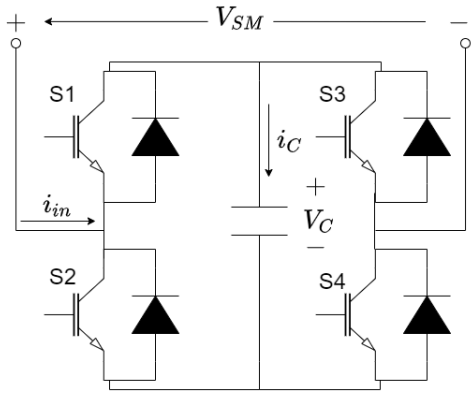


Figure 2.6: Full Bridge Submodule [34]

S_1	S_2	S_3	S_4	V_{SM}
1	0	0	1	V_C
0	1	1	0	$-V_C$
1	0	1	0	0
0	1	0	1	0

Table 2.2: FBSM Switching States of interest [34]

Switches S_1 and S_2 alternate with each other. Switches S_3 and S_4 behave similarly. Switches S_1 and S_4 determine the current flowing through the DC capacitor. When both S_1 and S_4 are ON, the submodule voltage is equal to V_C. When both S_1 and S_4 are OFF, the submodule voltage is equal to $-V_C$. If the state of switches S_1 and S_4 are different, V_{SM} is 0. Therefore: [34]

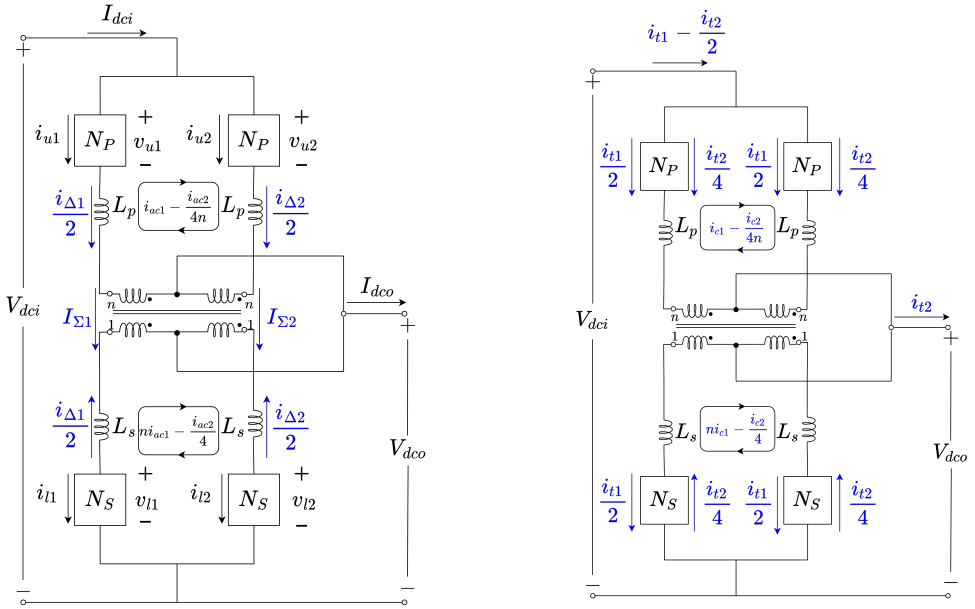
$$V_{SM} = (S_1 S_4 - S_2 S_3) V_C \tag{2.25}$$

and,

$$i_C = (S_1 S_4 - S_2 S_3) i_{in} \tag{2.26}$$

2.3 High Voltage Ratio Modular Multilevel DC Converter

This section describes the high voltage ratio DC-DC MMC used to augment the HVDC bipole system for tapping purposes in this thesis. Figure 2.7 shows the topology of the DC-DC MMC as proposed in [29], referred to as the M2DC-CT.



(a) M2DC-CT with physical (Black) and Σ-Δ (Blue) Currents

(b) M2DC-CT with abstract 'c' and 't' (Blue) Currents

Figure 2.7: M2DC-CT with different current configurations

In DC-AC applications, a two-leg DC-AC MMC with N submodules in all arms is used to produce single phase quantities. As described in section 2.2, the Σ and Δ quantities produce currents in such a way that both AC and DC current flow within the arms while AC current is obtained at the grid output [29]. In the M2DC-CT, the upper and lower arms have N_p and N_s submodules, respectively, and the AC current is made to circulate within the arms through the use of a center tapped transformer so that only DC current is obtained at the output as shown in 2.7(a). The windings center taps are connected together at the output to allow for DC power transfer. Due to the

DC power transfer mechanism, the winding currents are required to have both AC and DC components [29]. However, the transformer windings are oriented in such a way that there is core DC flux cancellation [29]. Here, n denotes the transformer turns ratio.

In the M2DC-CT, the AC and DC quantities are not decoupled when transferring to the Σ and Δ values. The physical arm currents are denoted by i_{u1}, i_{u2}, i_{l1} and i_{l2} while the arm voltages are denoted by v_{u1}, v_{u2}, v_{l1} and v_{l2} as shown in Figure 2.7(a). Initially, two ac current loops, i_{ac1} and i_{ac2} along with the DC currents I_{dci} and I_{dco} comprise the arm currents based on:

$$\begin{bmatrix} i_{u1} \\ i_{u2} \\ i_{l1} \\ i_{l2} \end{bmatrix} = \frac{1}{4} \begin{bmatrix} 2 & 0 & -4 & -\frac{1}{n} \\ 2 & 0 & 4 & \frac{1}{n} \\ 2 & -2 & -4n & 1 \\ 2 & -2 & 4 & -1 \end{bmatrix} \begin{bmatrix} I_{dci} \\ I_{dco} \\ i_{ac1} \\ i_{ac2} \end{bmatrix} \tag{2.27}$$

From equation (2.27), it can be seen that the physical arm currents are not decoupled into its AC and DC components respectively. Representing the arm currents by Σ and Δ quantities yields:

$$\begin{bmatrix} i_{\Sigma 1} \\ i_{\Sigma 2} \\ i_{\Delta 1} \\ i_{\Delta 2} \end{bmatrix} = \frac{1}{4(n+1)} \begin{bmatrix} 2(n+1) & -2 & -8n & 0 \\ 2(n+1) & -2 & 8n & 0 \\ 0 & 4 & 8(n-1) & -2(n+1) \\ 0 & 4 & 8(1-n) & 2(n+1) \end{bmatrix} \begin{bmatrix} I_{dci} \\ I_{dco} \\ i_{ac1} \\ i_{ac2} \end{bmatrix} \tag{2.28}$$

However, inspection of (2.28) shows that, unlike the DC-AC MMC, the M2DC-CT does not offer frequency decoupling when moving into the $\Sigma - \Delta$ domain. Therefore, the $\Sigma - \Delta$ currents are broken down further into four abstract variables i_{t1}, i_{t2}, i_{c1} and i_{c2} as shown in Figure 2.7(b), where

$$\begin{bmatrix} i_{t1} \\ i_{t2} \\ i_{c1} \\ i_{c2} \end{bmatrix} = \begin{bmatrix} 1 & -\frac{1}{2} & 0 & 0 \\ 0 & 1 & 0 & 0 \\ 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 1 \end{bmatrix} \begin{bmatrix} I_{dci} \\ I_{dco} \\ i_{ac1} \\ i_{ac2} \end{bmatrix} \tag{2.29}$$

From (2.29), i_{t1} and i_{t2} only have DC components while i_{c1} and i_{c2} have only AC components. Thus, frequency decoupling is obtained. In the M2DC-CT, i_{c2} is equal to the the transformer magnetizing current which is practically negligible when compared to the other currents.

Therefore, as described in [29], the individual arm currents and voltages can finally be expressed as:

$$\begin{bmatrix} i_{t1} & i_{t2} & i_{c1} & i_{c2} \end{bmatrix}^T = T_i \begin{bmatrix} i_1 & i_2 & i_3 & i_4 \end{bmatrix}^T \tag{2.30}$$

and,

$$\begin{bmatrix} v_{t1} & v_{t2} & v_{c1} & v_{c2} \end{bmatrix}^T = T_v \begin{bmatrix} v_{u1} & v_{u2} & v_{l1} & v_{l2} \end{bmatrix}^T \tag{2.31}$$

where,

$$T_i = \frac{1}{4} \begin{bmatrix} 2 & 2 & 2 & 2 \\ 4 & 4 & -4 & -4 \\ -1 & 1 & -\frac{1}{n} & \frac{1}{n} \\ -4n & 4n & 4 & -4 \end{bmatrix} \tag{2.32}$$

and,

$$T_v = \frac{1}{4} \begin{bmatrix} 1 & 1 & 1 & 1 \\ 1 & 1 & -1 & -1 \\ -1 & 1 & -n & n \\ -1 & 1 & n & -n \end{bmatrix} \tag{2.33}$$

The AC and DC components are fully decoupled in 2.7(b).

In this thesis, the parameters of the M2DC-CT installed at each pole are as follows:

Parameter	Description	Value
$P_{dc,rated}$	Rated Power of M2DC-CT	75 MW
V_{dci}	Input DC voltage	500 kV
v_{dco}	Output DC voltage	40 kV
v_{cap}	Nominal Cap Voltage	2 kV
N_P	Number of SMs in upper arms	460 (FBSM)
N_S	Number of SMs in lower arms	40 (HBSM)
L_P	Upper arm inductance	50 mH
L_S	Lower arm inductance	10 mH
C_P	Upper arm capacitance	1 mF
C_S	Lower arm capacitance	12.5 mF
f	Fundamental frequency	150 Hz

Table 2.3: M2DC-CT Parameters

The M2DC-CT voltage ratio is given by:

$$G_v = \frac{V_{dco}}{V_{dci}} \tag{2.34}$$

The turns ratio of the transformer is directly determined by the voltage ratio:

$$n = \frac{1 - G_v}{G_v} \tag{2.35}$$

Based on the M2DC-CT parameters, G_v is 12.5 and n is 11.5. This will establish a $\pm 40\ kV$ MVDC output bus for DC tapping on the $\pm 500\ kV$ LCC-HVDC system. The 75 MW M2DC-CT rating is set equal to 5% of the LCC-HVDC pole rating (1500 $MW \times 0.05$). To counter the adverse effects of DC faults on the HVDC link of the LCC bipole system, FBSMs have been used on the upper arms of the M2DC-CT. This way, the M2DC-CT can block the flow of DC fault currents [29]. Since FBSMs are only required at the side connected to the LCC bipole HVDC link, the lower arms SMs are still HBSMs.

2.3.1 M2DC-CT Control System

As described earlier, the voltages and currents of the M2DC-CT are broken into 't' and 'c' domain quantities to facilitate control of DC and AC quantities, respectively. The control loops are broken into two main parts as shown in Figure 2.8 [29]:

1. Output Power Regulation

    - The output power regulation mechanism is set to make sure that the required P_{dc} is obtained at the dc output current by regulating i_{t2} through PI controllers.

2. Capacitor Voltage Balancing

    - The total sum of the average capacitor voltages ($\Sigma v_{cap,t1}$) is used in a cascaded loop comprising of an inner current loop to regulate the dc current, i_{t1}, through PI controllers and an outer voltage loop to generate i_{t1}^{ref}.

- Another component of the capacitor voltage balancing mechanism is the regulation of the difference in average capacitor voltages ($\Delta v_{cap,t2}$) which again utilizes cascaded loops. The inner current loop is used to regulate the ac current i_{c1} through the use of proportional resonant controllers while the outer voltage loop generates $\hat{I}_{c1}^{ref}$ through PI controllers.

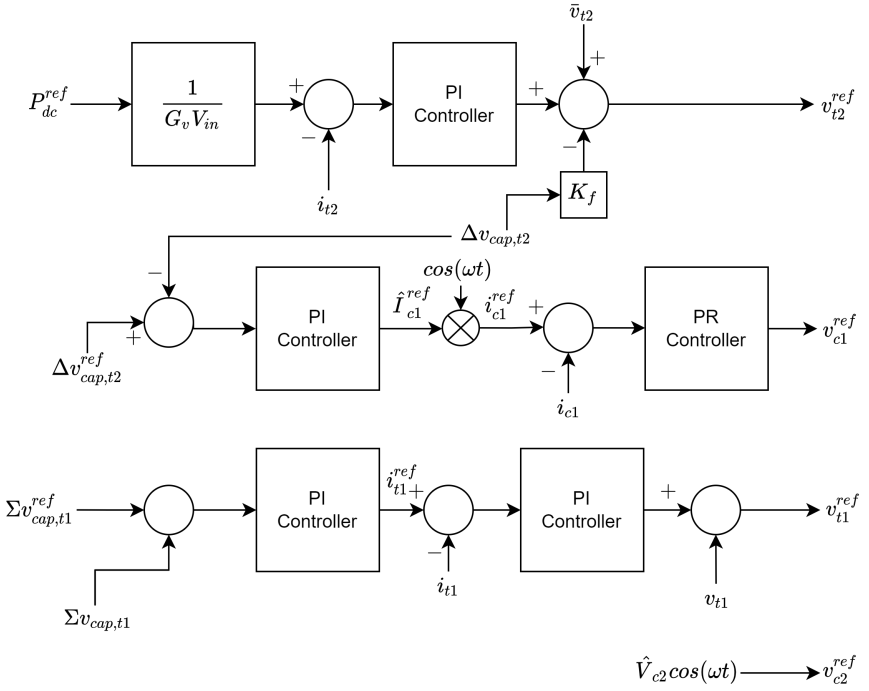


Figure 2.8: Control Loops for M2DC-CT [29].

The reference waveforms created by the control loops (v_{c1}^{ref},v_{c2}^{ref},v_{t1}^{ref},v_{t2}^{ref}) are used to generate the modulating signals (m_1, m_2, m_3, m_4) using the nearest level modulation technique. Further details are available in [29]. The Σ and Δ components of the capacitor voltages are defiend as follows:

$$\Sigma v_{cap,t1} = \frac{1}{4}(\sum_{j=1}^{N_p} v_{c,j}^{arm1} + \sum_{j=1}^{N_p} v_{c,j}^{arm2} + \sum_{j=1}^{N_s} v_{c,j}^{arm3} + \sum_{j=1}^{N_s} v_{c,j}^{arm4}) \tag{2.36}$$

$$\Delta v_{cap,t2} = \frac{1}{4}(\sum_{j=1}^{N_p} v_{c,j}^{arm1} + \sum_{j=1}^{N_p} v_{c,j}^{arm2} - \sum_{j=1}^{N_s} v_{c,j}^{arm3} - \sum_{j=1}^{N_s} v_{c,j}^{arm4}) \tag{2.37}$$

Table 2.4 summarizes the main components of the control loops and their main control goal:

Variable	Frequency Component	Control Goal
i_{t1}	dc	Regulating $\Sigma v_{cap,t1}$
i_{t2}	dc	Regulating P_{dc}
i_{c1}	AC fundamental frequency	Regulating $\Delta v_{cap,t2}$

Table 2.4: M2DC-CT Control Goals [29].

2.4 Hybrid HVDC Study System

The system being studied is a bipole LCC system based on the 3-Gorges system in China, available in the RSCAD library [35], augmented by using two MMC-based DC-DC converters (i.e two M2DC-CT Topologies) each with a high voltage step ratio, of $G_v = \dfrac{40}{500} = 0.08$ in Figure 2.9. The high voltage side of the tapping converters are connected to the HVDC line at the halfway point between the rectifier and inverter stations at each pole.

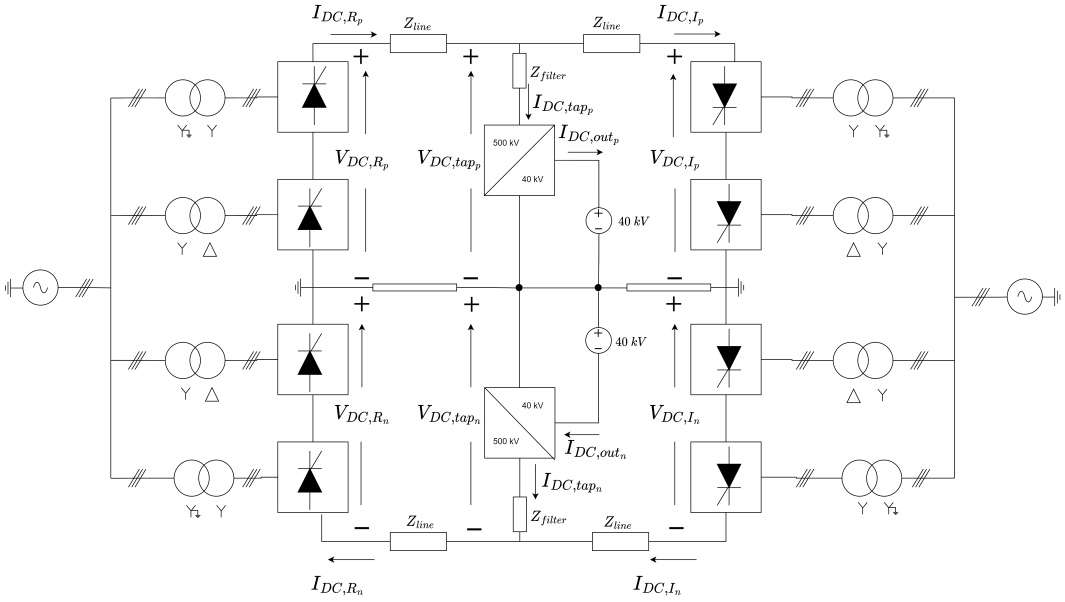


Figure 2.9: LCC Bipole System with MMC-based tapping stations

2.4.1 RTDS Bipole LCC HVDC System

The main parameters of the bipole system is given in table 2.5. Each pole is rated at 500 $kV, 3\ kA$ (1500 MW). Rectifier and inverter stations at each pole use twelve-pulse LCC configuration. The wye-wye and wye-delta transformers are equipped with tap changers to regulate the secondary voltage for different scenarios. The HVDC link spans a distance of 1059.1 km [35]. Electrode lines of length 60 km and 40 km are connected at the rectifier and inverter sides respectively. These electrode lines are used for grounding purposes [35].

Parameter	Description	Value
P_{dc}	DC power measured at the rectifier	3000 MW
$V_{dc,R}$	Nominal rectifier DC voltage	$\pm$500 kV
$v_{ac,R}$	Rectifier side AC line-to-line voltage	525 $kV\ rms$
$v_{ac,I}$	Inverter side AC line-to-line voltage	525 $kV\ rms$
α	Nominal rectifier firing angle	15°
γ	Nominal inverter extinction angle	17°
R_{dc}	Single pole DC line resistance	9.710 Ω
f	rectifier and inverter ac side frequency	50 Hz
I_{dc}	Nominal DC link current	3.0 kA
$I_{dc,margin}$	Nominal DC link current margin	0.3 kA

Table 2.5: LCC Bipole System Parameters [35]

2.4.2 Control System

This section describes the main components of the control system for the bipole LCC system.

2.4.2.1 Overview

Figure 2.10 provides an overview of the main control scheme at each rectifier and inverter stations for the converter operations. The α_{max} value is important when it comes to setting the correct output for both the current and

voltage controllers which are then used to produce the firing pulses (signals $CP1$ through $CP12$) for the corresponding twelve-pulse stations. The individual components of the control scheme are described in more detail in the upcoming sections.

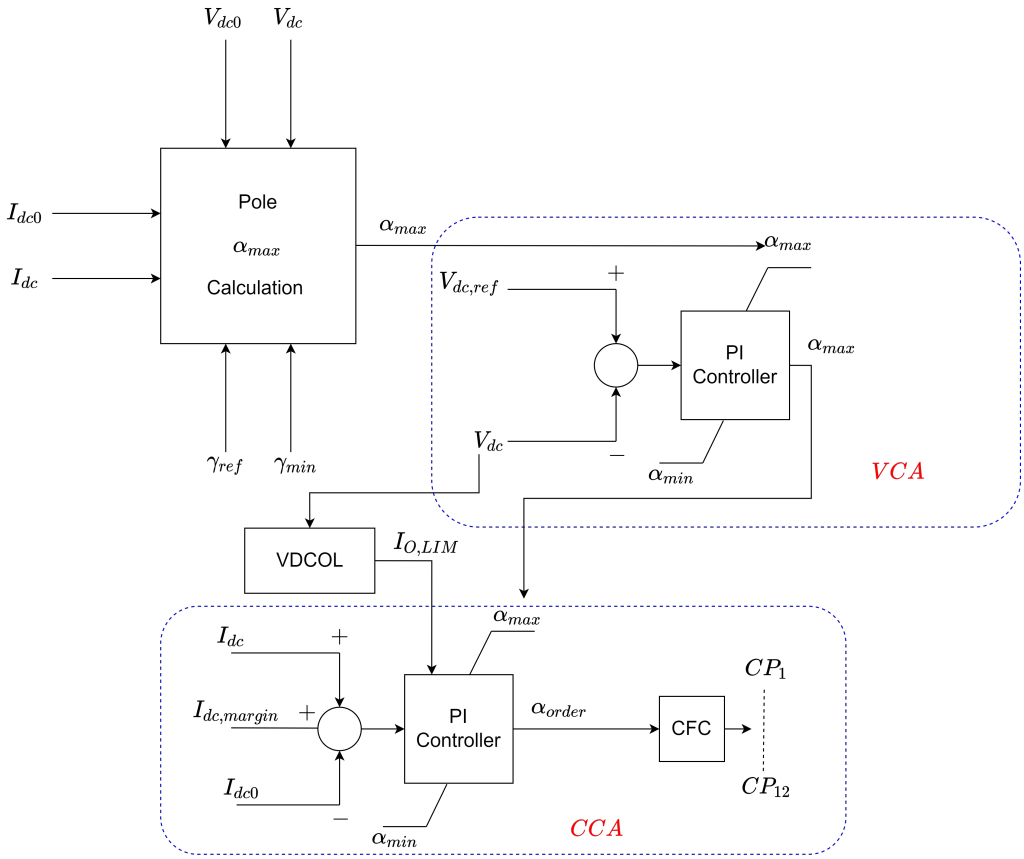


Figure 2.10: LCC Control Structure at inverter stations [35]

2.4.2.2 Pole α_{max} Calculation

α_{max} is one of the main components involved in the voltage and current control of both the rectifier and the inverter stations.

Figure 2.11 shows the quantities required to calculate α_{max} for each pole and is obtained as follows:

$$\alpha_{max} = 180^\circ - cos^{-1}[cos\gamma_{ref} - 2\frac{d_x I_{dc0}}{V_{dc0}} - K(I_{dc0} - I_{dc})] \tag{2.38}$$

where, I_{dc} is the HVDC link DC current, I_{dc0} is the rectified current at the

rectifier station, V_{dc0} is the rectified AC voltage. γ_{min} is directly involved in the measurement of I_{dc} and is used in the inner loop of the pole α_{max} calculation to determine whether γ_{min} or γ_{ref} will be used to calculate α_{max}. One assumption here is that $I_{dc} = I_{dc0}$. If this is not true, the term $K(I_{dc0} - I_{dc})$ is used to make sure the $I - V$ characteristic of the inverter/rectifier produces a positive slope.

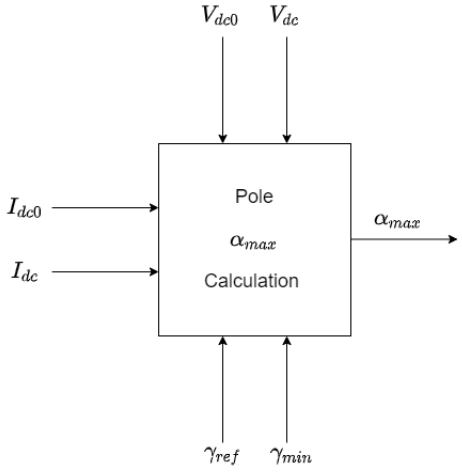


Figure 2.11: Pole α_{max} Calculation [35]

2.4.2.3 Voltage Control Amplifier

A voltage control amplifier (VCA) is used at both the rectifier and inverter stations to control voltage. The VCAs are set up differently in the control loops of the rectifiers and inverters. For simplicity purposes, the VCA at the inverter is described in this section, see Figure 2.12.

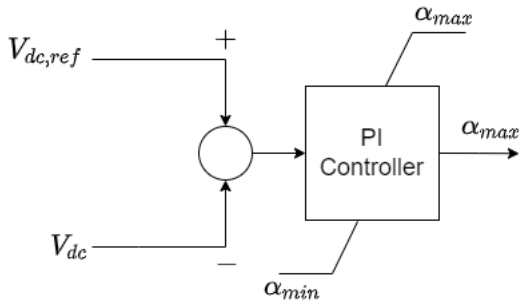


Figure 2.12: Voltage Control Amplifier [35]

Under normal operation, the VCA (realized here with PI controller) is saturated with its reference voltage set at a value higher than the measured pole voltage. When the voltage difference between the reference pole voltage and the measured pole voltage is above the threshold, VCA comes out of saturation and actively controls voltage [35]. The input polarity of the measured pole voltage determines whether a rectifier station or an inverter station requires active voltage control, through logic operations [35]. Another way to get VCA out of saturation is to reduce the reference voltage itself [35]. As shown in Figure 2.12, the VCA outputs an α_{max} value to be used in the lower level current control logics, see Figure 2.10.

2.4.2.4 Current Control Amplifier

Under normal operation ($I_{dc} = I_{dc0}$), the rectifer stations regulates LCC current. Figure 2.13 illustrates a simplified setup of the current control amplifier (CCA), realized using a PI controller.

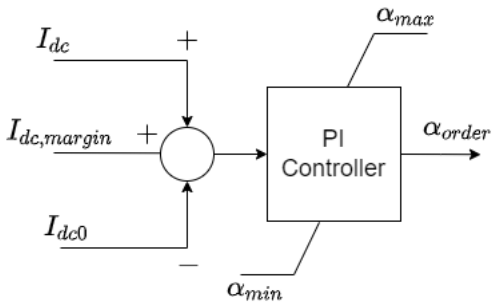


Figure 2.13: Current Control Amplifier [35]

$I_{dc,margin}$ is an additional input used in the CCA at the inverter side only. It is used to keep the inverter CCA saturated at its upper limit as long as $0\ p.u \leq I_{dc,margin} \leq 0.2\ p.u$ [35]. If $I_{dc,margin} > 0.2\ p,u$, inverter CCA is actively controlling current with a reference current of $I_{dc} = I_{Idc0} - I_{dc,margin}$ [35]. In this work, $I_{dc,margin}$ is set to 0.3 kA (corresponds to 0.1 $p.u$ of hte main DC link current).

2.4.2.5 Converter Firing Controls

To generate firing pulses for the thyristors, the converter uses a transvector control method as shown in Figure 2.14 below.

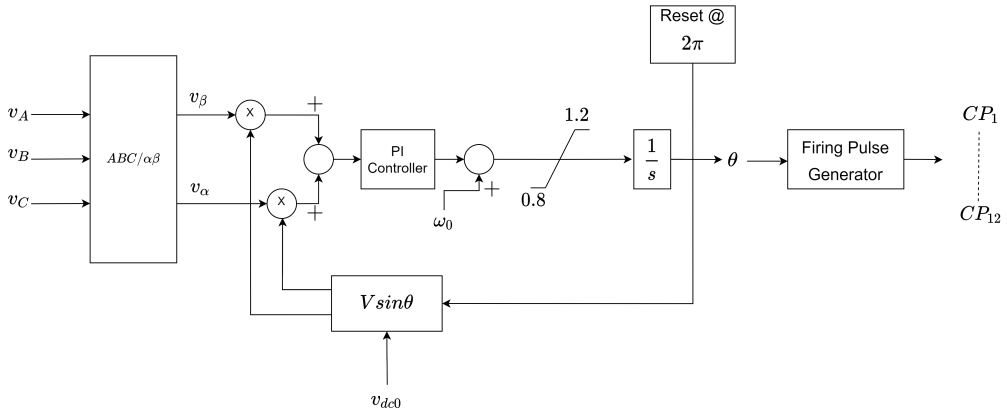


Figure 2.14: Converter Firing Control Scheme [35]

The control scheme makes use of an oscillator determined by the ac voltage of the bipole system to generate a ramp output. This ramp output is then compared to a specific reference to generate firing pulses. To ensure that the firing pulses are equally spaced, the ramp generator is decoupled from the ac system through the use of PI controllers [35].

2.4.2.6 Voltage Dependent Current Order Limit (VDCOL)

VDCOL is another important control component of the bipole LCC control system in Figure 2.10. Its function is to reduce the current order when the DC voltage detected is lower than normal. Figure 2.15 shows the control method for the VDCOL.

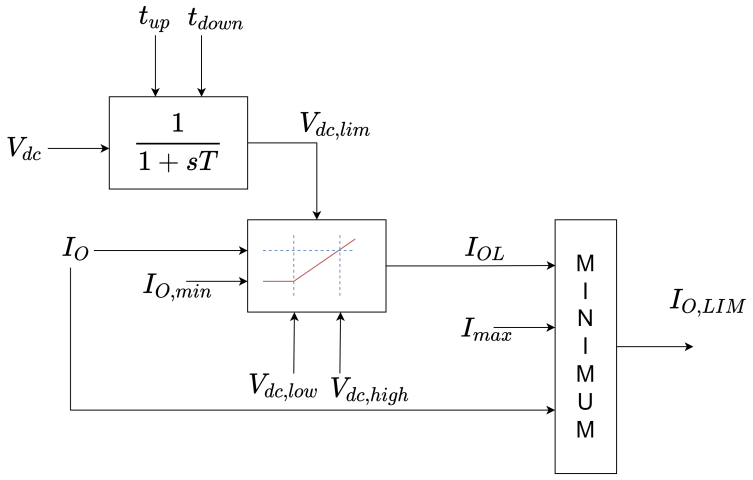


Figure 2.15: Voltage Dependent Current Order Limit Control [35]

VDCOL has a very important role to play when it comes to both AC and DC faults. During AC faults, if the current order is reduced, the reactive power consumption of the converters is also reduced [35]. Similarly, during a DC fault, the rectifier's reactive power consumption is reduced, reducing the severity of this fault on the AC network [35]. In both cases, VDCOL helps with the post-fault recovery of the converter stations. Recovery times can also be varied through the parameters of this control component.

2.4.2.7 Other Control Schemes

The LCC bipole control system also makes use of several other control schemes, which are not shown in detail in Figure 2.10 but are explained in [35]. These are summarized briefly below:

1. **Tap changer controls (TCC)**: At the rectifier, the TCC ensures that $12.5° \leq \alpha \leq 17.5°$ while at the inverter, the TCC ensures that rectifier DC voltage is as close to 1 p.u as possible. This method of controlling rectifier DC voltage through the inverter can only be feasible if the inverter is running α_{max} or γ_{min} control and not while the inverter is in VCA or CCA operation modes. In this work, the tap changer controls activate once monitored parameters exceed their threshold values for 1 second.

2. **Bipole Power Control Modes**: This component ensures that power flow is constant during minor fluctuations in the converter bus voltages. It also allows one pole to compensate another pole for power limitations. In this study, balanced bipole power control (BBPC) is used. Unbalanced bipole power control (UBPC) along with pole current control are also available but are left unused.

3. **Current Order Synchronization**: This control component uses the calculated current order variations and applies it accordingly to the rectifier and inverter stations. Increases in current order are applied at the rectifier station first while reductions are applied at the inverter stations first.

4. **Current Margin Compensation (CMC)**: This control component makes use of a "slow speed feedback regulator" to account for current reductions when inverter current control is active for longer periods of time.

5. **Rectifier Alpha Minimum Limiter (RAML)**: This acts as the AC fault detector and it increases the rectifier's minimum alpha reference value. The increase is directly dependent on the severity of the AC fault.

6. **Commutation Failure Protection**: Commutation failures are detected easily by comparing the pole DC current to the rectifier side transformer secondary current. If $I_{dc,pole} > I_{secondary,R}$, commutation failure has occured and there is a 5° increase in the γ_{ref} value to try and reduce the occurrence of consecutive commutation failures.

7. **DC Line Fault Protection**: In the LCC bipole system, faults are detected through voltage measurement of $V_{dc,pole}$. If this voltage gets too low, the DC line fault protection scheme becomes active, but only at the rectifier side. When a fault is detected, a retard of the firing angle occurs and the DC current through the pole is extinguished. After a specific

interval of time, restart orders are put in place to reestablish the DC current. If a fault is still present, the waiting interval increases before another restart order is sent. If after a third restart attempt the current is still not reestablished, the pole is blocked. Pole power compensation also takes place since the healthy pole will be directly affected by a DC fault in the other pole. To minimize the risk of commutation failure in the healthy pole, the γ_{ref} is increased while the fault is active and the system has not recovered.

2.4.3 M2DC-CT Input Filter Design

Each M2DC-CT tapping station in Figure 2.9 uses an input filter denoted by Z_{filter}. This filter is needed to suppress mainly second order harmonic currents that are drawn by the M2DC-CT. This is to reduce voltage/power losses and to also keep the total harmonic distortions within an acceptable limit. In general, filtering can be achieved through two main methods:

- Active Filtering - Making use of M2DC-CT controls to reduce the input current harmonics by appropriate control actions.
- Passive Filtering - Making use of additional physical components such as capacitors, inductors and resistors to suppress/eliminate the input currnt harmonic components. This is the approach adopted in this work.

Active filtering avoids adding extra physical components. This section shows a comparison between the input and output current waveforms of the M2DC-CT when using the aforementioned methods of filtering to motivate why passive filtering was adopted in this thesis.

Active filtering was implemented by adding resonant controllers to suppress the second order and fourth order harmonics observed in both the i_{t1} and i_{t2} measured waveforms, as both the input and output currents can be expressed using these two abstract variables, see Figures 2.7(b) and 2.9. For passive filtering, two parallel LC filters were added in series as shown in Figure 2.16 and were tuned as described in [17] with a quality factor of 60. The damping resistance added is used to obtain the targeted quality value.

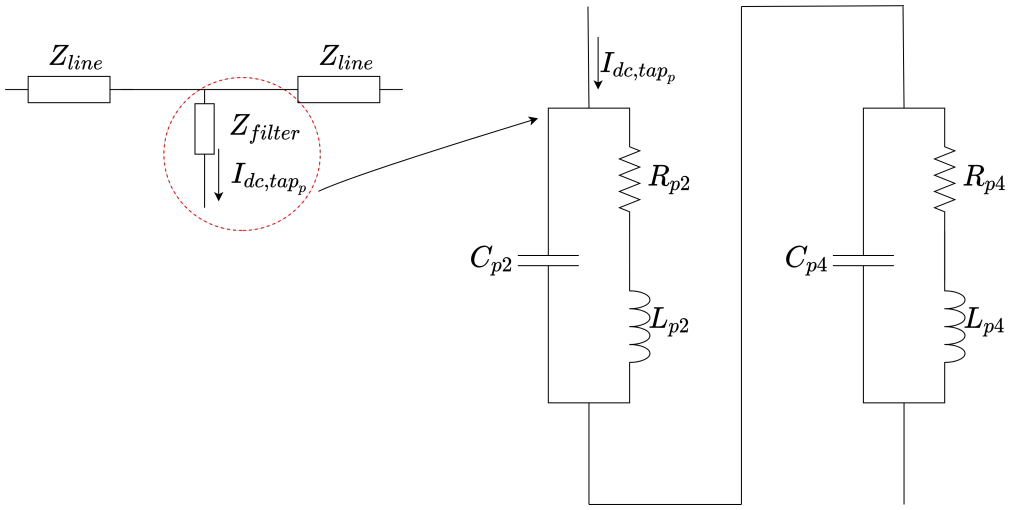


Figure 2.16: Parallel LC Filters (Z_{filter}) used at M2DC-CT inputs in Figure 2.9 [17]

where, $L_{p2} = 0.0025\ H, C_{p2} = 112.5\ \mu F$ and $R_{p2} = 0.07854\ \Omega$ for the second order harmonic filter at 300 Hz and $L_{p4} = 0.0025\ H, C_{p4} = 28.1\ \mu F$ and $R_{p4} = 0.1578\ \Omega$ for the fourth order harmonic filter at 600 Hz.
The FFT analysis of the M2DC-CT input dc current ($i_{dc,tap}$) obtained when tapping rated power of $P_{dc} = 75\ MW$ is shown in Figure 2.17:

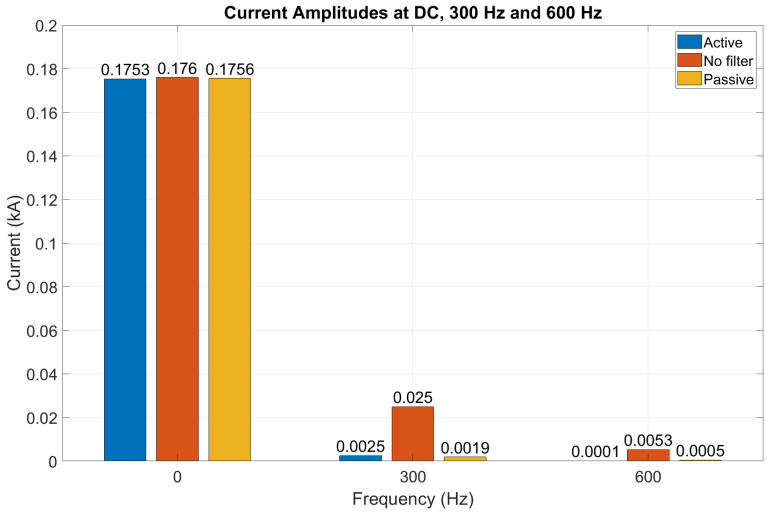


Figure 2.17: FFT Analysis of $i_{dc,tap}$ at $P_{dc} = 75\ MW$ considering different filtering Schemes

With a power demand of 75 MW and the M2DC-CT output voltage set

at 40 kV, the ideal dc output current is

$$I_{dc,out} = \frac{P_{dc}}{V_{dc,out}} = 1.875\ kA \tag{2.39}$$

Due to HVDC line voltage drops and power losses in the M2DC-CT, the M2DC-CT input current, $I_{dc,tap}$, has a dc component of approximately 0.175 kA. Observe from Figure 2.17 that the passive and active filtering provide similar levels of harmonic attenuation at both second and fourth harmonics. However, undesirable control interactions between the two M2DC-CTs were observed during simulated test cases when implementing the latter, which sometimes led to converter instability. Solving this control interaction problem would require detailed inter-converter harmonic analysis that is outside the scope of this thesis. Therefore, given the systems level focus of this work, the converter level passive filtering solution of Figure 2.16 was adopted.

Figure 2.18 shows the response from the M2DC-CT when power demand is ramped up to 75 MW at $t = 0.25s$ with a ramp rate of 750 MW/s. From Figures 2.18 and 2.19, it can be seen that the unwanted second and fourth order harmonics have been effectively attenuated. The total harmonic distortion (THD) of $I_{dc,tap}$ is 6.1% and for $I_{dc,out}$, the THD is less than 1% at rated power ($P_{dc} = 75\ MW$). The results are the same for the DC tapping station on the negative pole and thus only the results from the positive pole tapping station are shown in Figures 2.18 and 2.19.

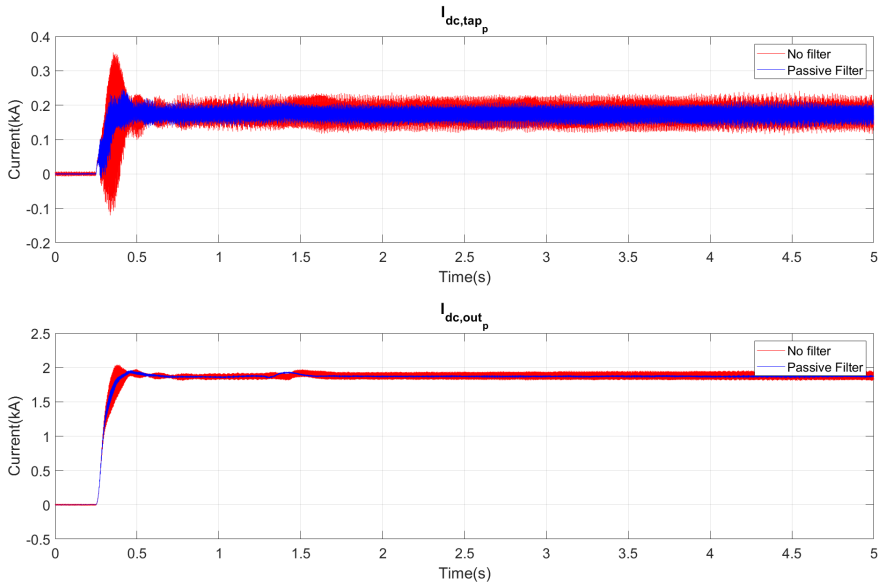


Figure 2.18: I_{dc,tap_p} and I_{dc,out_p} for $P_{dc} = 75\ MW$ demand initiated at $t = 0.25s$

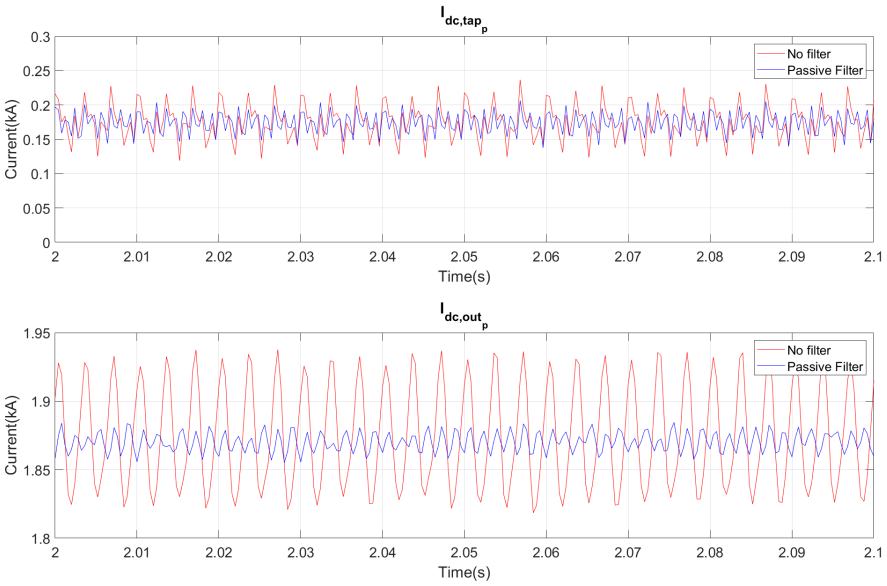


Figure 2.19: Steady state: I_{dc,tap_p} and I_{dc,out_p} waveforms of Figure 2.18

2.5 Summary

This chapter begins by providing an overview on the design and operating principle of classical LCCs and two-leg single phase MMCs. It then introduces

the LCC bipole system augmented with two M2DC-CTs and their control approach as well as the filter design in this hybrid HVDC system. The design of the M2DC-CT allowed for a high voltage ratio DC-DC converter to link the HVDC bipole to an MVDC bus (12.5:1 ratio). The M2DC-CT consists of 460 FBSMs in the upper arms and 40 HBSMs in the lower arms. The FBSMs purpose is to block the flow of DC fault currents through the M2DC-CT to prevent any significant damage to the components. As for the M2DC-CT control system, since Σ-Δ quantities did not achieve frequency decoupling in both the current and voltage quantities, 'c' and 't' variables were introduced and consequently used for the control mechanism. The LCC-HVDC bipole system is a typical $\pm 500\ kV$ symmetrical bipole and has all the controls required from current and voltage controls to fault responses whether they are AC faults or DC faults. The filter design in the link between the M2DC-CT tapping stations and the HVDC link has also been described and showed that passive filtering worked better in this case compared to active filtering, due to the unwanted control system interactions happening between M2DC-CTs when the two tapping stations were simultaneously in use.

Chapter 3

Power Flow Studies of Hybrid VSC-LCC HVDC System

This chapter first discusses the pre-charging operation of the hybrid VSC-LCC HVDC bipole system in Figure 2.9 and then presents study results for different system power flow conditions, considering both dynamic and steady-state operations. In these situations, the tapping power demands at both positive and negative pole tapping stations, respectively $P_{dc,p}$ and $P_{dc,n}$, varied from 0 MW to 75 MW (0 to 1 p.u). Both symmetrical and asymmetrical power tapping scenarios are studied, where the former and the latter correspond to $P_{dc,p} = P_{dc,n}$ and $P_{dc,p} \neq P_{dc,n}$, respectively. When $P_{dc,p} = P_{dc,n}$, the power demand is referred to as a general P_{dc} term for both tapping stations since they are equal.

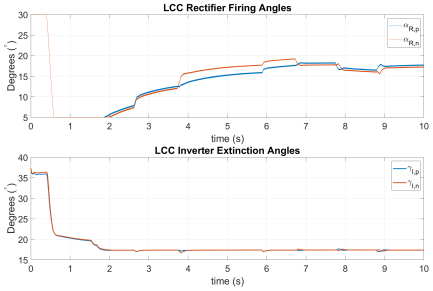
3.1 Normal LCC Operation with Zero Power Tapping Demand

Under normal operation of the LCC Bipole system, each M2DC-CT is idle (i.e $P_{dc} = 0\ MW$ at each tapping station) and does not affect any of the power flows of the exisiting LCC system. Specifically, each M2DC-CT tapping station is actively regulating $P_{dc} = 0\ MW$ through the converter controls presented in section 2.3.1. The DC current flowing from the rectifier to the inverter is at 3 kA ($\equiv 1p.u$) at both poles while the DC link voltage is nominally 500 kV ($\equiv 1p.u$).

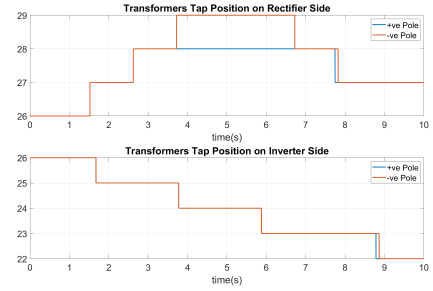
3.1.1 Precharging the Hybrid VSC-LCC HVDC System

Before carrying out any studies, we have to make sure that both the LCC Bipole system and the M2DC-CT tapping stations are energized properly. The startup of the LCC system is shown in Figure 3.1.

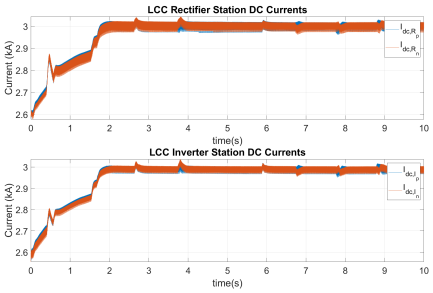
3.1.1.1 LCC System Startup Sequence



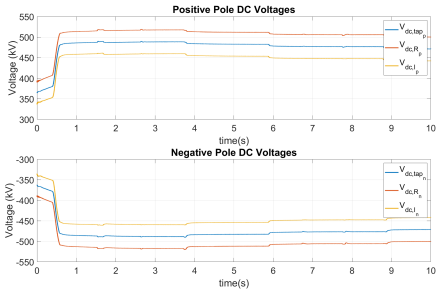
(a) Firing and Extinction Angles



(b) Transformer Tap Position



(c) LCC Rectifier and Inverter Currents



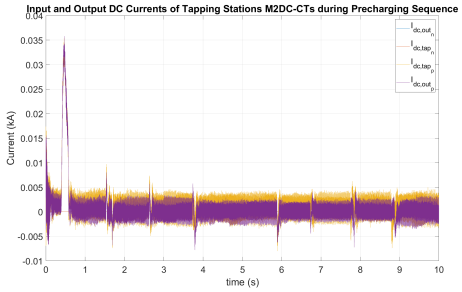
(d) LCC Rectifier and Inverter Voltages

Figure 3.1: Precharging Results for LCC System with P_{dc} set at 0 MW

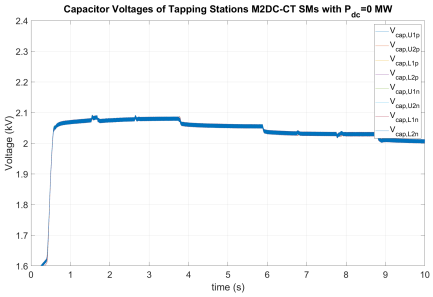
The rectifier firing angles and the inverter extinction angles (α and γ) are shown to slowly stabilize to their reference values towards the tail end of the graphs. Similarly, the tap position of the transformers at both the rectifier and inverter sides are shown to increase over their reference but stabilize again. As for the LCC DC currents, they rapidly reach their reference value of 1 p.u (i.e 3 kA) with a ripple of about 1%. As for the DC voltages, their variation is directly related to the transformer taps. At the beginning, the voltages go above their reference value but slowly come back to their reference value as the tap changer on the transformer also reaches the desired value. For example, the rectifier side DC link voltage is at 1 pu (i.e 500 kV) but due

to power losses along the HVDC link, the voltages at the tap stations and at the inverters are at a lower level. Throughout the whole startup process, P_{dc} demand both tapping stations was set to 0 MW. Figure 3.1 confirms that the LCC-HVDC system can energize properly when the tapping stations are physically connected to the HVDC lines, as adopted in Figure 2.9.

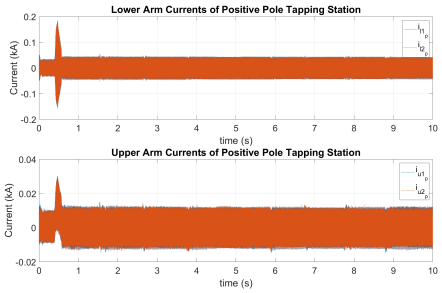
3.1.1.2 M2DC-CTs Startup Sequence



(a) Tapping and Output DC Currents of M2DC-CT



(b) SM Capacitor Voltage of M2DC-CT



(c) Arm Currents of M2DC-CT

Figure 3.2: Precharging Results for M2DC-CT with P_{dc} set at 0 MW at each tapping station

For the two M2DC-CTs, the precharge procedure is dependent on the voltage of the DC link at their respective tapping points. The output side (i.e 40 kV side in Figure 2.9)of the DC-DC converters are left open via an isolating switch until the submodule capacitor voltages reach their set voltage of 2 kV. Once the capacitor voltages stabilize at 2 kV, the output side of each M2DC-CT can be connected to the 40 kV DC bus via appropriate switchgear (not studied in this work). Figure 3.2 shows the main quantities of the M2DC-CTs during the pre-charging sequence. As seen in Figure 3.2(b), once the submodule capacitor

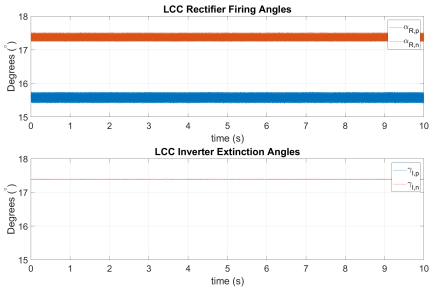
voltages reach their nominal values of 2 kV, they are kept constant from that point onwards and the aforementioned output side switchgear could be used to connect to the 40 kV bus.

3.1.2 Steady State Response

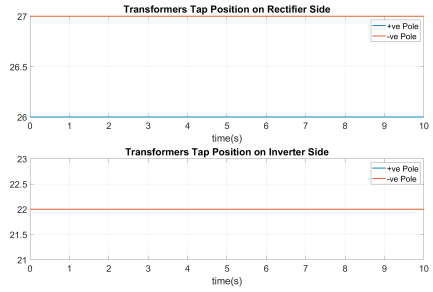
In this section, the steady state operation of the entire hybrid LCC-VSC bipole HVDC system is discussed. Similar to the precharging stage previously discussed, the steady state response is shown in Figures 3.3 and 3.4 where $P_{dc,p} = P_{dc,n} = P_{dc}$ is 0 MW.

3.1.2.1 LCC System

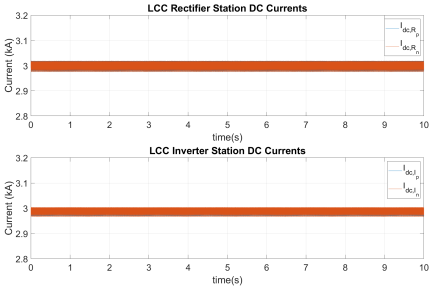
All the components of the LCC-HVDC bipole system are consistently at their reference values with minimal ripples, as shown in Figure 3.3. The steady state values of main components of the LCC-HVDC Bipole are given in Table 3.1. Only the major components of the bipole system are being shown.



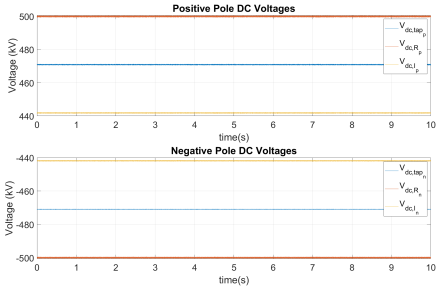
(a) Firing and Extinction Angles



(b) Number of Taps on Transformer



(c) LCC Rectifier and Inverter Currents



(d) LCC Rectifier and Inverter Voltages

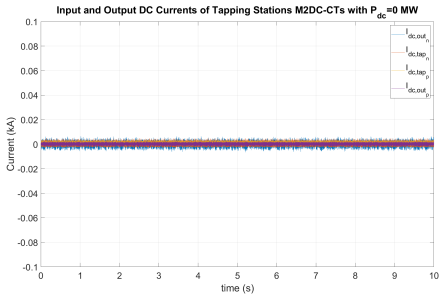
Figure 3.3: Steady State Results for LCC System with P_{dc} set at 0 MW at each pole

Parameter	Notation	Value
Firing Angle of Positive Pole Rectifier	$\alpha_{R,p}$	15.6°
Firing Angle of Negative Pole Rectifier	$\alpha_{R,n}$	17.4°
Extinction Angle of Positive Pole Inverter	$\gamma_{I,p}$	17.4°
Extinction Angle of Negative Pole Inverter	$\gamma_{I,n}$	17.4°
Rectifier Currents (Average Value)	I_{dc,R_p}	3 kA
	I_{dc,R_n}	3 kA
Inverter Currents (Average Value)	I_{dc,I_p}	3 kA
	I_{dc,I_n}	3 kA
Transformer Taps Position	$Taps_{R,p}$	26
	$Taps_{R,n}$	27
	$Taps_{I,p}$	22
	$Taps_{I,n}$	22
Rectifier Side Voltages (Average Value)	V_{dc,R_p}	500 $kV(1\ p.u)$
	V_{dc,R_n}	500 $kV(1\ p.u)$
Tapping Station Voltages (Average Value)	V_{tap_p}	469 $kV(0.94\ p.u)$
	V_{tap_n}	469 $kV(0.94\ p.u)$
Inverter Side Voltages (Average Value)	V_{dc,R_p}	441 $kV(0.88\ p.u)$
	V_{dc,R_n}	441 $kV(0.88\ p.u)$

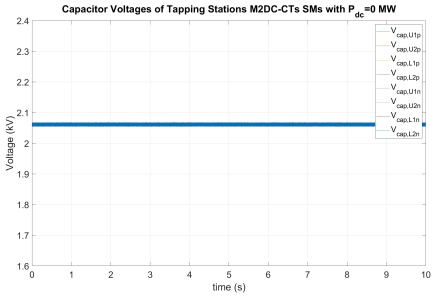
Table 3.1: Steady State Values of LCC-HVDC Bipole System, $P_{dc,p} = P_{dc,n} = P_{dc} = 0\ MW$

The values in Table 3.1 are reached within the first $15s$ from starting up the system, and are considered the threshold values used when analyzing the effects of different power demands of the tapping stations on the LCC-HVDC Bipole system in subsequent sections.

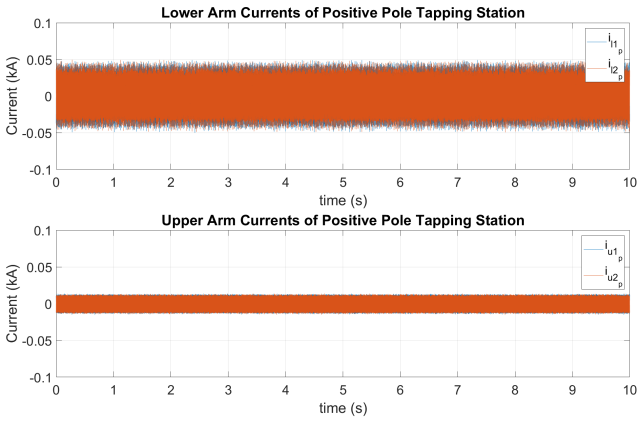
3.1.2.2 M2DC-CTs



(a) Tapping and Output DC Currents of M2DC-CT



(b) SM Capacitor Voltage of M2DC-CT



(c) Arm Currents of M2DC-CT at Positive Pole Tapping Station

Figure 3.4: Steady State Results for M2DC-CT with P_{dc} set at 0 MW at each pole

Figure 3.4 shows the response of both M2DC-CTs at steady state with P_{dc} is 0 MW. As expected, given the power tapping demand is zero, there is no current flowing in the arms and the tapping DC currents as well as the output DC currents are nearly zero. Similar to the LCC quantities, all the M2DC-CTs quantities reach their steady state values within the first 15s of starting up. From Figure 3.4(b), the capacitor voltages are near the desired steady voltage of 2 kV. Figure 3.4(c) demonstrates the arm currents of the positive pole tapping station. The negative pole tapping station has the same arm currents values and variation.

3.2 Symmetrical DC Tapping

During symmetrical DC tapping, the tapping stations on both the positive and negative poles of the LCC-HVDC system tap the same amount of power, that is, $P_{dc,p} = P_{dc,n} = P_{dc}$. In this study, the simulation sequence is as follows:

1. At $t = 0s$, $P_{dc,p} = P_{dc,n} = 0\ MW$ and the LCC-based bipole HVDC system is operating at steady state.
2. At $t = 1s$, $P_{dc,p} = P_{dc,n} = 37.5\ MW$ and the ramp rate for the power demand is set at 750 MW/s.
3. At $t = 3s$, $P_{dc,p} = P_{dc,n} = 75\ MW$ at the same power ramp rate.
4. At $t = 5s$, $P_{dc,p} = P_{dc,n} = 0\ MW$ at the same power ramp rate.

3.2.1 DC Currents of Hybrid LCC-VSC HVDC System

In this section, the dc currents of the HVDC link at both the rectifier side and the inverter side as well as the input and output dc currents of the MMC-based tapping stations (i.e M2DC-CTs) are plotted.

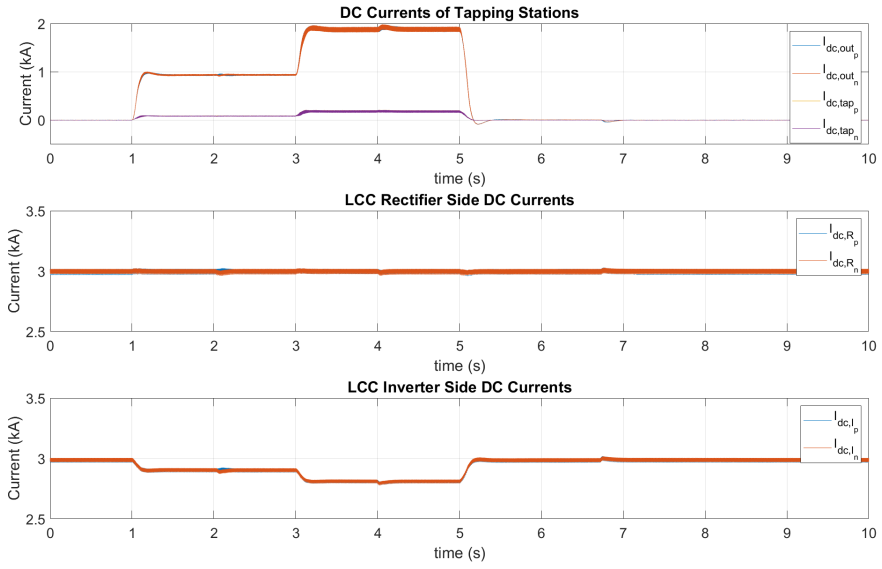


Figure 3.5: DC Currents Variations during Symmetrical Tapping, $P_{dc,p} = P_{dc,n}$

In Figure 3.5, both tapping stations exhibit the same behaviour when the same amount of power is being tapped. For the tapping stations, the DC output current at positive and negative poles is respectively given as:

$$I_{dc,out_p} = \frac{P_{dc,p}}{40\ kV} \tag{3.1}$$

$$I_{dc,out_n} = \frac{P_{dc,n}}{40\ kV} \tag{3.2}$$

while the input side tapping currents are given as:

$$I_{dc,tap_p} = \frac{P_{dc,p_{in}}}{V_{dc,tap_p}} \tag{3.3}$$

$$I_{dc,tap_n} = \frac{P_{dc,n_{in}}}{V_{dc,tap_n}}, \tag{3.4}$$

and consequently, the currents at the inverter side are given by:

$$I_{dc,I_p} = I_{dc,R_p} - I_{dc,tap_p} \tag{3.5}$$

and,

$$I_{dc,I_n} = I_{dc,R_n} - I_{dc,tap_n} \tag{3.6}$$

In this case study, $P_{dc,p_{in}} > P_{dc,p}$ and $P_{dc,n_{in}} > P_{dc,n}$ due to internal losses of the M2DC-CTs. As a result, the power supplied to the converter is higher than the power demand for any P_{dc} ($P_{dc,p} = P_{dc,n}$) value. From Figure 3.5, the measured steady state currents are as follows:

Parameter	$P_{dc} = 0\ MW$	$P_{dc} = 37.5\ MW$	$P_{dc} = 75\ MW$
Time Interval (sec)	$[0, 1)\&[5, 10]$	$[1, 3)$	$[3, 5)$
$I_{dc,tap_p}\ (kA)$	$0\ k$	0.0844	0.176
$I_{dc,tap_n}\ (kA)$	0	0.0843	0.176
$I_{dc,out_p}\ (kA)$	0	0.934	1.875
$I_{dc,out_n}\ (kA)$	0	0.933	1.875
$I_{dc,R_p}\ (kA)$	3	3	3
$I_{dc,R_n}\ (kA)$	3	3	3
$I_{dc,I_p}\ (kA)$	3	2.916	2.823
$I_{dc,I_n}\ (kA)$	3	2.916	2.824

Table 3.2: DC Currents of Hybrid HVDC System during Symmetrical Power Tapping where $P_{dc,p} = P_{dc,n} = P_{dc}$

3.2.2 Firing Angles, Extinction Angles and Transformer Taps

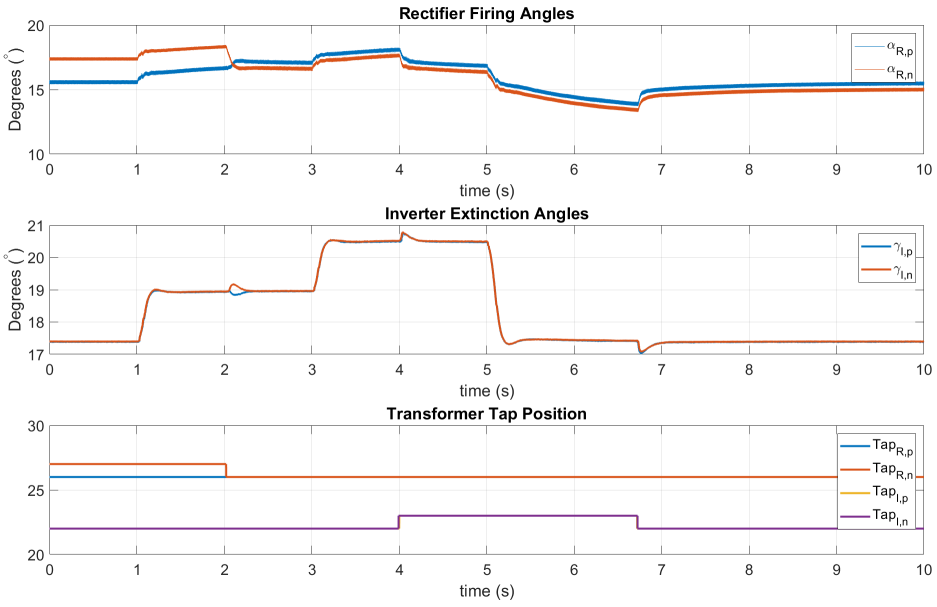


Figure 3.6: Firing Angles, Extinction Angles and Transformer Taps of the LCC Bipole HVDC System, $P_{dc,p} = P_{dc,n}$

Figure 3.6 shows the variation of the rectifier α values, the inverter γ values and the transformer tap positions at different power demands in the range $0s \leq t \leq 10s$.

At $t = 1s$, the first instance of power demand ($P_{dc} = 37.5\ MW$) occurs and both the α and γ values at the rectifier side and inverter side, respectively, start to increase to its designated value as determined by the control loops. Initially, α increases steadily to a maximum value of 18.3° at the positive pole rectifier and 16.6° at the negative pole rectifier. At the same time, the γ values also increase until they reach a steady value of 18.93° at the inverters on both poles. As for the transformer taps, they stay at their initial values of 26 on the positive pole rectifier side, 27 on the negative pole rectifier side and 22 on the inverter side at both poles.

At $t = 2s$, upon detecting that $\alpha_{R,n}$ is above 17.5°, the tap changer controls reduces the number of taps on the negative pole rectifier side to 26 thus causing $\alpha_{R,n}$ to drop to a steady value of 16.6° while $\alpha_{R,p}$ is steady at 17.1°. No major changes happen to the γ values.

At $t = 3s$, the second instance of power demand occurs where P_{dc} is now operating at rated power (75 MW). Similar to the previous power demand, both α and γ increase at the rectifier stations and inverter stations respectively. γ reaches a steady state value of 20.5° while $\alpha_{R,p}$ and $\alpha_{R,n}$ increase to above 17.5° again, at values of 17.9° and 17.6° respectively.

At $t = 4s$, the transformer tap changer controls become active again to reduce α by increasing the number of taps of the transformer on the inverter at both inverter poles from 22 to 23. This causes both $\alpha_{R,p}$ and $\alpha_{R,n}$ to drop to 16.8° and 16.4° respectively.

At $t = 5s$, there are no more power demands at either tapping stations, i.e. $P_{dc} = 0\ MW$. Both α and γ are now decreasing and in this instance, α at both stations reach values below 12.5° while γ becomes constant at approximately 17.4° which is its reference value.

At $t = 6.7s$, the number of taps on the transformer at the inverter sides drop down to 22 again to increase the $\alpha_{R,p}$ and $\alpha_{R,n}$ to drop to steady state values of 15.4° and 14.9° respectively.

3.2.3 M2DC-CT Quantities

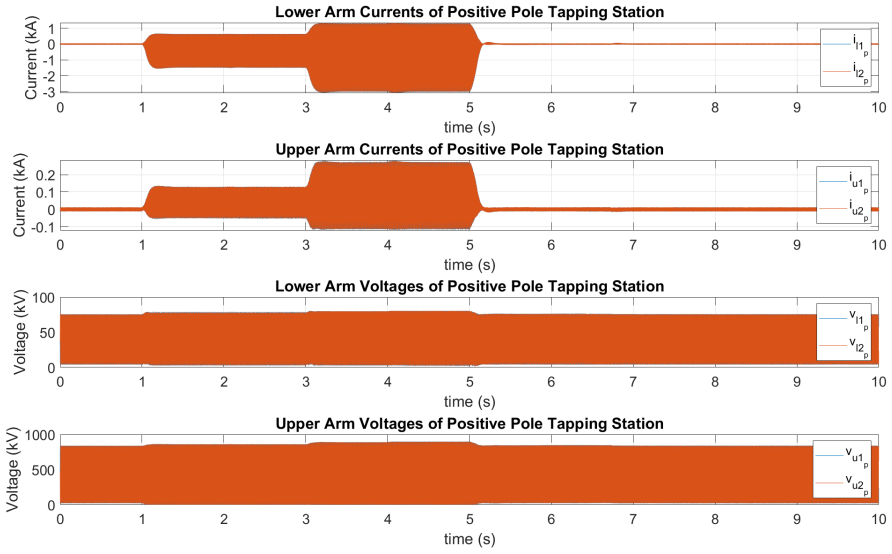


Figure 3.7: Arm Currents and Voltages of Positive Pole Tapping Station M2DC-CT, $P_{dc,p} = P_{dc,n}$

Figure 3.7 shows the variation of the M2DC-CT arm currents and arm voltages during symmetrical tapping. Only the positive pole M2DC-CT results are being shown since both positive and negative poles tapping stations behave the same way.

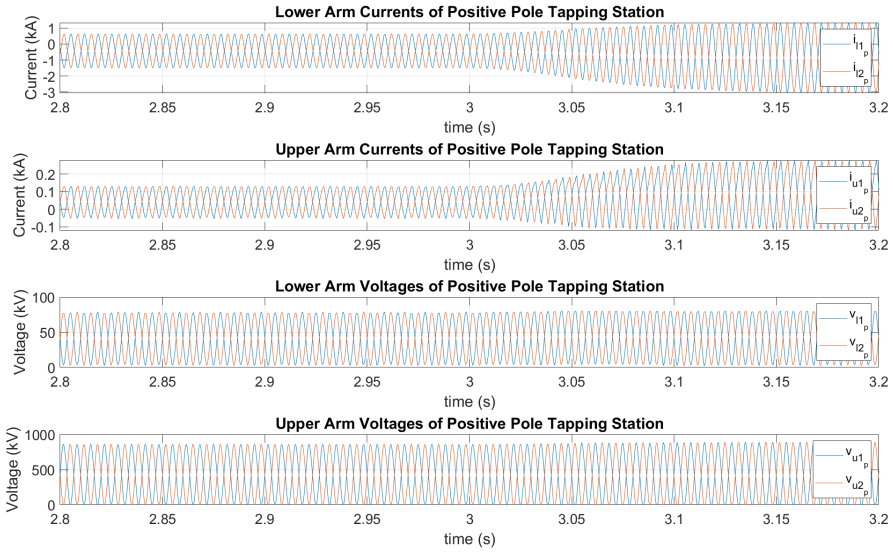


Figure 3.8: Arm Currents and Voltages of Positive Pole Tapping Station M2DC-CT, $P_{dc,p} = P_{dc,n}$ for $2.8 \leq t \leq 3.2$

Figure 3.8 provides a closer look as to how the arm currents and arm voltages in the positive pole tapping station vary at $t = 3s$. As shown, the fundamental frequency of arm currents in the upper arms are flowing in opposite phases of each other. The same principle applies to the lower arm currents as well as the upper and lower arm voltages. The arm currents and the arm voltages also have DC components. The two upper arms have the same DC components for the currents and voltages. The two lower arms follow the same principle.

Similarly, Figure 3.9 shows the capacitor voltages at the positive pole tapping station. Observe the SM capacitor voltages are well regulated near their nominal 2 kV value.

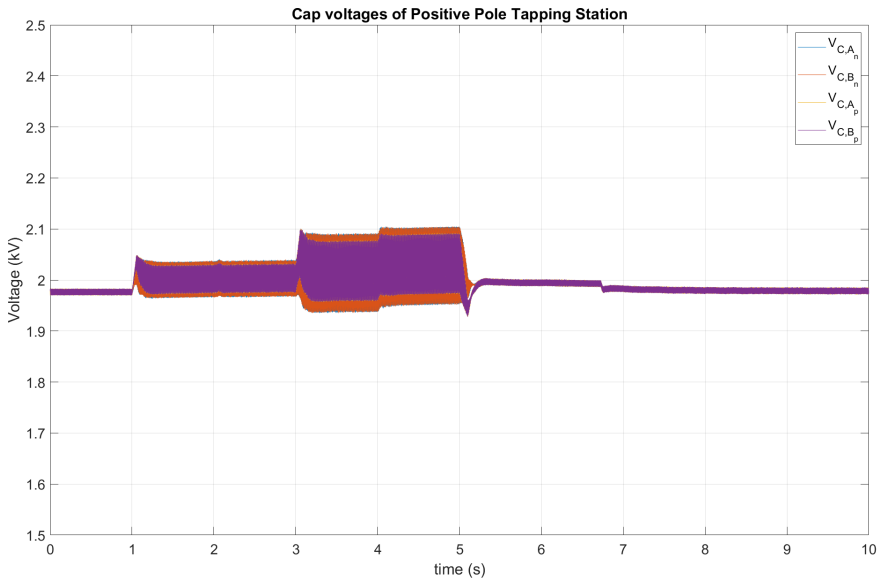


Figure 3.9: Capacitor Voltages of SMs in the Positive Pole Tapping Station where $P_{dc,p} = P_{dc,n}$

At t = 1s: $P_{dc,p} = P_{dc,n} = P_{dc} = 37.5\ MW$ and arm currents of both the upper and lower arms increase to 0.0732 kA_{rms} and 0.822 kA_{rms} respectively with peak current magnitudes of 0.131 kA and 1.475 kA. As for the arm voltages, the RMS values are set at 425.97 kV and 48.70 kV in the upper and lower arms respectively. As for the capacitor voltages, they are set at 2 kV. With increasing power demands, the voltage ripples also increase. In this case, voltage ripples are at 1.38% and 1.75% for the capacitors in the upper and lower arms respectively, at rated power.

At t = 3s: P_{dc} is increased from 37.5 MW to 75 MW. Consequently, the arm currents and voltages amplitudes both increase. The currents increase by a factor of two as they are directly proportional to the power demand. Therefore, for the arm currents, the upper arms have RMS values of 0.146 kA and 1.695 kA with peak magnitudes of 0.272 kA and 3.004 kA respectively. As for the arm voltages, there are increases in their RMS values as well. For the upper arms, the RMS value is 524.69 kV while for the lower arms, the arm voltage is at 50.40 kV. With the increase in both the voltages and currents, the voltage ripples in the capacitor voltages become 3.75% and 3.1% respectively.

At t = 5s: P_{dc} is set to zero and all quantities return to their initial state (at $t = 0s$).

3.3 Asymmetrical DC Tapping

Asymmetrical power tapping occurs when the positive and negative pole tapping stations extract unequal powers from the LCC-HVDC system, that is, $P_{dc,p} \neq P_{dc,n}$. To demonstrate asymmetrical tapping, the power demand of the positive pole tapping station is twice that of the negative pole tapping station. However, the two values can be anything between 0 MW and 75 MW as long as they are different. The simulated tapping sequence follows a similar methodology to the symmetrical tapping study and is as follows:

1. At $t = 0s$, $P_{dc,p}$ and $P_{dc,n}$ are 0 MW and the LCC-based bipole HVDC system is operating at steady state.

2. At $t = 1s$, $P_{dc,p} = 37.5\ MW$ and $P_{dc,n} = 18.75\ MW$ (i.e $P_{dc,p} = 2 \times P_{dc,n}$) and the ramp rate for the power demand is set at 750 MW/s.

3. At $t = 3s$, $P_{dc,p} = 75\ MW$ and $P_{dc,n} = 37.5\ MW$ (i.e $P_{dc,p} = 2 \times P_{dc,n}$) at the same power ramp rate.

4. At $t = 5s$, $P_{dc,p}$ and $P_{dc,n}$ decrease to 0 MW at the same power ramp rate.

3.3.1 DC Currents of Hybrid LCC-VSC HVDC System

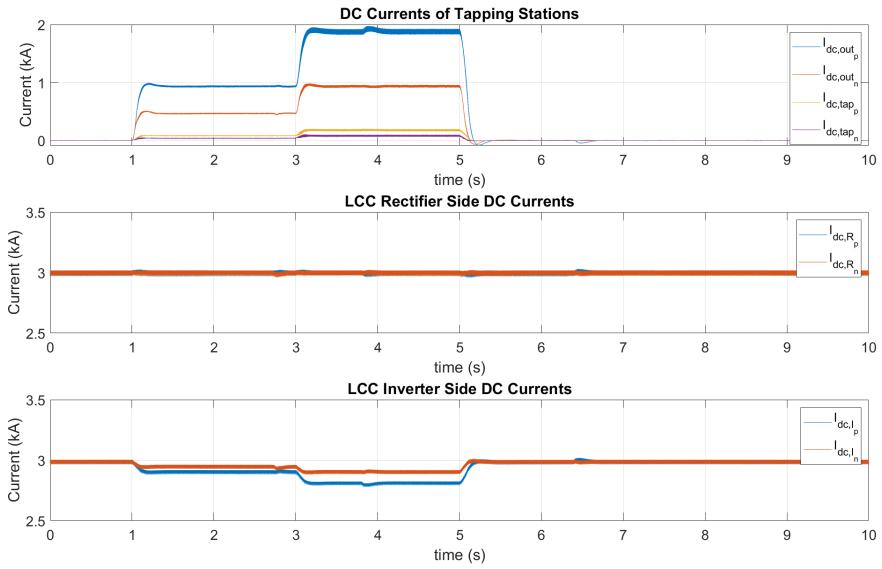


Figure 3.10: DC Currents Variations during asymmetrical Tapping, $P_{dc,p} = 2 \times P_{dc,n}$

Figure 3.10 shows the current variations of the tapping stations DC currents as well as the rectifier and inverter DC currents of the bipole. The differences between the tapping station DC currents are quite noticeable with the positive pole tapping station currents being twice as big and take approximately twice as much time to reach their intended value. Rectifier DC currents remain unchanged (due to current control enforced by the LCC-HVDC system) while inverter DC currents decrease by the same amount as the input tapping currents increase. Essentially, the tapping currents and the output currents at the negative pole tapping station is half that of the positive pole tapping station as the stations have the same parameters. Therefore, the following ratios apply for all P_{dc} values at both stations:

$$\frac{P_{dc,p}}{P_{dc,n}} = \frac{I_{dc,tap_p}}{I_{dc,tap_n}} = \frac{I_{dc,out_p}}{I_{dc,out_n}} \tag{3.7}$$

3.3.2 Firing Angles, Extinction Angles and Transformer Taps

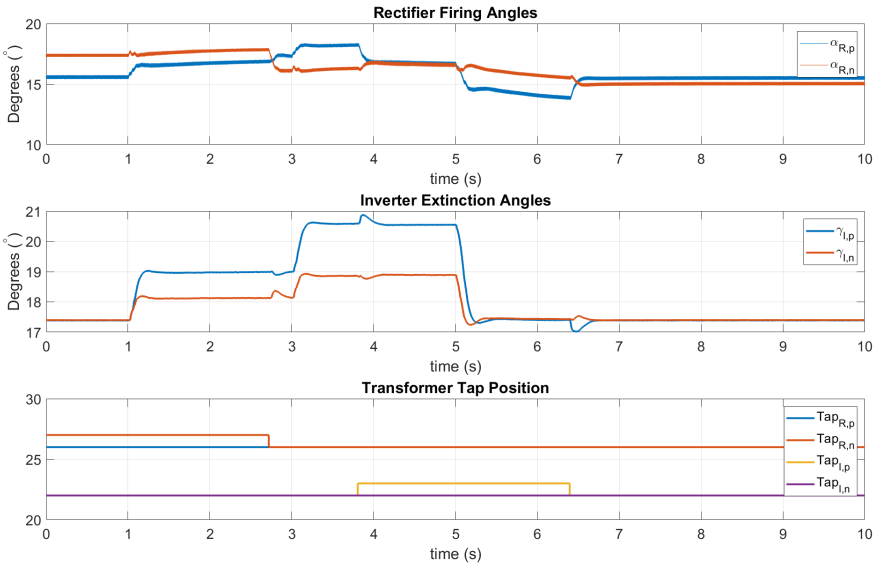


Figure 3.11: Firing Angles, Extinction Angles and Transformer Taps of the LCC Bipole HVDC System, $P_{dc,p} = 2P_{dc,n}$

Now that the power demands are different at the two tapping stations, the firing angles, extinction angles and the transformer taps will all vary. As compared to Figure 3.6, the firing angles in Figure 3.11 do not follow each other as closely while the extinction angles are different but follow the same trend as the tapping DC currents. As for the transformer tap positions, they occur at different times as well. In this case, there are three instances where the number of taps change in the transformers:

1. At $t = 2.719s$, $\alpha_{R,n}$ exceeds 17.5° from the first power demand scenario and the number of taps at the negative pole rectifier decreases from 27 to 26.

2. At $t = 3.805s$, $\alpha_{R,p}$ is now above the threshold as power demand had increased at $t = 3s$ and the number of taps at the positive pole inverter side transformer increases to 23.

3. At $t = 6.395s$, P_{dc} is now 0 MW (P_{dc} is set to 0 at $t = 5s$) in both tapping stations and $\alpha_{R,p}$ is now below 12.5° causing $Tap_{I,n}$ to decrease back to 22.

As for $\gamma_{I,p}$ and $\gamma_{I,n}$, they go through a minor transient period when tap changes occur but they reach their required values at the same time as the tapping station DC currents. The different steady state values of extinction angles at both the positive pole inverter station and negative pole inverter station are shown in Table 3.3.

Parameter	$P_{dc,p} = P_{dc,n} = 0\ MW$	$P_{dc,p} = 37.5\ MW$	$P_{dc,p} = 75\ MW$
		$P_{dc,n} = 18.75\ MW$	$P_{dc,n} = 37.5\ MW$
$\gamma_{I,p}$	17.4°	18.98°	20.54°
$\gamma_{I,n}$	17.4°	18.13°	18.88°

Table 3.3: Steady State Extinction Angles at the Inverter stations for Different Power Demands during Asymmetrical Tapping

Observe that during asymmetrical power transfer, both LCC rectifier stations successfully maintain dc link current control as I_{dc,R_p} and I_{dc,R_n} stay at 3 kA as shown in Figure 3.10.

3.3.3 M2DC-CT Quantities

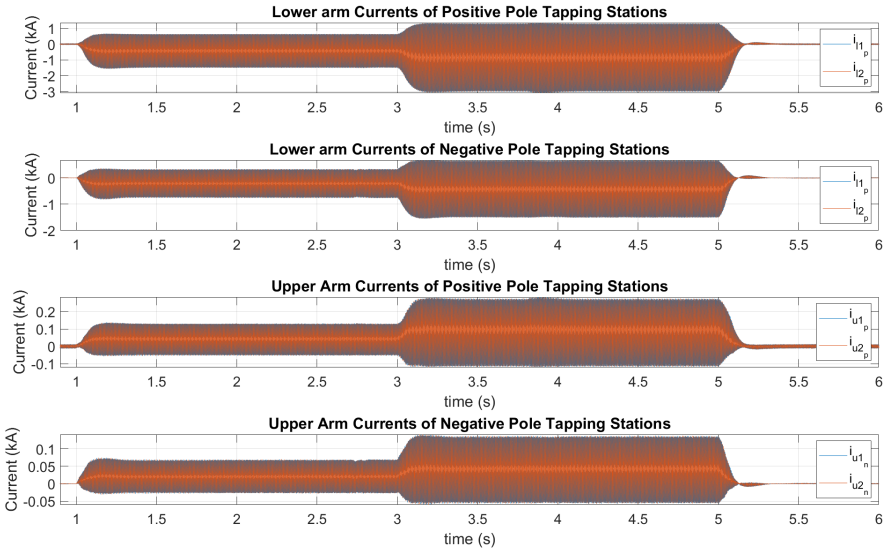


Figure 3.12: Arm Currents of Tapping Stations M2DC-CTs, $P_{dc,p} = 2P_{dc,n}$

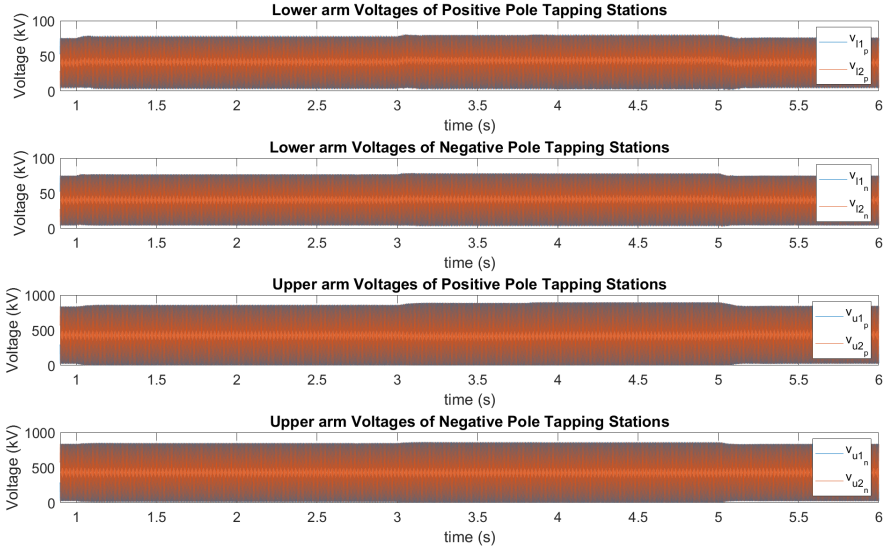


Figure 3.13: Arm Voltages of Tapping Stations M2DC-CTs, $P_{dc,p} = 2P_{dc,n}$

With the $P_{dc,n}$ being half $P_{dc,p}$, the RMS values of the tapping DC currents and output DC currents of the tapping station at the positive pole is twice that

at the negative pole (except when $P_{dc,p} = P_{dc,n} = 0\ MW$). As demonstrated in Figure 3.12, the peak magnitudes for the arm currents of the positive pole tapping station are twice that of the negative pole tapping station. As for the arm voltages in Figure 3.13, the RMS values as well as the peak to peak values are larger in the positive pole tapping station as well.

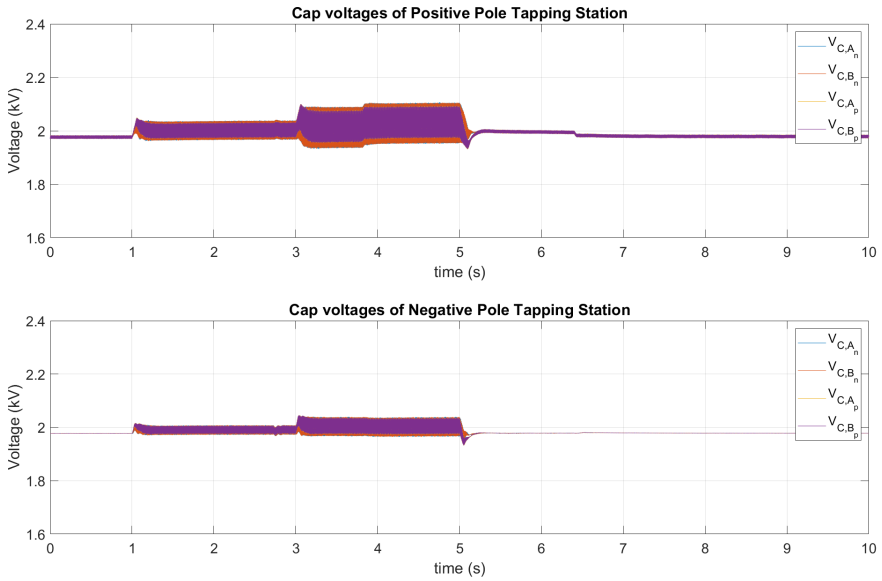


Figure 3.14: Capacitor Voltages of SMs in the Tapping Stations, $P_{dc,p} = 2 \times P_{dc,n}$

From Figure 3.14, similar to the capacitor voltage variations in Figure 3.9, only the peak to peak voltage ripples vary based on the power demand. The average value of the capacitor voltages is approximately 2.0 kV in all the cases, with the voltage ripples being consequently smaller at the negative pole tapping station.

3.4 Power Injection for Renewable Energy Integration

The previous studies all concerned tapping power from the HVDC bipole system. In this section, the effect of power injection back into the LCC-Based HVDC Bipole system is investigated and discussed. The positive pole station

will continue behaving as a tapping station, removing power from the positive pole while the negative pole station now acts as an power generating station, mimicking renewable energy sources. The simulation is set up as follows:

1. At $t = 0s$, $P_{dc,p}$ and $P_{dc,n}$ are 0 MW and the LCC-based bipole HVDC system is operating at steady state.

2. At $t = 1s$, $P_{dc,p} = 37.5$ MW and $P_{dc,n} = -37.5$ MW and the ramp rate for the power demand is set at 750 MW/s.

3. At $t = 3s$, $P_{dc,p} = 75$ MW and $P_{dc,n} = -75$ MW at the same power ramp rate.

4. At $t = 5s$, $P_{dc,p}$ and $P_{dc,n}$ decrease to 0 MW at the same power ramp rate.

The negative power demands values show the direction of the power flow and in this case, the negative pole station is supplying power to the LCC-HVDC bipole system.

3.4.1 DC Currents of Hybrid LCC-VSC HVDC System

The variation of the DC currents for both the LCC and the tapping stations are shown in Figure 3.15.

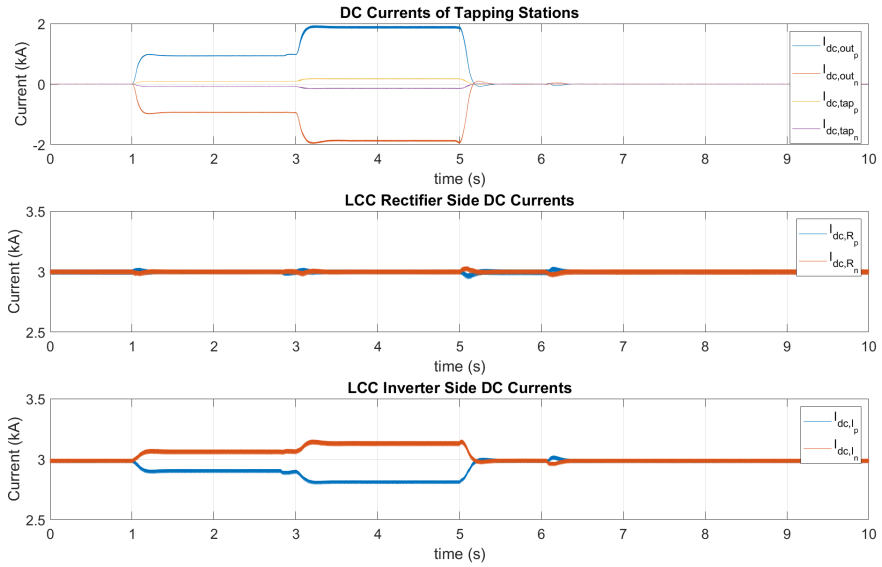


Figure 3.15: DC Currents Variations when $P_{dc,p} = -P_{dc,n}$

As it can be seen, the response of the negative pole tapping station is opposite that of the positive pole tapping station as the current flow is reversed when a particular tapping station is feeding power to the LCC-HVDC bipole system. This demonstrates the feasibility of adding renewable resources for energy generation as well as distributed energy resources (DERs) to supply existing LCC-HVDC systems with more power.

The RMS values of the DC currents for this case are shown in table 3.4.

Parameter	$P_{dc,p} = 0\ MW$	$P_{dc,p} = 37.5\ MW$	$P_{dc,p} = 75\ MW$
	$P_{dc,n} = 0\ MW$	$P_{dc,n} = -37.5\ MW$	$P_{dc,n} = -75\ MW$
Time Interval (sec)	$[0, 1)\&[5, 10]$	$[1, 3)$	$[3, 5)$
$I_{dc,tap_p}\ (kA)$	0	0.0844	0.176
$I_{dc,tap_n}\ (kA)$	0	0.0751	0.144
$I_{dc,out_p}\ (kA)$	0	0.934	1.875
$I_{dc,out_n}\ (kA)$	0	0.936	1.873
$I_{dc,R_p}\ (kA)$	3	3	3
$I_{dc,R_n}\ (kA)$	3	3	3
$I_{dc,I_p}\ (kA)$	3	2.916	2.823
$I_{dc,I_n}\ (kA)$	3	2.925	2.856

Table 3.4: DC Currents of Hybrid HVDC System when $P_{dc,p}$ varies from 0 MW to 75 MW and $P_{dc,n}$ varies from 0 MW to -75 MW.

The power flowing into the negative pole is 35.2 MW when the power at the output of the M2DC-CT (for the negative pole tapping station, $P_{dc,n}$) is set at 37.5 MW. When $P_{dc,n}$ is set to 75 MW, the power flowing into the negative pole HVDC link is 67.5 MW. Since the power is set for the output of the M2DC-CT, when supplying power to the negative pole of the HVDC link, the power losses cause the decrease in the tapping current magnitude (I_{dc,tap_n}) and hence the tapping currents are different at the the two tapping stations.

3.4.2 Firing Angles, Extinction Angles and Transformer Taps

Similar to the DC currents, the firing angles and extinction angles follow opposite trends. As described in the previous sections, when the α values are not within range, the number of transformer taps changes to bring the α values back into range. Figure 3.16 confirms this expected response.

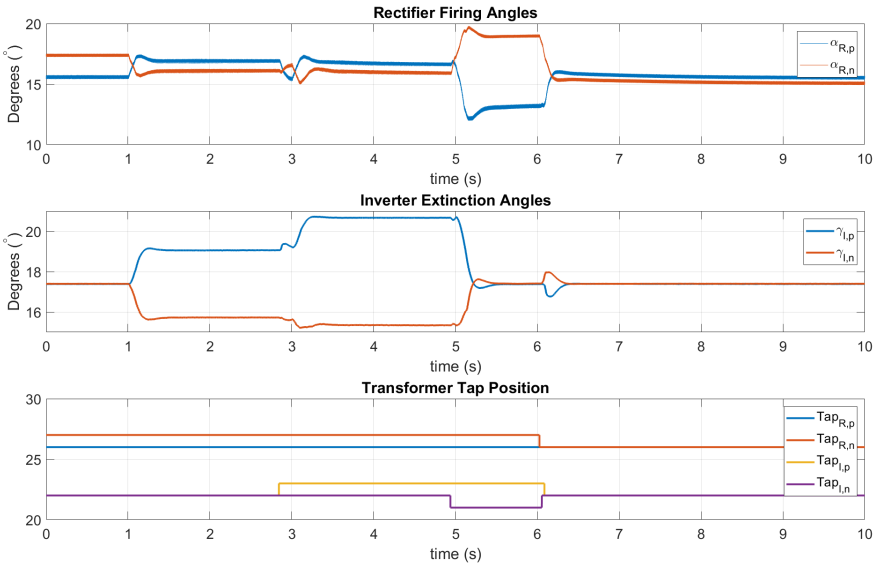


Figure 3.16: Firing Angles, Extinction Angles and Transformer Taps of the LCC Bipole HVDC System when $P_{dc,p} = -P_{dc,n}$

3.4.3 M2DC-CT Quantities

The variations of arm currents, arm voltages as well as the capacitor voltages are opposite in the positive pole tapping station as compared to the negative pole tapping station. Any increase in the magnitude or ripples in the quantities for the positive pole tapping station will cause a similar decrease in the same quantities for the negative pole power station provided P_{dc} is the same as demonstrated in Figures 3.17, 3.18 and 3.19.

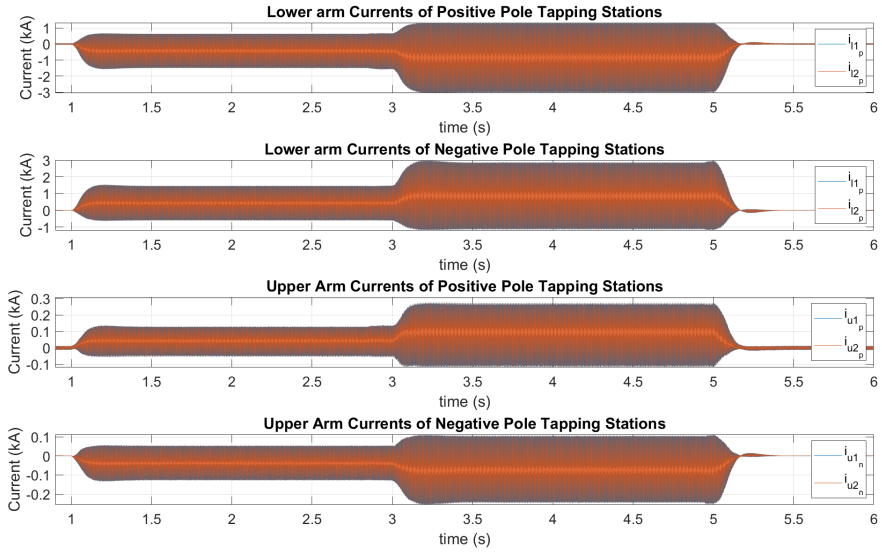


Figure 3.17: Arm Currents of Tapping Stations M2DC-CTs when $P_{dc,p} = -P_{dc,n}$

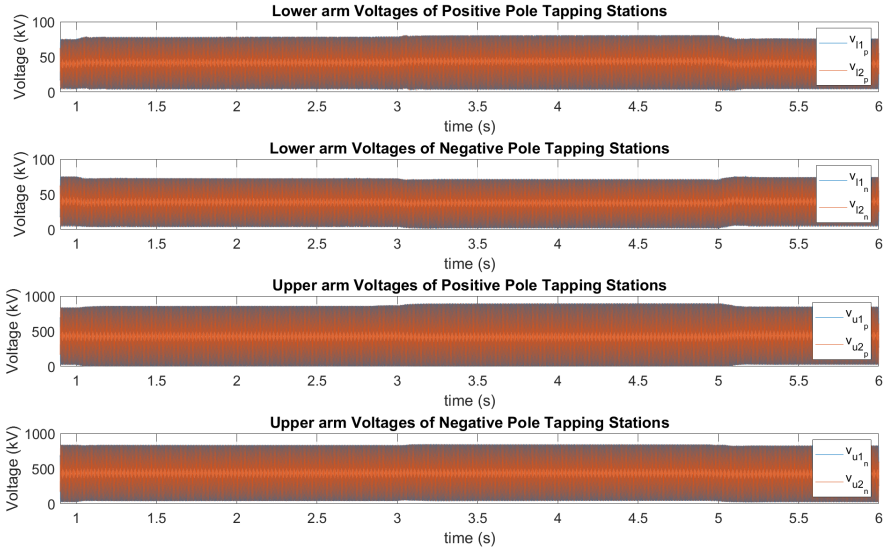


Figure 3.18: Arm Voltages of Tapping Stations M2DC-CTs when $P_{dc,p} = -P_{dc,n}$

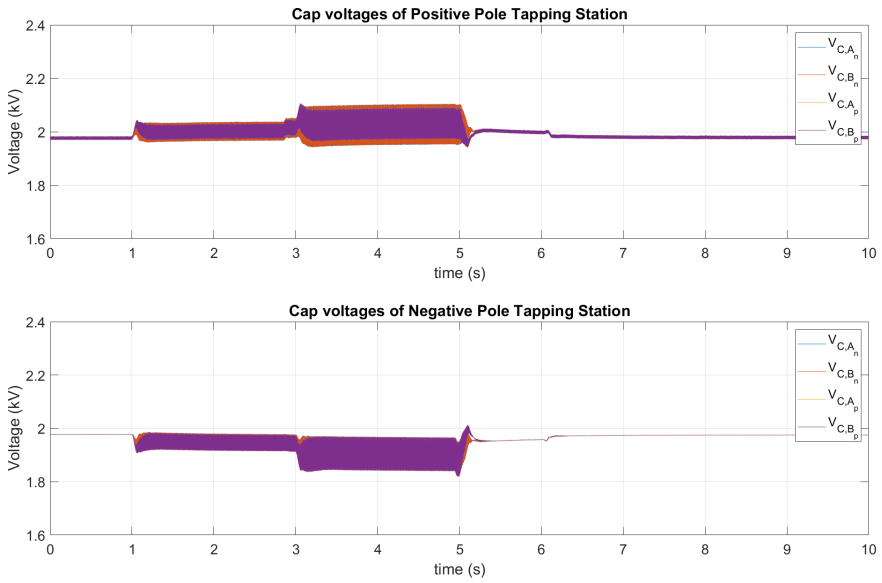


Figure 3.19: Capacitor Voltages of SMs in the Tapping Stations when $P_{dc,p} = -P_{dc,n}$

The peak-to-peak capacitor voltage ripples are the same in both cases as well as the rms capacitor voltage values even if the voltage magnitude is larger in the positive pole tapping station as compared to the negative pole tapping station.

3.5 Effects of Power Extraction Rates

The results of sections 3.2 to 3.4 all employed a power change ramp rate of 750 MW/s for the M2DC-CTs. In this section, the effects of varying the power extraction rates are studied. The responses of the tapping stations at either pole as well as the LCC-HVDC bipole system are the same when $P_{dc,p} = P_{dc,n}$. As a result, in this section, only the positive pole tapping station is used to study the responses of both the tapping station and the LCC-HVDC bipole system.

The four ramp rates studied in this work are 375 MW/s, 750 MW/s, 1500 MW/s, 3000 MW/s. The purpose of this study is to investigate how severe the transients in the DC currents can get at different power tapping rates since any kind of unwanted disturbances have to be avoided for both the

tapping stations and the LCC-HVDC system. $P_{dc,p}$ increases from 0 MW to 75 MW at the corresponding rates at $t = 0.25s$. The worst case scenario would usually be a step change in power demand. However, in real life applications, power increases happen at a rate of approximately $500 - 600$ MW/s [36]. At a rate of 3000 MW/s or higher, there were no major differences in the response of either the LCC-HVDC bipole system or the positive pole tapping station.

3.5.1 DC Currents of Hybrid LCC-VSC HVDC System

The rectifier and inverter DC currents of positive pole of the LCC-HVDC bipole system is shown in Figure 3.20. For the positive pole tapping station, the tapping DC currents and the output DC currents are shown in Figure 3.21.

The rectifier currents remain almost same across the entire simulation runtime. For the inverter DC current, the two slowest rates (375 MW/s,750 MW/s) provided the best transient response with minimal undershoot and a cleaner ramp decrease. As the power demand rate increases, slight undershoots occur and in the case of the transient for the 3000 MW/s case, the increase is not smooth as clearly seen in Figure 3.20. There are sharp changes that happen during the transient period, specifically at $t = 0.28s$ and $t = 0.35s$.

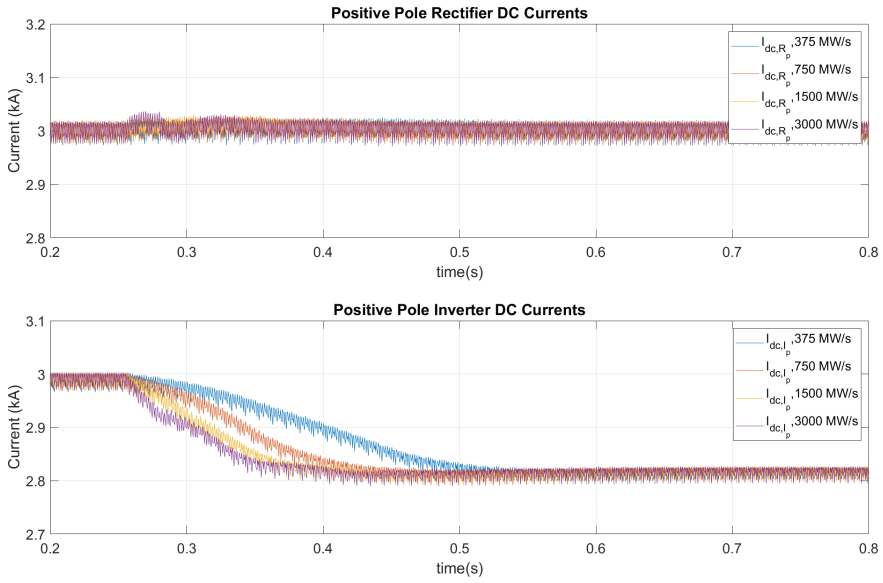


Figure 3.20: LCC-HVDC System Positive Pole DC Currents for different power ramp rates

Similarly, for the positive pole DC tapping currents and DC output currents, the two slowest rates provide the best responses. Anything higher than 1000 MW/s was giving bigger overshoots as demonstrated by the results obtained when the power demand rate was 1500 MW/s and 3000 MW/s. With the tapping DC currents being relatively small as compared to the output DC current, the controls had to be optimized to reduce any kind of ripples in the tapping DC currents. From Figure 3.21, there are larger transient ripples as the rate of power demand increase.

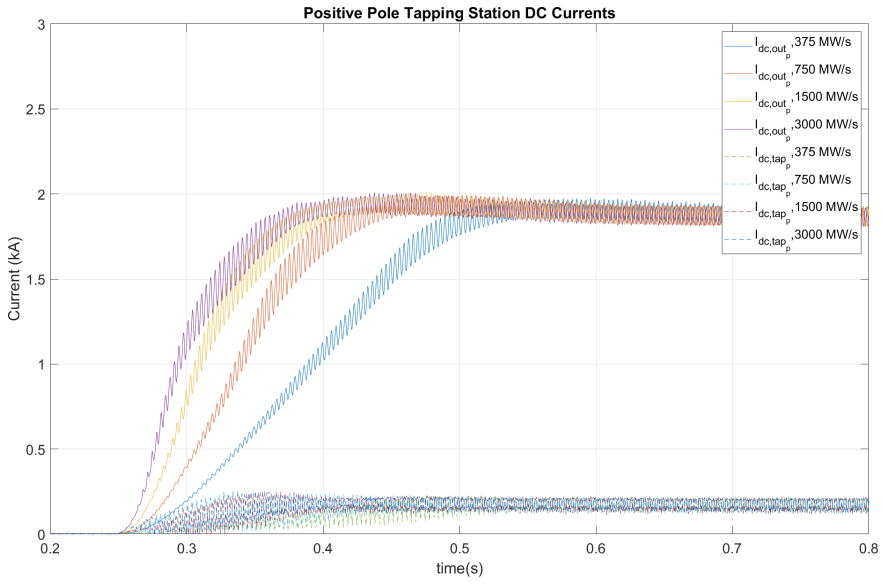


Figure 3.21: Positive Pole Tapping Station M2DC-CT Input and Output DC Currents for different power ramp rates

Figure 3.22 demonstrates the effect of the different ramp rates on the response of the M2DC-CTs SMs capacitor voltages at rated power demand. As compared to Figures 3.20 and 3.21, the effect of the different ramp rates is more emphasized in the capacitor voltages. Larger ramp rates result in higher percentage overshoot in the transients of the capacitor voltages. At 750 MW/s, the percentage overshoot is almost half that obtained when a 3000 MW/s ramp rate is used. However, the settling time is almost the same for all the ramp rates except for the 375 MW/s.

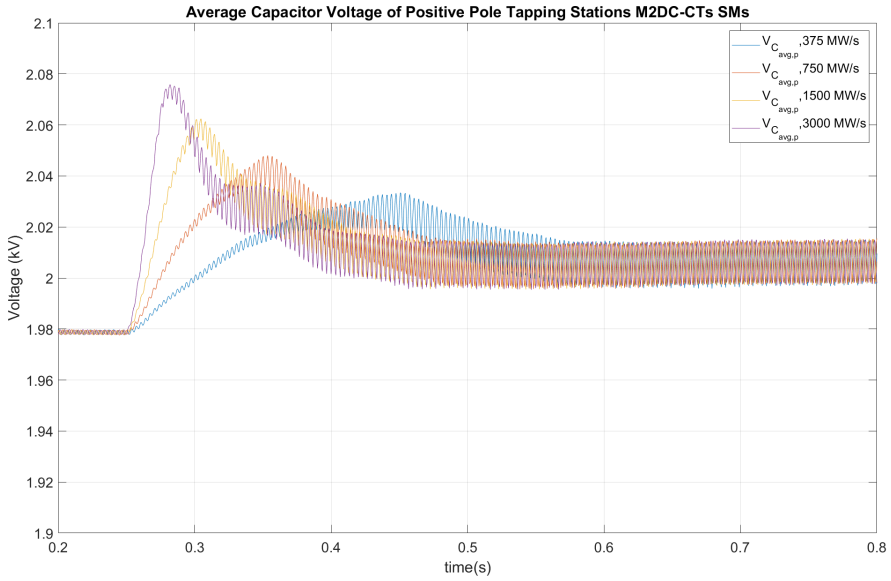


Figure 3.22: Average Capacitor Voltages of Positive Pole Tapping Station M2DC-CTs SMs for different power ramp rates

As for the arm currents, it was discussed in the previous sections that the lower arm currents are much bigger than the upper arm currents and thus the effects of variable ramp rates would be more prominent in those quantities. Figure 3.23 shows the response of the M2DC-CTs lower arm currents at the positive pole tapping station. There are no transient disturbances. The lower arm currents undergo a smooth rise to their rated values in all situations. The main difference is the amount of time it takes to reach the rated value. It takes the longest time when a power deman ramp rate of 375 MW/s is used (approximately 0.2s) while the response is fastest when a 3000 MW/s power demand ramp rate is used as expected (approximately 0.1).

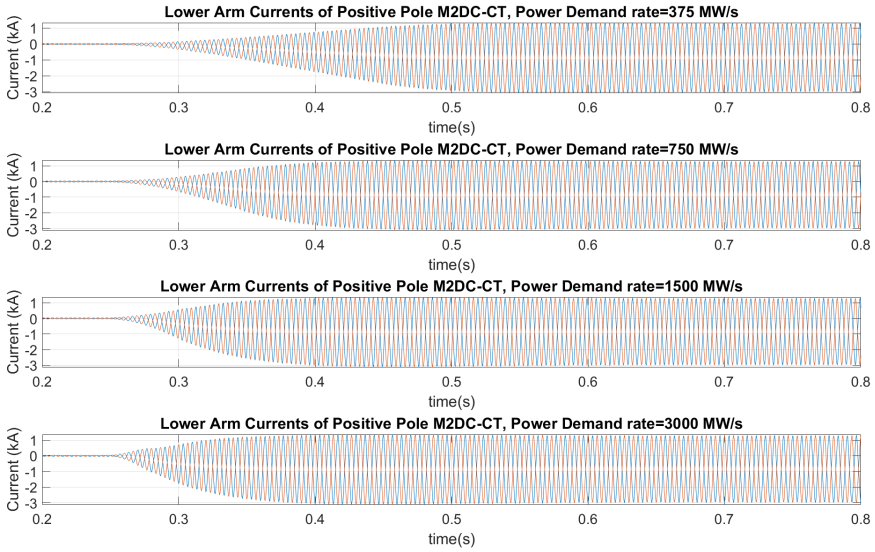


Figure 3.23: Lower Arm Currents of Positive Pole M2DC-CTs at different Power Demand Rates

From these results, the power demand rate of 750 MW/s was chosen for the following reasons:

1. It is the closest ramp rate to real life applications and is exactly 0.5 $p.u/s$.
2. Compared to the 1500 MW/s ramp rate, the difference in settling time is less than 0.03s whereas when compared to the 375 MW/s, it was 0.1s.
3. There are minimal disturbances in the transients as compared to the higher power demand rates without losing much in terms of rising time.
4. It provides the most acceptable overshoot possible without sacrificing settling time, as shown in Figure 3.22.

3.6 Summary

This chapter provided an in depth study of how different tapping scenarios affect both the LCC-HVDC bipole system as well as both tapping stations. Through symmetrical tapping where $P_{dc,p} = P_{dc,n}$ (0 MW, 37.5 MW, 75 MW), it was demonstrated that both tapping stations behaved the same

way with the same responses. The main differences happened in the LCC system more specifically, the number of taps at the transformers. Asymmetrcial tapping on the other hand showed that the two tapping stations would not adversely affect the LCC-HVDC bipole system or cause any kind of instability and operated independently of each other. Therefore, any power demand, within rated power limits, could be set at either tapping station. The M2DC-CT tapping station was also used to show the feasibility of integrating renewable resources or DERs to existing LCC-HVDC systems through the use of high voltage ratio DC-DC converters. As long as the LCC DC current changes occurred within specified thresholds, the control modes of the LCC-HVDC bipole system would not change. The power injection/extraction rates can vary based on the requirements of the hybrid HVDC system. Higher power demand rates can definitely be achieved and may be more desirable as they have shorter rising times and settling times. However, the transients might cause issues if a more robust and aggressive control system was to be used. Thus, these studies have shown that the LCC-HVDC bipole system can operate under all anticipated tapping conditions without any loss of overall system stability or reliability.

Chapter 4

Fault responses of Hybrid LCC-VSC HVDC System

In this chapter, the responses of both the LCC-based HVDC bipole system and the tapping stations are studied considering symmetrical AC faults (three lines-to-ground) and asymmetrical AC faults (single line-to-ground and double line-to-ground), as well as DC link faults (DC link line-to-ground fault) triggered on the LCC-HVDC system. As for the tapping stations, a line-to-ground fault is initiated on the MVDC bus at the output side of the M2DC-CT. The responses of both LCC-HVDC system and the tapping stations M2DC-CTs are studied and analyzed for all the types of faults. This chapter also includes the workings of the M2DC-CTs in response to fault detection and the measures taken to ensure a smooth restart once the fault is cleared.

4.1 LCC Bipole Fault Control Mechanisms

There are several control components involved in both the AC and DC fault recovery strategies but the main control components involved are the VDCOL and the RAML; those are discussed in section 2.3.1.

In the event of a rectfier side AC fault, the VDCOL, RAML and Power control mechanisms are the major factors that control to the fault recovery process. These are explained below.

1. When a low HVDC link voltage is detected, VDCOL reduces the rectified DC current, I_{dc0}. Once the HVDC link voltage is back to normal values,

the rectified DC current is slowly returned to its reference value. The recovery time depends on the voltage level thresholds that have been set in the VDCOL control mechanism and also the length of the fault itself.

2. The rectifier's α_{min} value is increased by the RAML control mechanism so that the inverter is now controlling current and by changing α_{min}, VDCOL response time is decreased. As a result of inverter controlling current, the power transferred across the HVDC-link is reduced but this ensures a smoother fault recovery. The RAML control mechanism also reduces the chance of commutation failure occurring during the recovery process.

3. The power control mechanism also ensures that I_{dc0} is not increased when inverter current control is active since in the event of the AC fault, this current will be smaller and the inverter current control will try to increase back to its reference value to keep power at 1.0 $p.u.$ To avoid such a scenario, locking mechanisms have been included in the control system upon detection of a fault.

Several factors affect the severity of the fault and the response time of the LCC-HVDC system as well as the recovery time once the fault has been cleared. These factors include:

1. The CFC ability to continuously create firing pulses as expected when there are disturbances in the AC network.

2. The gain values of the PI controllers in the rectifier/inverter CCAs: These directly affect how aggressively $I_{dc,R}$ follows I_{dc0} reference values.

3. The strength of the AC network: Weaker AC networks tend to have increased phase angles when there are changes in power. PLLs need to be able to track these power changes. Weak AC networks on the inverter side could also lead to voltage instability which in turn can cause commutation failures.

As for DC faults, the response of the LCC-HVDC bipole is as follows:

1. The detection process involves a voltage threshold which is set to monitor the changes in DC voltages at the connection point between the HVDC link and the tapping station at each pole. These voltage changes along with consistently lower HVDC link voltage whether at the rectifier side or inverter side trigger the DC fault response of the LCC-HVDC bipole system.

2. Upon detection, the pole DC current is rapidly reduced to zero.

3. After a set period of time (t_1), a 'restart' signal is ordered and the pole DC current is set back to its reference value.

4. If pole voltage is not the same as during normal operation, the DC fault detection mechanisms extinguishes the DC pole current again and another restart is ordered after another time interval (t_2, $t_2 > t_1$).

5. If the pole voltage does not recover, the time interval before sending another restart order is increased (t_3, $t_3 > t_2 > t_1$).

6. If unsuccessful, the pole voltage itself is reduced (in this case to 0.7 $p.u$) and another restart is attempted.

7. In the event, all of these approaches are unsuccessful, the pole will be blocked.

As it will be shown in the upcoming studies, the unfaulted pole is significantly affected when a DC fault happens at the other pole. The risk of commutation failure is increased and to mitigate it, γ_{ref} of the healthy pole's inverter is increased until the fault is cleared.

For the tapping stations, fault detection happens when the DC tapping voltages ($V_{dc,tap_p}A$ or V_{dc,tap_n}) drop below a certain voltage threshold (in this case 400 kV). Having this voltage threshold allows for a better performance of the bipole LCC-HVDC system in terms of fault recovery or situations where undervoltage is required. When either of DC tapping voltages, V_{dc,tap_p} or V_{dc,tap_n}, drop below the threshold, the SMs in all M2DC-CT arms will be in a

blocked state after a delay of 100 μs [24]. Both the DC tapping current and the DC output current at the corresponding tapping station will also be set to zero. When the voltage threshold is exceeded, indicating removal of the fault, and after a brief delay to allow for the full recovery of the LCC-HVDC system, power tapping will resume at the same level as pre-fault conditions.

4.2 DC Faults

This section demonstrates the responses of both tapping stations and the LCC-HVDC system in the event of a DC side fault, whether it is on the LCC system or the tapping station. The independent behaviour of the respective tapping stations are further reinforced while investigating DC faults on the MVDC bus side of the M2DC-CT at the positive pole. The fault duration was 200ms in all scenarios. All cases involve symmetrical tapping scenarios.

4.2.1 HVDC Link Fault - Line-to-Ground Fault on Positive Pole

The pre-fault, fault and recovery period along with the restart of the hybrid HVDC system were recorded when investigating the response of both tapping stations and the LCC-HVDC bipole system when the DC fault occurred. Three pre-fault power flow scenarios were considered:

1. $P_{dc,p} = P_{dc,n} = P_{dc} = 0\ MW$ at both tapping stations
2. $P_{dc,p} = P_{dc,n} = P_{dc} = 75\ MW$ at both tapping stations
3. No tapping stations were connected to the system

Scenarios 1 and 3 were used to investigate the effect on the fault response of the LCC-HVDC system before and after connecting the tapping stations on the respective poles. In scenarios 1 and 2, symmetrical tapping is used as the worse case scenario since both stations are tapping rated power at both poles simultaneously.

4.2.1.1 Fault Response of bipole LCC-VSC HVDC System

Figure 4.1 shows the variation of the rectifier and inverter DC currents of the LCC system at both poles for the dc line-to-ground faults. Waveforms for the three different pre-fault scenarios are overlaid. The DC fault is triggered by temporarily shorting the DC link on the rectifier side to ground for 200 ms. As discussed previously, upon detection of a DC fault on the positive pole, I_{dc,R_p} is quickly extinguished and consequently I_{dc,I_p} falls to zero as well. On the negative poles, both I_{dc,R_n} and I_{dc,I_n} initially drop but the CCA on the negative pole rectifier quickly brings I_{dc,R_n} back to its reference value.

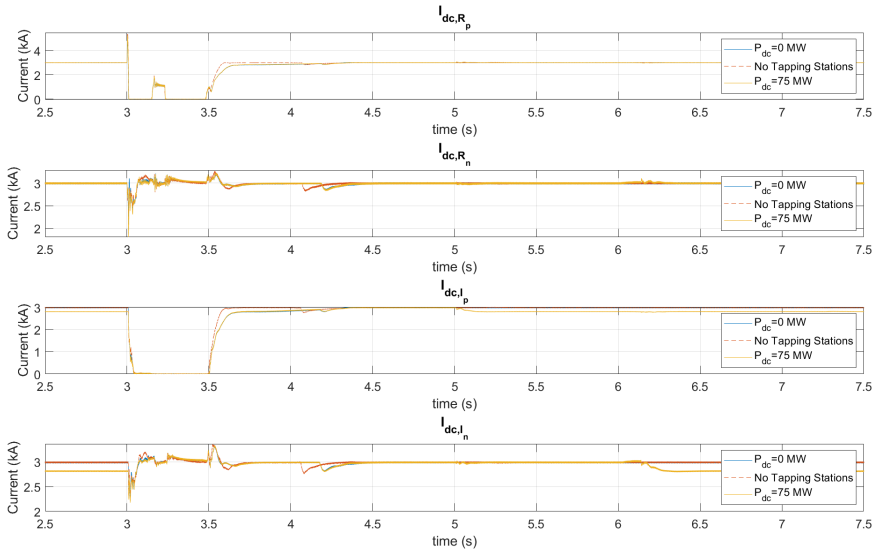


Figure 4.1: LCC-HVDC System DC Currents during a line-to-ground DC Link Fault for different pre-fault loading scenarios

Figures 4.2 and 4.3 show the variations of the DC voltages at both poles in the event of a DC fault at the positive pole HVDC link. With a DC line-to-ground fault on the positive pole HVDC link, it was expected for all the DC voltages on the positive pole HVDC link to be zero as shown in Figure 4.2. 150ms after the fault was detected, a restart was attempted as shown by the quick change in I_{dc,R_p} in Figure 4.1 at $t = 3.15s$. Since the fault was still active, the first restart attempt failed and the time interval before the second restart was set at 350ms. At $t = 3.5s$, the second restart was attempted and

since the fault was no longer active, the restart was successful. At both poles, the LCC-HVDC bipole system resumed normal operation at around $t = 4.25s$.

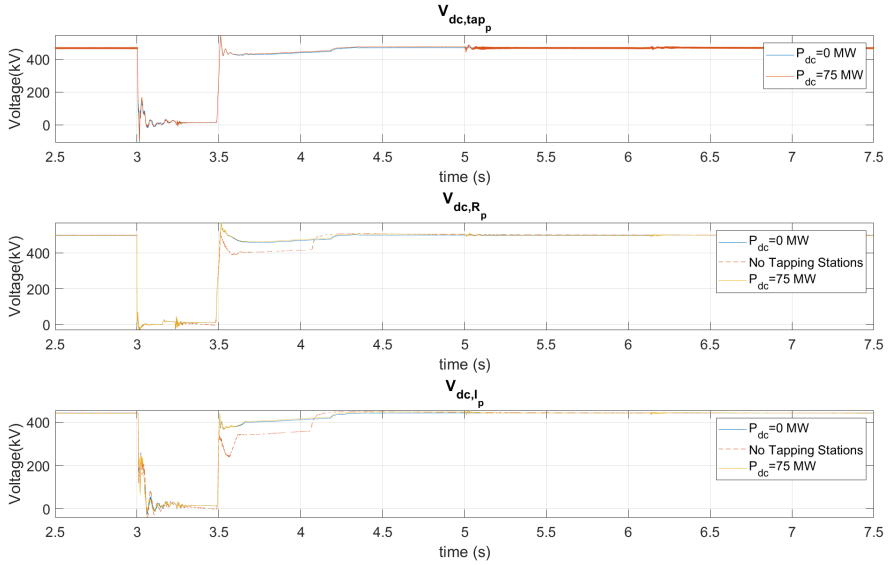


Figure 4.2: Positive Pole DC Voltages Variation during positive pole HVDC-link DC Fault for different pre-fault loading scenarios

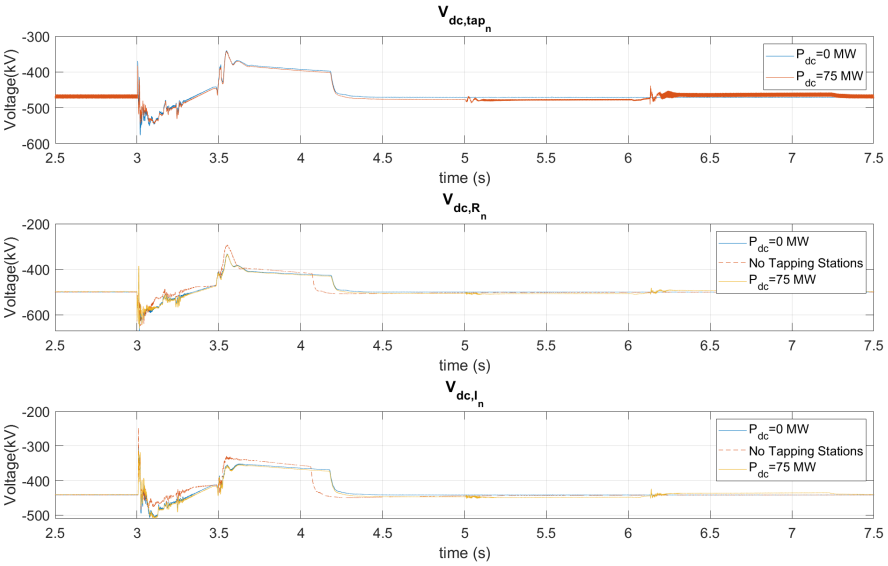


Figure 4.3: Negative Pole DC Voltages Variation during positive pole HVDC-link DC Fault for different pre-fault loading scenarios

Similar to AC faults, when a DC fault is detected α and γ at the rectifier

station on the healthy pole increases to mitigate any risk of commutation failure at the corresponding inverter station as shown in Figures 4.4 and 4.5 respectively. At the faulty pole, both α and γ values of the positive pole rectifier and inverter stations reach a maximum value of approximately 150°. During the attempted restart at $t = 3.15s$, $\alpha_{R,p}$ sharply decreases. However, since the fault has not been cleared, $\alpha_{R,p}$ is held saturated against its upper limit. At $t = 3.5s$, the fault is cleared and the restart is successful which in turn leads to a quick drop in both $\alpha_{R,p}$ and $\gamma_{I,p}$ to its calculated value. Tap changer controls then become active to ensure the firing and extinction angles of the positive pole rectifier and inverter stations are within their threshold values.

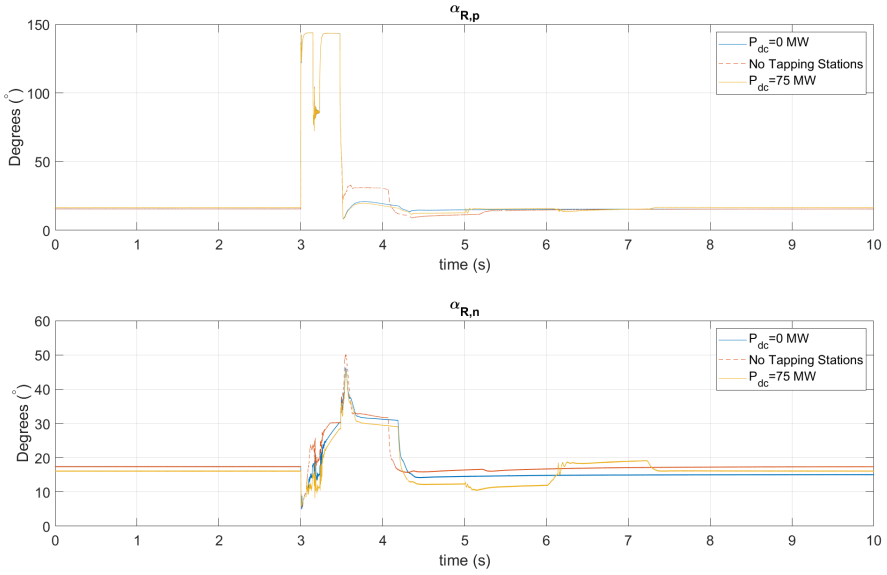


Figure 4.4: Rectifier Stations α variation in different pre-fault loading scenarios

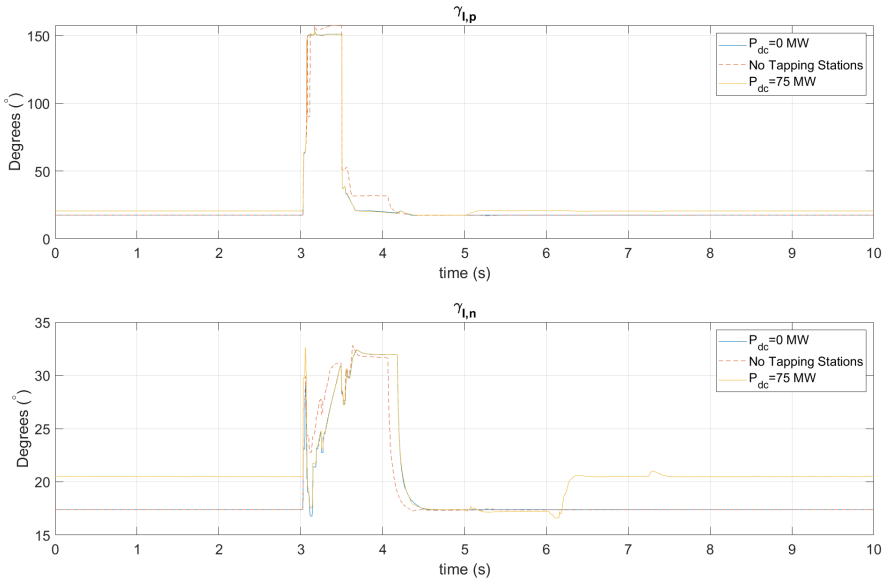


Figure 4.5: Inverter Stations γ variation in different pre-fault loading scenarios

From Figures 4.1 to 4.5, the effect caused by connecting the tapping stations to the HVDC bipole system can be clearly distinguished especially in the DC voltages and the firing and extinction angles of the rectifier and inverter stations at either pole. In all the figures, it was demonstrated that the presence of the tapping stations delay the recovery time of the fault, albeit minimally. In Figure 4.1, the rectifier side DC currents reached their normal operation value approximately $0.75s$ earlier when there are no tapping stations. However, during the transient period when the succesful restart has been ordered, the DC voltages at the faulty pole were at a lower value. For the healthy pole, the voltage levels were very similar except that the they recovered $0.15s$ faster as compared to when tapping stations have been connected.

In general, the presence of tapping stations did not negatively affect the response of the LCC-HVDC bipole system to a DC line-to-ground fault at the positive pole HVDC link. In both cases where tapping stations were present (considering pre-fault power flow scenarios, $P_{dc} = 0\ MW$ and $P_{dc} = 75\ MW$), the variation in quantities were very similar to the response obtained from just the LCC-HVDC system itself. Even at rated power, the differences were minimal and thus, as long as power demand is set within the rated power

limits of the tapping stations, the recovery period does not worsen.

4.2.1.2 Fault Response of DC Tapping Stations

Figure 4.6 shows the DC currents of both tapping stations during two different pre-fault power flow scenarios: $P_{dc,p} = P_{dc,n} = P_{dc} = 0\ MW$ and $P_{dc,p} = P_{dc,n} = P_{dc} = 75\ MW$. As demonstrated in Figure 4.6, both the input and output DC currents were quickly extinguished when the voltage fell below the set threshold (in this case 400 kV). The fault happened on the positive pole but since both pole DC voltages are below 400 kV (Figures 4.2 and 4.3), the negative pole tapping station treated it as a similar disturbance. A two second time interval was set between an attempted restart and the undervoltage detection. Everytime the DC pole voltage would drop below 400 kV, this interval is reset to minimize unwanted transients while guaranteeing a smoother recovery of the tapping stations.

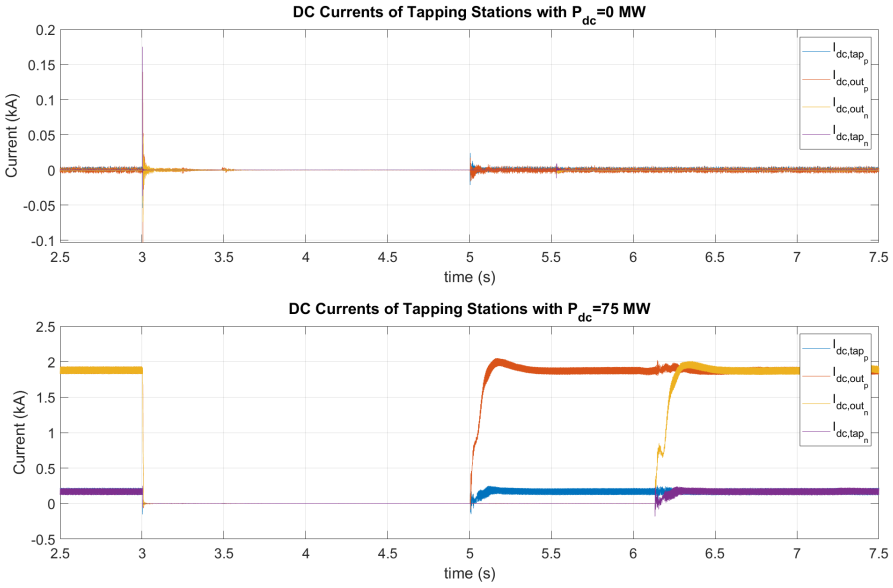


Figure 4.6: Tapping Stations DC Input and Output Currents during an HVDC DC link Fault

After the DC voltage was back to normal, the SMs were unblocked and power tapping was resumed to its pre-fault power demand at both tapping stations. Whether the fault happened during symmetrical or asymmetrical

tapping, the response of the M2DC-CTs would follow a similar procedure of undervoltage detection, SM blocking and unblocking and recovery.

During this whole period of fault detection and recovery, the SMs capacitor voltages have to be maintained to minimize any transient that could occur at startup. As demonstrated in Figure 4.7, upon detection of the lower than normal voltage, the SMs are blocked and the capacitor voltages were maintained within 4% of the nominal 2 kV capacitor voltage. For whichever P_{dc} value, as long as the detection and blocking procedures were properly carried out, the DC fault would not adversely affect the tapping stations except for a temporary 'shutdown'. Keeping the SM capacitor voltages as close as possible to its nominal value was essential. Large deviations would create undesired large transients and inrush currents when restarting the tapping stations (unblocking the SMs capacitors). When the unblocking signal was sent to the firing pulse controller, the M2DC-CTs would start tapping the same amount of power as before the fault occurred. At worst, the transients caused a maximum peak-to-peak voltage ripple of 7.1%.

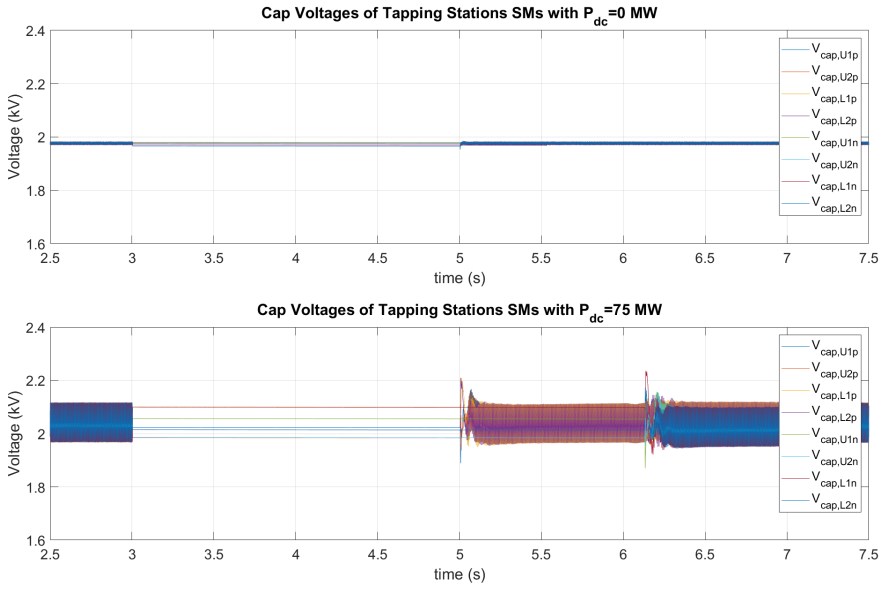


Figure 4.7: SMs capacitor voltage variations during an HVDC DC link Fault

4.2.2 Tap Station MVDC Side DC Fault

After investigating the effect and responses of both the LCC-HVDC bipole system as well as the tapping stations to an HVDC link DC line-to-ground fault, a similar fault was triggered on the MVDC bus side of the positive pole tapping station. The fault duration was again $200ms$ and the DC fault detection happens in a similar way as previously described. Once a sustained lower than normal voltage was detected (in this case, the voltage threshold was set at 30 kV on the MVDC bus side), the SMs capacitors were blocked until the fault was cleared and the MVDC bus nominal voltage was restored to 40 kV.

Two simulations were carried out with P_{dc} set at 0 MW and 75 MW in both tapping stations simultaneously (i.e symmetrical tapping). When $P_{dc} =$ 0 MW, the simulation investigates the event of a DC fault while the tapping stations are on standby mode. When $P_{dc} = 75$ MW, the responses of the individual tapping stations gave a better insight into how the M2DC-CTs and the existing LCC-HVDC system handle the DC faults.

4.2.2.1 Fault Response of Bipole LCC-VSC HVDC System

In all scenarios, the pre-fault stage consisted of the steady state stage when power tapping had already started. Figure 4.8 shows the pre-fault, fault, recovery and power tapping resumption stages for the LCC-HVDC Bipole DC currents. The initial quantities were the same as in Table 3.2. As demonstrated in Figure 4.8, when the fault was detected on the positive pole tapping station at $t = 3s$, the SMs capacitors were blocked after the short delay of 100 μs and the positive pole tapping station stops tapping power until the fault was cleared and a successful reset was enabled. The same recovery delay of $2s$ was applied. After $200ms$, the fault was cleared and the positive pole tapping station was ready for restart at $t = 5s$.

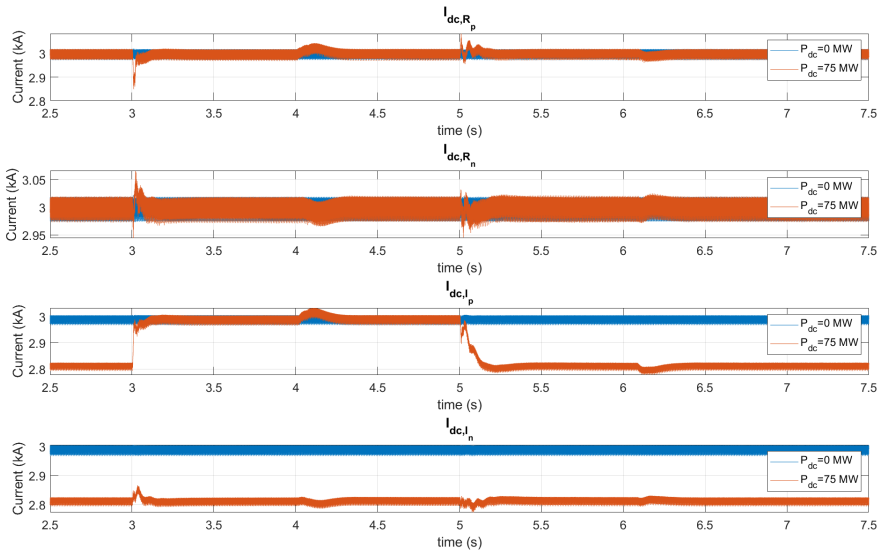


Figure 4.8: LCC-HVDC Bipole System DC Currents variations during an MVDC bus DC Fault at positive pole tapping station

As shown in Figures 4.9, 4.10, 4.11 and 4.12, the main transients happened at $t = 3s$, $t = 4.15s$, $t = 5s$ and $t = 6.15s$.

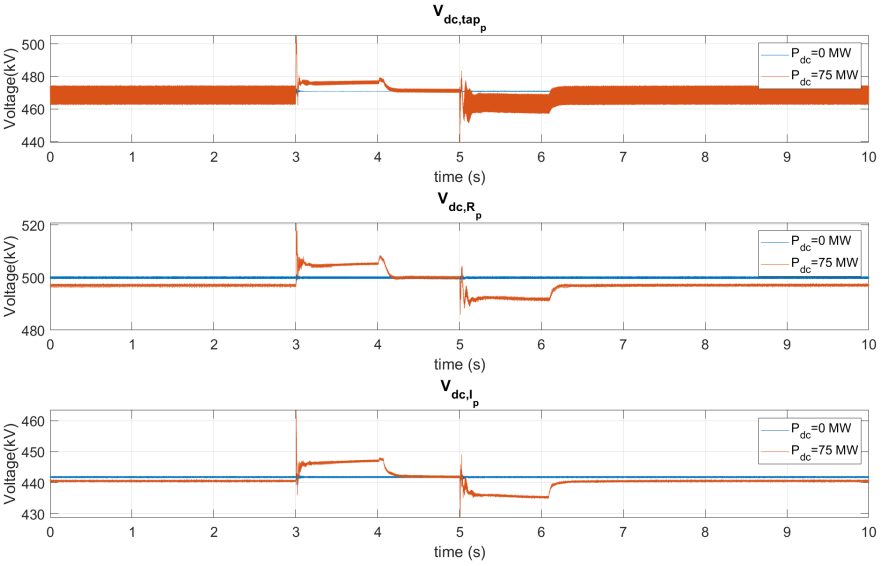


Figure 4.9: LCC-HVDC Positive Pole DC Voltages variations during an MVDC bus DC Fault at positive pole tapping station

At $t = 3s$, the fault was detected and the capacitor SMs blocked. The peak

DC voltage V_{dc,tap_p} reached during the transient was 505 kV which accounted for an increase of 7.68%. Similar increases were recorded for the rectifer and inverter DC voltages. At the positive pole, V_{dc,R_p} and V_{dc,I_p} increased by 4.4% and 5.0% respectively. The negative pole was less affected by the MVDC side DC fault. V_{dc,R_n} and V_{dc,I_n} underwent maximum amplitude changes of less than 2% in all cases and the transients in V_{dc,tap_n} was minimal as well.

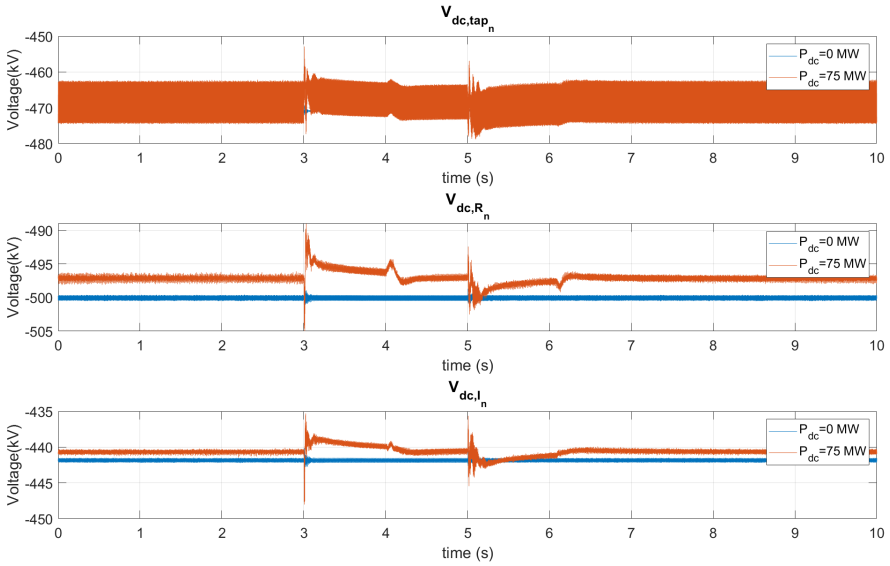


Figure 4.10: LCC-HVDC Negative Pole DC Voltages variations during an MVDC bus DC Fault

The changes in firing and extinction angles at the rectifier and inverter stations respectively at both poles were more prevalent as shown in Figures 4.11 and 4.12. However, these changes happened due to the power demand at the positive pole changing from 75 MW to 0 MW.

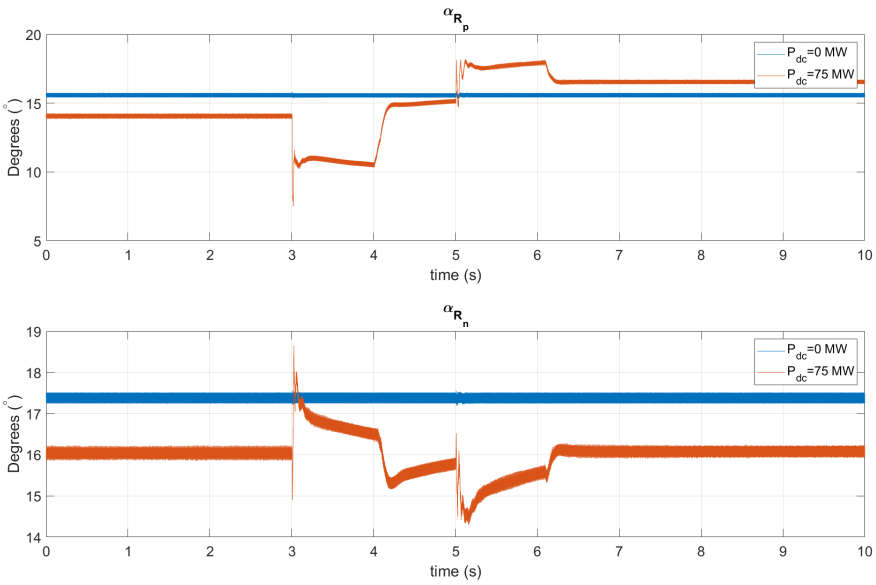


Figure 4.11: α_{R_p} and α_{R_n} variations during an MVDC bus DC Fault at positive pole tapping station

In the case when $P_{dc} = 0\ MW$ at both poles, when the fault happened, there are minimal effects on the LCC-HVDC bipole system. As a result, the changes in all the quantities of the LCC-HVDC bipole system could be directly attributed to changes in power demand rather than the MVDC side DC fault itself. Essentially, the LCC-HVDC bipole system saw the DC Fault as a step change in power demand at the faulty tapping station while the other station continued to operate normally.

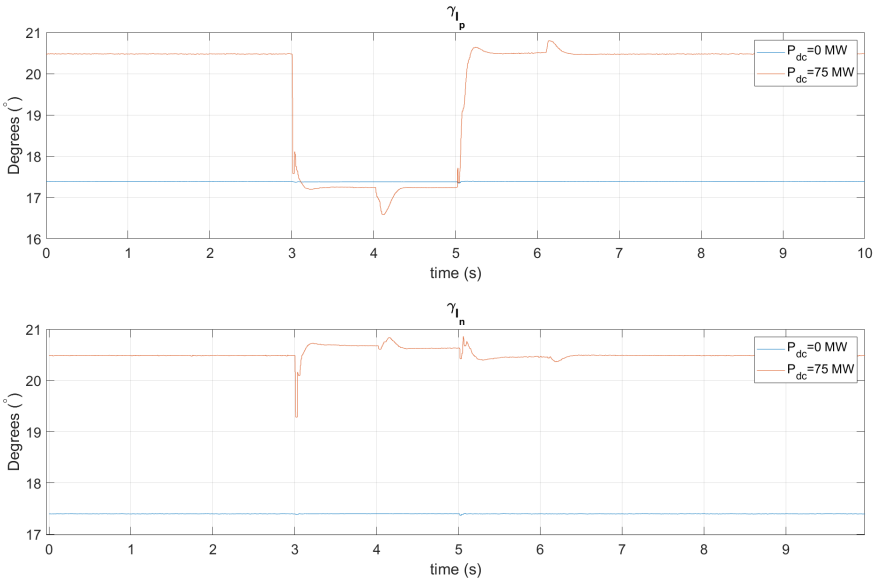


Figure 4.12: γ_{R_p} and γ_{R_n} variations during an MVDC bus DC Fault at positive pole tapping station

4.2.2.2 Fault Response of DC Tapping Stations

As for the tapping stations, it is demonstrated through Figures 4.13 and 4.14 that if a fault happened on the MVDC side of one tapping station, the other tapping station would operate normally with minor disturbances happening at the fault detection point and the restart point of the faulty tapping station.

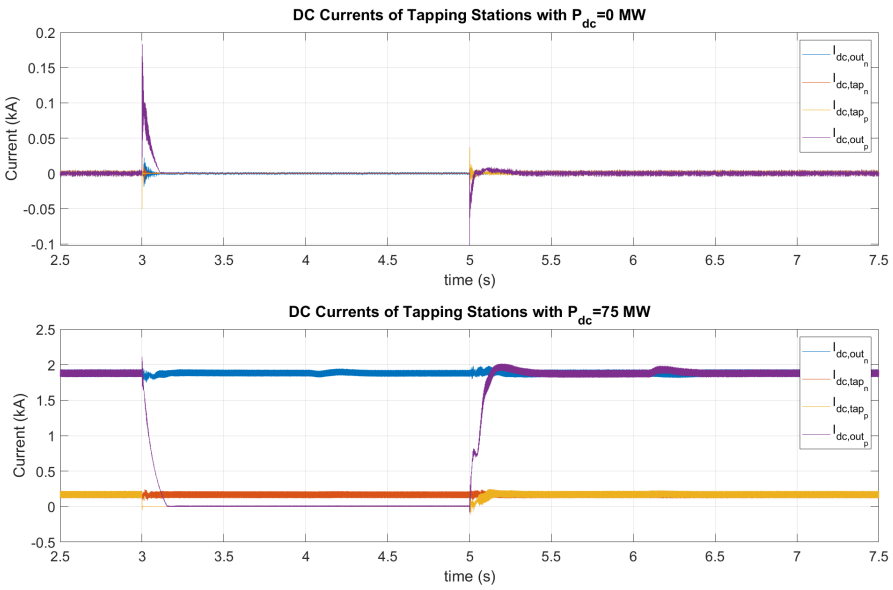


Figure 4.13: Tapping Stations DC Input and Output Currents during an MVDC bus DC Fault at positive pole tapping station

When $P_{dc} = 0\ MW$, both tapping stations behave the same way apart from the transient periods. In Figure 4.13, when the fault happened, the inrush current created by the fault was quickly extinguished. There were minor disturbances that occurred at the negative pole tapping station. A similar response was seen during the restart. However, in either case, the maximum current amplitude did not go beyond 200 A for the DC tapping currents and DC output currents at either tapping stations.

Similarly, when $P_{dc,p} = P_{dc,n} = 75\ MW$, when a fault was detected at the MVDC bus of the positive pole tapping station, I_{dc,tap_p} as well as I_{dc,out_p} was quickly extinguished while I_{dc,tap_n} and I_{dc,out_n} stayed at their required values with minimal transient disturbances at the fault instant and at the restart.

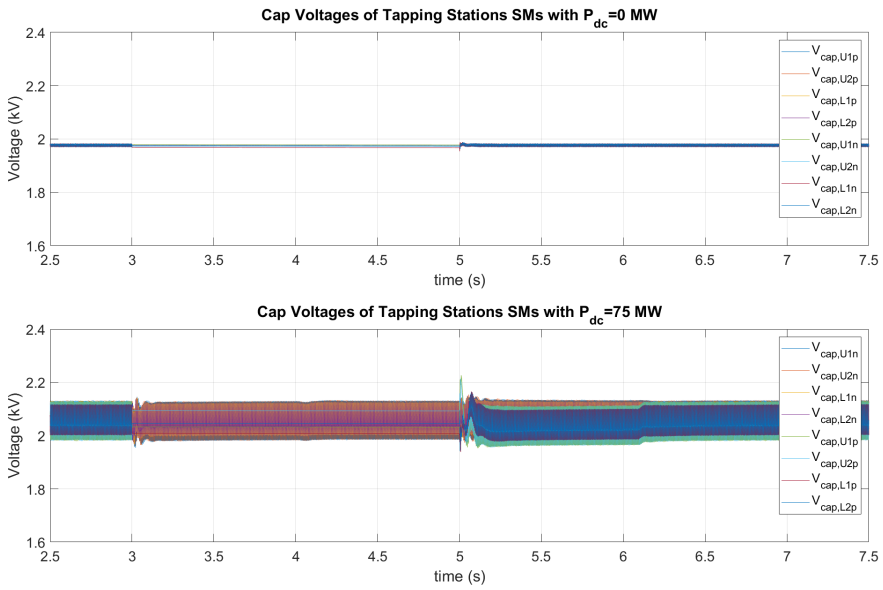


Figure 4.14: SMs capacitor voltage variations during an MVDC bus DC Fault at positive pole tapping station

AS for the capacitor voltages, the nominal voltage was maintained throughout the whole fault and recovery stage as shown in Figure 4.14. Apart from the peak-to-peak voltage ripple changes, the transients were all kept within $\pm 10\%$ of the nominal capacitor voltage.

4.3 Bipole LCC-HVDC System AC Faults

In this section, both symmetrical and asymmetrical AC bus faults were investigated. The rectifier side faults and inverter side faults were both tested with similar results and therefore, the focus is on the rectfier side AC faults. The fault responses for both the LCC system and the tapping stations are examined in different pre-fault loading scenarios.

The capacitor voltages had the same variation as during DC faults since the SMs capacitors were blocked once the HVDC DC-link voltage was below the threshold. As a result, the pre-fault loading scenario discussed in the following sections has $P_{dc,p} = P_{dc,n} = 0\ MW$ to investigate the worst case fault scenario. Afterwards, $P_{dc,p} = P_{dc,n} = 75\ MW$ and the response of the LCC system and the tapping stations to AC fault with the worst transients during a no power demand pre-fault loading scenario is studied.

4.3.1 Symmetrical Fault

For the symmetrical fault, a three phase line-to-ground AC fault was triggered for 200 ms duration at the rectifier station commutation bus. Figure 4.15 shows the three rectifier AC voltage phases dropping instantly to zero when the fault is triggered at $t = 3\ sec$.

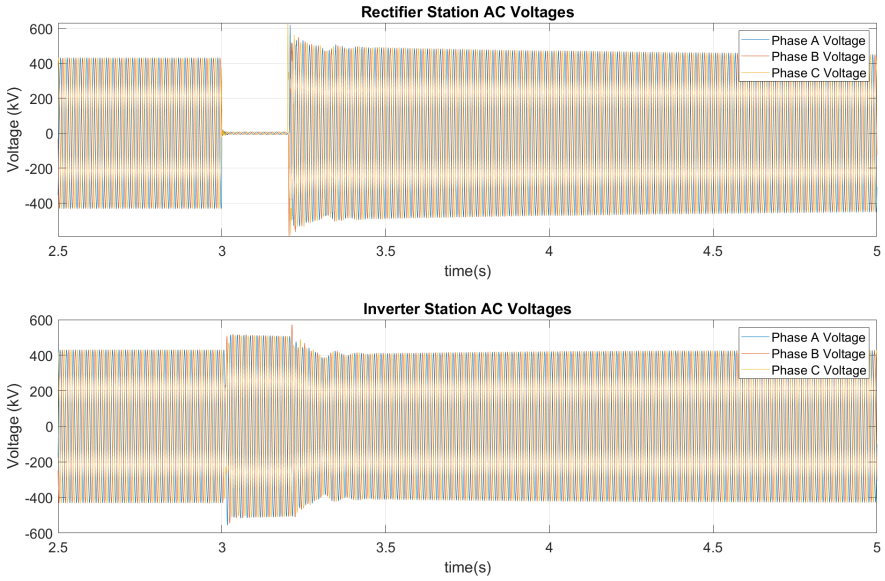


Figure 4.15: Rectifier and Inverter Staions AC network voltages during a Symmetrical AC Fault at the Rectifier

In Figure 4.15, when the rectifier side AC voltage dropped to zero, the inverter side AC voltage increased to maintain the operation in the HVDC link poles at reduced DC voltage. The reduced voltage operation is shown in Figure 4.16. Here, the voltage initially dropped to zero when the AC fault was detected and the DC voltage at both poles quickly ramped up to around 100 kV. Oncethe fault is removed (at $t = 3.2s$), the restart was attempted by the control system of the LCC-HVDC bipole system.

With a successful restart, both the rectifier side AC voltages and the HVDC link poles DC voltages both increased back to their nominal values. During the transient period, the rectifier station AC voltages had a peak amplitude of 630 kV for phases A and C and 550 kV for phase B. At the same time, the corresponding phase voltages at the inverter station dropped by an approximately equal amount from its increased values during the fault period.

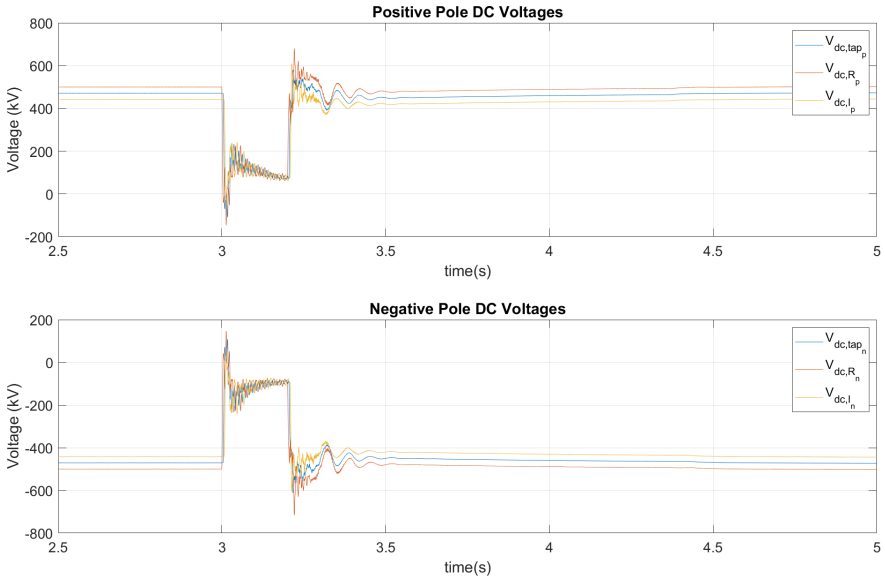


Figure 4.16: HVDC DC Link Pole Voltages during a Symmetrical AC Fault imposed at rectifier commutation bus

Figures 4.15 and 4.16 demonstrate that within $1s$ of the fault being cleared, both the AC voltages at either station and the DC pole voltage at either pole were within 2% of their nominal value. The DC currents followed the variations of the HVDC link voltages. The rectifier side DC currents had more disturbances during the period when the current was being extinguished and when the restart was ordered. On the other hand, the inverter side DC currents were much "cleaner", with a smoother decrease to zero and a smoother increase to its nominal value. Figure 4.17 demonstrates these responses.

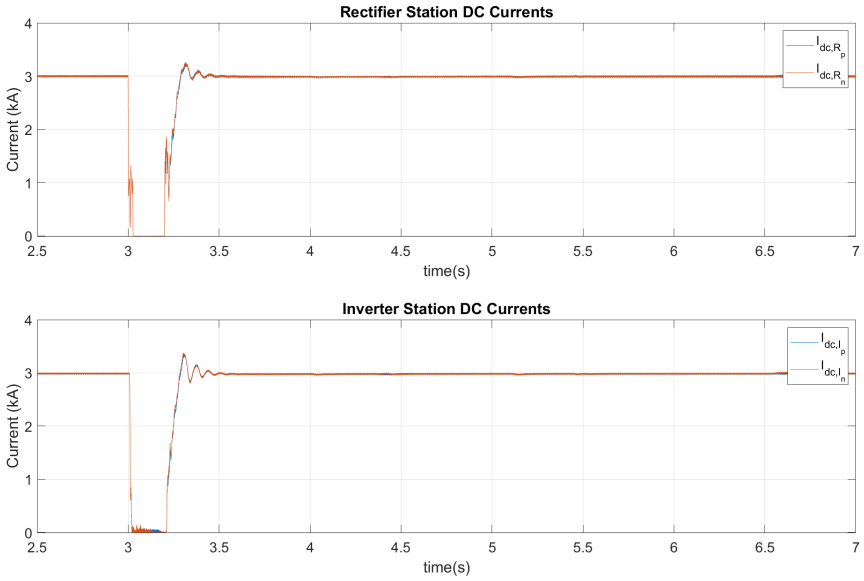


Figure 4.17: LCC-HVDC Bipole System DC Currents variations during a Symmetrical AC Fault

The firing angles took the longest to return back to normal after the fault was cleared as compared to the extinction angles as shown in Figure 4.18. At the instant the fault happened, both firing angles ($\alpha_{R,p}$ and $\alpha_{R,n}$) as well as both extinction angles ($\gamma_{I,p}$ and $\gamma_{I,n}$) increased to 30° due to RAML action and 70° respectively. However, throughout the duration of the fault, $\alpha_{R,p}$ and $\alpha_{R,n}$ stayed constant this value while $\gamma_{I,p}$ and $\gamma_{I,n}$ both increased consequently as the inverter CCA was responsible for the current control. Both VDCOL and RAML contributed in avoiding commutation failures during the fault or at restart when the LCC-HVDC system was trying to go back to its pre-fault stage.

Upon clearing the AC fault, the rectifier stations CCAs started controlling the current and VDCOL as well as RAML caused $\gamma_{I,p}$ and $\gamma_{I,n}$ to promptly return to their pre-fault (their nominal value in this case). Dropping the extinction angles back to normal was less than $1s$. However, as for the firing angles at both rectifier stations, bringing them back to their pre-fault values was a longer process. However, the recovery length could be altered by changing the parameters of the PI controllers in the rectifier stations' CCA.

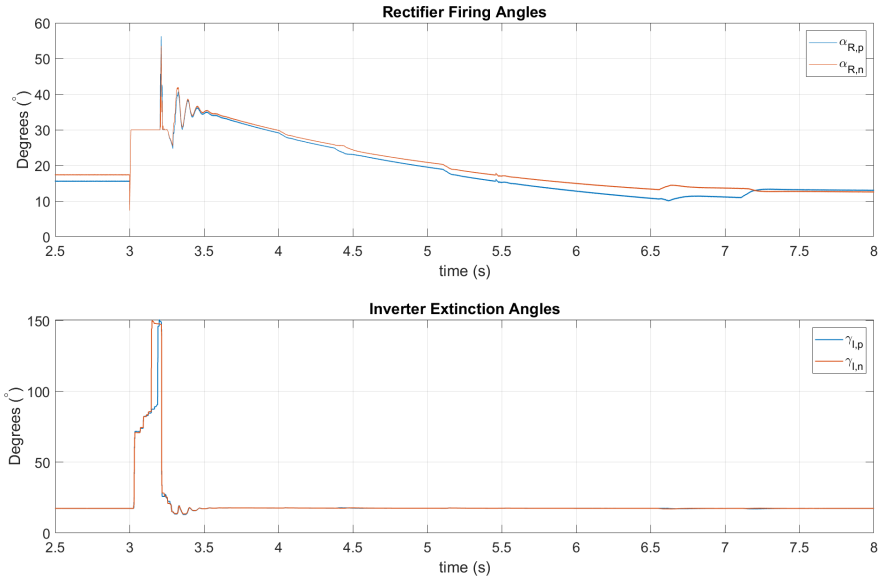


Figure 4.18: Firing and Extinction Angles Variation during a Symmetrical AC Fault

As for the tapping stations, their responses was similar to when the DC fault happened on the positive pole HVDC link. Since the tapping voltages, V_{dc,tap_p} and V_{dc,tap_n} dropped below their threshold value of 400 kV, the SMs capacitors were blocked for both stations and no DC currents were flowing except during the transient periods as shown in Figure 4.19. The main disturbances happened in the tapping DC currents, I_{dc,tap_p} and I_{dc,tap_n}, while the output DC currents, I_{dc,out_p} and I_{dc,out_n} remained mostly zero. However, if either $P_{dc,p}$ or $P_{dc,n}$ were non-zero, bigger transients would have been seen but still, the system would stable and ready for a restart once faults were cleared as demonstrated in the DC fault section. Compared to the DC fault when $P_{dc,p}$ and $P_{dc,n}$ were both 0 MW, the peak amplitude of the DC currents for the tapping stations were lower as was the case for every power demand value within the rated power limits.

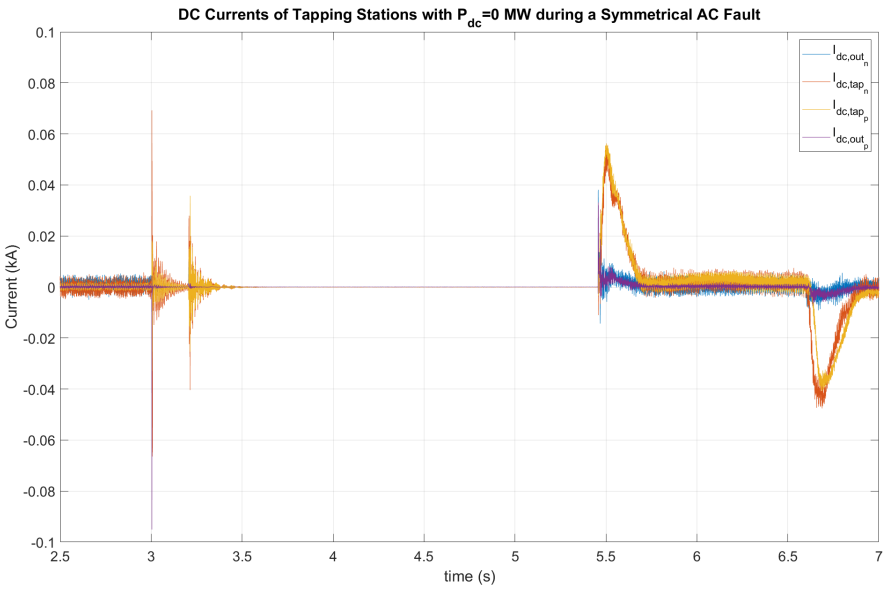


Figure 4.19: Tapping Stations Input and Output DC Currents during a Symmetrical Fault with $P_{dc,p} = P_{dc,n} = 0\ MW$

The arm voltages for both tapping stations followed the same variations of the corresponding HVDC link DC voltage. Since the SMs were blocked throughout the fault, there were no AC components in all the arm voltages as shown in Figure 4.20.

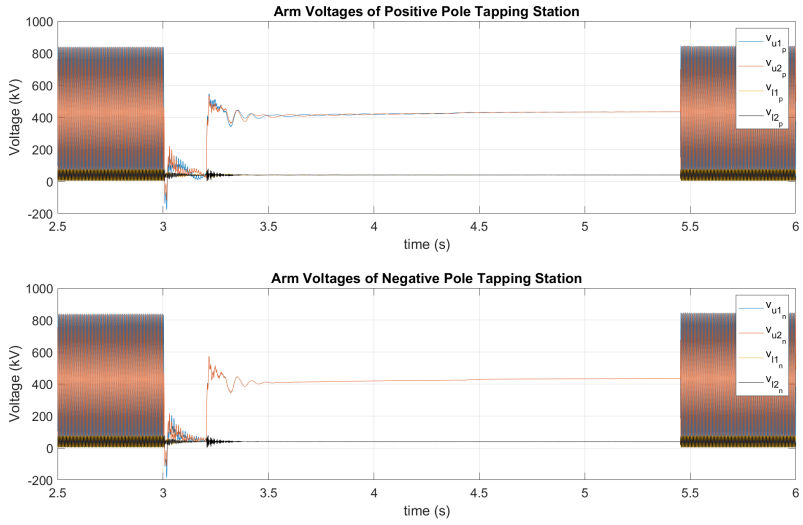


Figure 4.20: Tapping Stations Arm voltages with $P_{dc,p} = P_{dc,n} = 0\ MW$ during a Symmetrical AC Fault

4.3.2 Asymmetrical Fault

In the second AC fault case, a single line-to-ground fault was triggered on the rectifier side AC phases (Phase A was faulty). Figure 4.21 demonstrates how the AC voltages of the LCC-HVDC bipole system vary when one phase of the rectifier side AC voltage drops to zero.

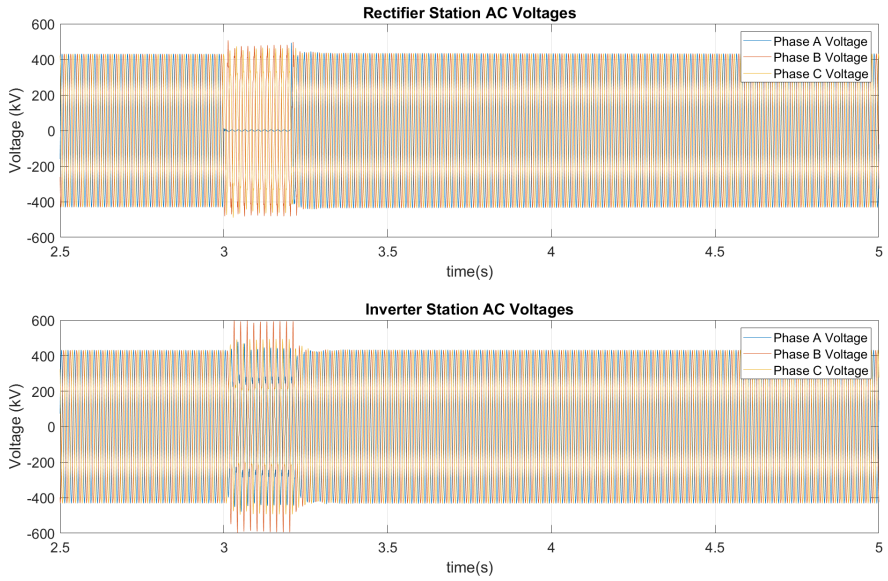


Figure 4.21: AC Network Voltages of LCC-HVDC System under a Single line-to-ground Fault at the Rectifier Station

For the rectifier side: The amplitude of both phases B and C increased to 507 kV. Throughout the fault, these voltage levels were maintained. Phase A had a peak-to-peak voltage ripple of 14 kV and could be considered as negligible based on the nominal AC voltage amplitudes (less than 2%).

For the inverter side: The amplitude of both phases B and C increased to 596 kV while for phase A, it stayed at its nominal value.

Due to these imbalances, as compared to the symmetrical three-phase line-to-ground fault, the DC link voltages at both poles (whether at the rectifier station or inverter station), varied in an oscillatory manner. All six DC voltage quantities, including the DC tapping voltages, had a large ripple component as shown in Figure 4.22.

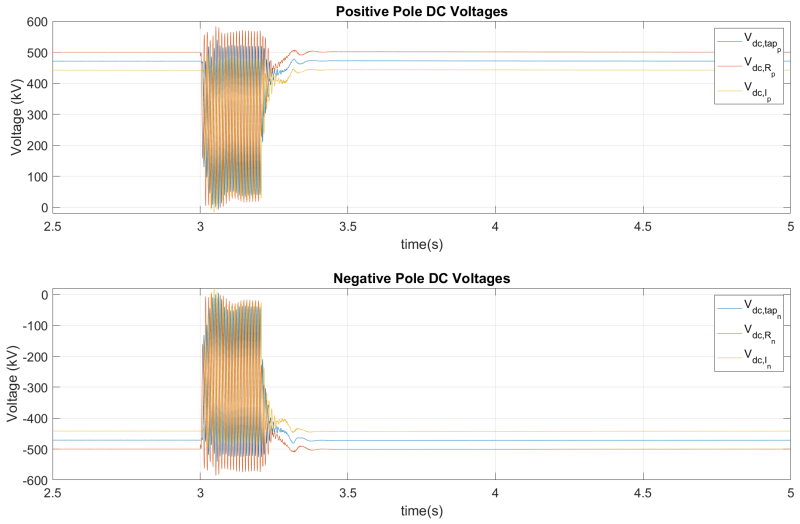


Figure 4.22: Pole DC Voltage Variations during a single line-to-ground AC Fault

Since the LCC-HVDC system DC currents follow the same profile as the DC voltages at the corresponding station, they had a big AC component as well. In this case, the highest peak-to-peak DC current variation measured during the fault period was approximately 2.5 kA (for both I_{dc,R_p} and I_{dc,R_n}). These ripples were smaller for both inverter DC currents, I_{dc,I_p} and I_{dc,I_n}, shown in Figure 4.23.

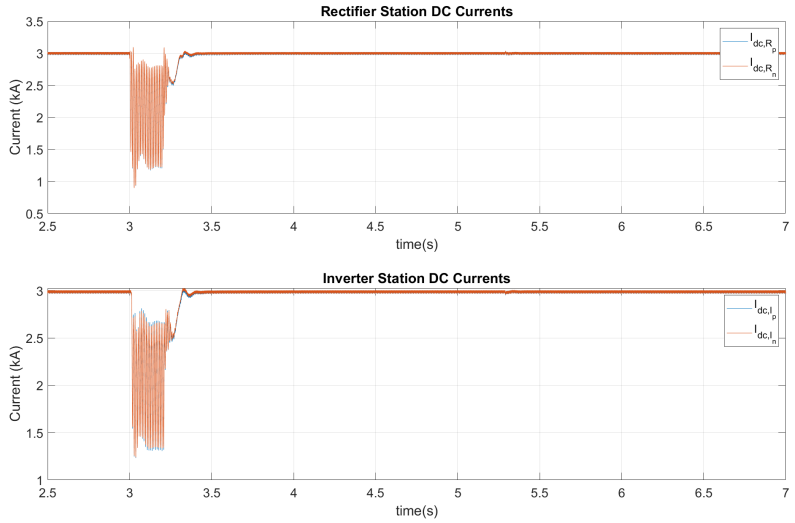


Figure 4.23: LCC-HVDC DC Currents under an Asymemtrical AC Fault

The severity of an AC fault can be measured by how much the firing angles deviate from their nominal values during the fault and recovery period. In the symmetrical AC fault case, the maximum $\alpha_{R,p}$ and $\alpha_{R,n}$ values were roughly 55° but when there was a single line-to-ground AC fault, the maximum values were around 42° as demonstrated in Figure 4.24. The extinction angles, $\gamma_{I,p}$ and $\gamma_{I,n}$ were both much smaller (peak value of approximately 44°) than in the previous AC fault scenario (peak value of approximately 150°). The other main difference was the recovery period. Here, the firing angles returned to their pre-fault values once the fault was cleared and the system had recovered.

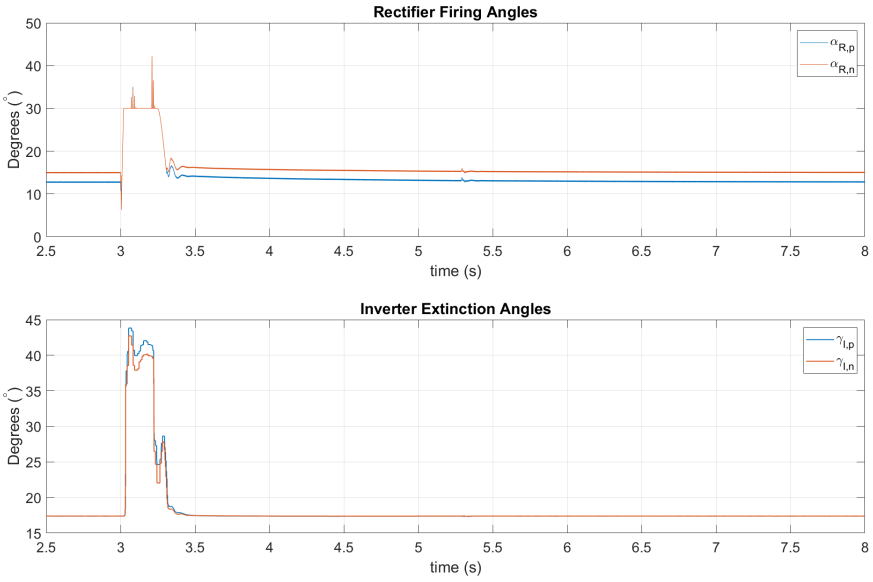


Figure 4.24: Rectifier Firing Angles and Inverter Extinction Angles during an Asymmetrical AC Fault

The response for a multiple lines-to-ground asymmetrical AC fault would be in between these two types of responses, with the symmetrical AC fault being the worst case scenario in terms of firing and extinction angles. The recovery period for these quantities were also the longest during the symmetrical AC fault and shortest during a single line-to-ground fault, irrespective of which line it was.

As for the tapping stations, during a single line-to-ground AC fault, the DC tapping currents, I_{dc,tap_p} and I_{dc,tap_n}, had large AC components with no

DC component. During the fault, these typically DC currents had AC currents with peak amplitudes of the order of hundreds of amperes (peaking at around 1.05 kA) as shown in Figure 4.25. However, once the fault was cleared, these DC currents dropped to zero almost instantly with minimal AC components. As the SMs capacitors were still blocked, there were no DC currents flowing in the M2DC-CTs at either tapping station and therefore, there was no power output even if both $P_{dc,p}$ and $P_{dc,n}$ were non-zero quantities.

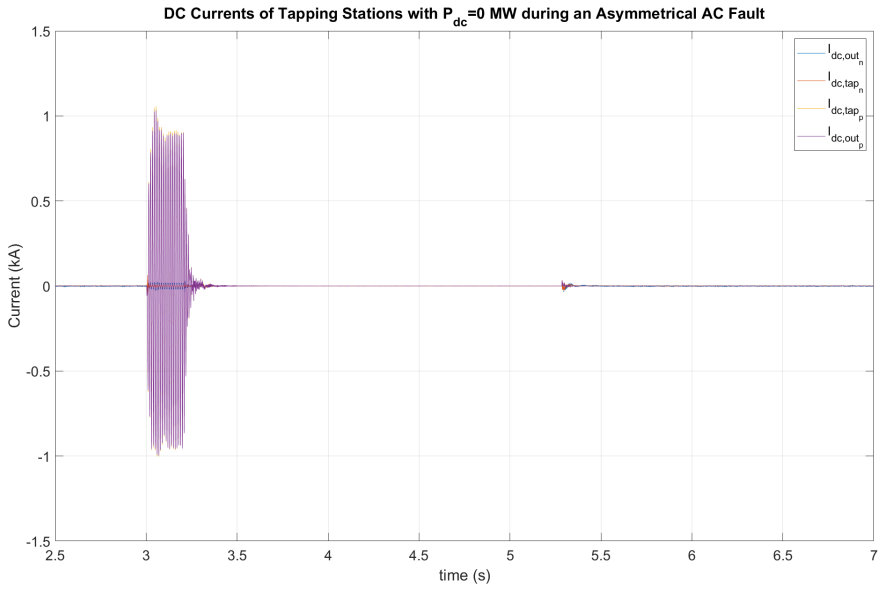


Figure 4.25: Tapping Stations DC Currents Variations

The arm voltages had more transients throughout the fault duration than in the previous scenario as shown in Figure 4.26. As it was the case with the DC tapping currents, once the fault was cleared while the SMs capacitors were still blocked, the arm voltages had minimal AC components. The arm currents were kept at zero throughout the fault duration and the recovery period until the SMs capacitors were deblocked. Thus, AC faults directly affected the tapping stations' arm voltages and tapping voltages but with no current flowing, the tapping stations were virtually not there.

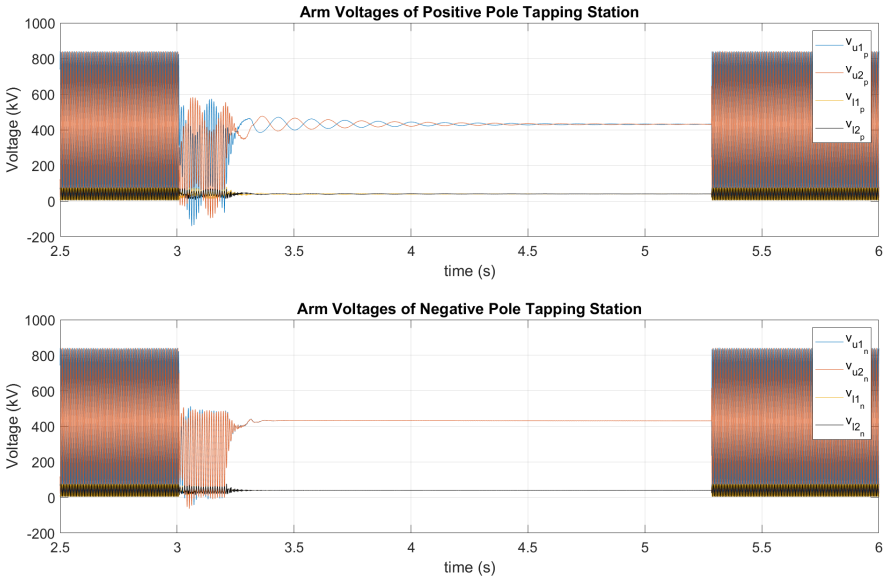


Figure 4.26: Tapping Stations Arm Voltages when $P_{dc,p} = P_{dc,n} = 0\ MW$ during an Asymmetrical AC Fault

4.3.3 Effect of Rated Power Tapping on the Fault Response of the Hybrid VSC-LCC HVDC Bipole System

With the symmetrical AC fault being the worst type of fault in terms of recovery period of the firing angles and extinction angles of the rectifier and inverter stations respectively, having tapping stations operating at rated power might complicate or delay the successful restart of both the LCC-HVDC system and the tapping stations.

In this section, a symmetrical three phase line-to-ground fault was initiated for a duration of 200 ms while both tapping stations were tapping rated power ($P_{dc,p} = P_{dc,n} = 75\ MW$).

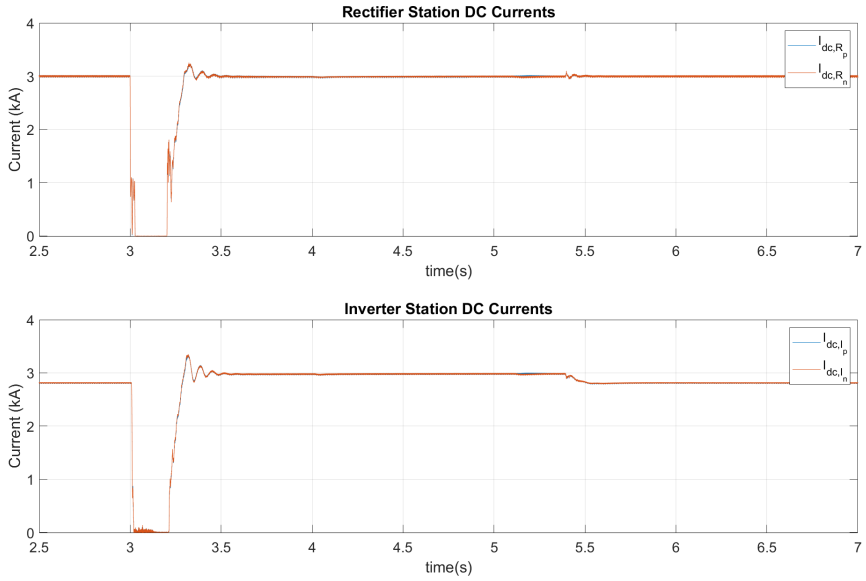


Figure 4.27: LCC-HVDC System DC Currents during a Symmetrical AC Fault when $P_{dc,p} = P_{dc,n} = 75\ MW$

Compared to Figure 4.17, the rectifier and inverter side DC currents were the same except for the reduced inverter current due to the power tapping occuring before the fault occurred and after the fault occurred as demonstrated in Figure 4.27.

Similarly, the tapping stations' DC currents, both on the input side (I_{dc,tap_p} and I_{dc,tap_n}) and the output side (I_{dc,out_p} and I_{dc,out_n}), remained the same at rated power during the fault and until the LCC-HVDC system had recovered. There were still some transients that occurred when the tapping stations SMs capacitors were deblocked and power tapping resumed simultaneously as shown in Figure 4.28. Adding another delay after the deblocking stage would reduce these transients and cause a smoother restart for power tapping.

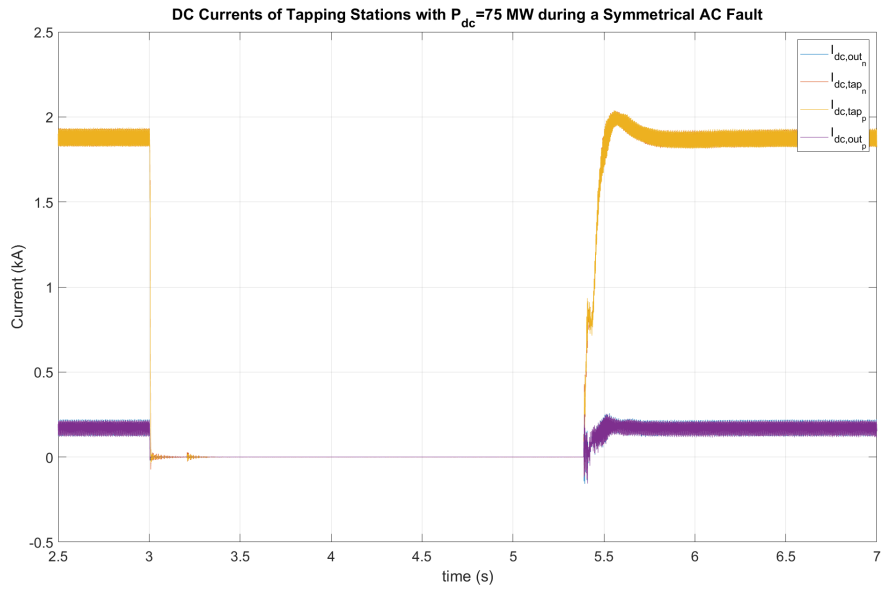


Figure 4.28: Tapping Stations DC Currents during a Symmetrical AC Fault when $P_{dc,p} = P_{dc,n} = 75\ MW$

Figure 4.29 demonstrates the response of the arm currents of the positive pole tapping station when a symmetrical three-phase AC fault at the rectifier station during rated power demand operation. The arm currents follow the same trend as the DC currents of the tapping station. When the SMs capacitors are in a blocked state, there is no current flowing and once the fault is cleared, the SMs capacitors are deblocked and normal tapping operation is resumed.

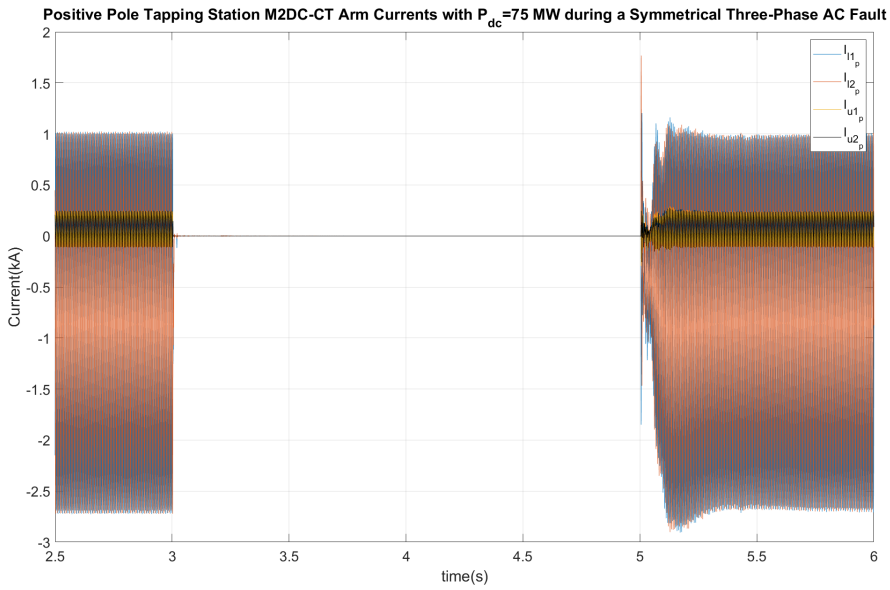


Figure 4.29: Positive Pole Tapping Station M2DC-CT Arm Currents during a Symmetrical AC Fault when $P_{dc,p} = P_{dc,n} = 75\ MW$

As for the LCC-HVDC bipole system quantities, there were barely any differences irrespective of power demand at either tapping station.

4.3.4 Symmetrical AC Fault at the Inverter Side AC Network

The symmetrical fault was triggered at $t = 3s$ and lasted $200ms$ but on the inverter side AC network in this case. The AC voltage variation was as expected as shown in Figure 4.30. All the phases of the AC network at the inverter dropped to zero while in that of the rectifier side, the amplitudes of all the AC voltage phases increased slightly. The peak amplitude measured was 554 kV on phase A of the rectifier AC network. Upon a successful restart, all the quantities returned to their nominal amplitudes after a few seconds. For this scenario, the pre-fault loading conditions was $P_{dc,p} = P_{dc,n} = 0\ MW$.

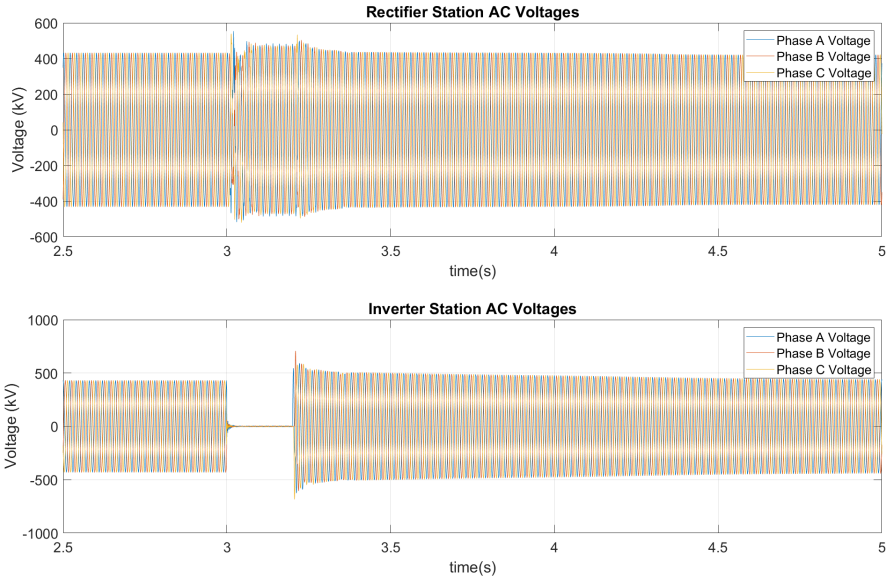


Figure 4.30: AC Network Voltages of LCC-HVDC System during a Three phase AC Fault at the Inverter Station with pre-fault loading scenario $P_{dc,p} = P_{dc,n} = 0\ MW$

The biggest differences were in the pole DC voltages and the LCC-HVDC system DC currents. Compared to when the fault was at the rectifier side, the DC voltages were zero at both poles and at all the stations. The fault had a severe effect on these voltages as the voltage suffered a change of almost 800 kV in a few milliseconds. Until the fault was cleared, the DC pole voltages remained at approcimately 0 kV. After the duration of the fault, all the DC voltages were returned to their nominal values in about half a second as shown in Figure 4.31. At $t = 5s$, the power tapping was resumed and the increased voltage ripple could be seen in V_{dc,tap_p} and V_{dc,tap_n} after a brief transient period. Another reason to set the common voltage threshold for fault detection at 400 kV was because of the variation in voltage that happened around $t = 3.25$. If the voltage threshold was any lower, the delay would be triggered again at this moment. Therefore, 400 kV was an ideal threshold to set for AC fault detections.

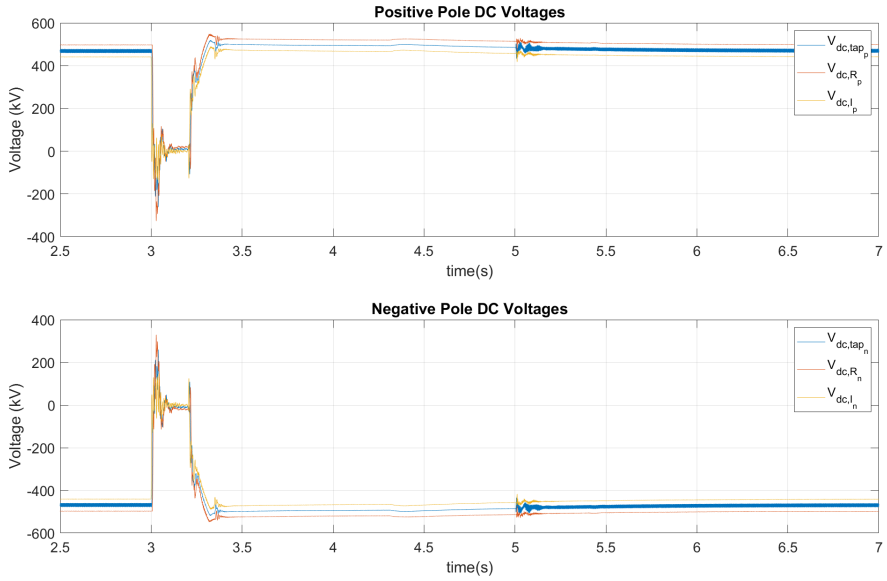


Figure 4.31: Pole DC Voltages of LCC-HVDC System during a Three phase AC Fault at the Inverter Station with pre-fault loading scenario $P_{dc,p} = P_{dc,n} = 0\ MW$

As for the DC currents, the response was completely different. The rectifier stations' CCA were actively controlling current and the DC currents were never extinguished. Instead, the rectifier DC currents, I_{dc,R_p} and I_{dc,R_n}, increased to around 5 kA at the moment the fault occurred and then dropped to 1 kA. The inverter DC currents had a similar response except that the peak current was at around 5.5 kA instead. Once the fault was cleared, the DC currents of the LCC-HVDC system were slowly increasing to their nominal values at 3 kA. At $t = 5s$, when the tapping stations resumed tapping at rated power, both the rectifier and inverter stations were operating normally. Figure 4.32 demonstrates these variations in the DC currents of the LCC-HVDC bipole system.

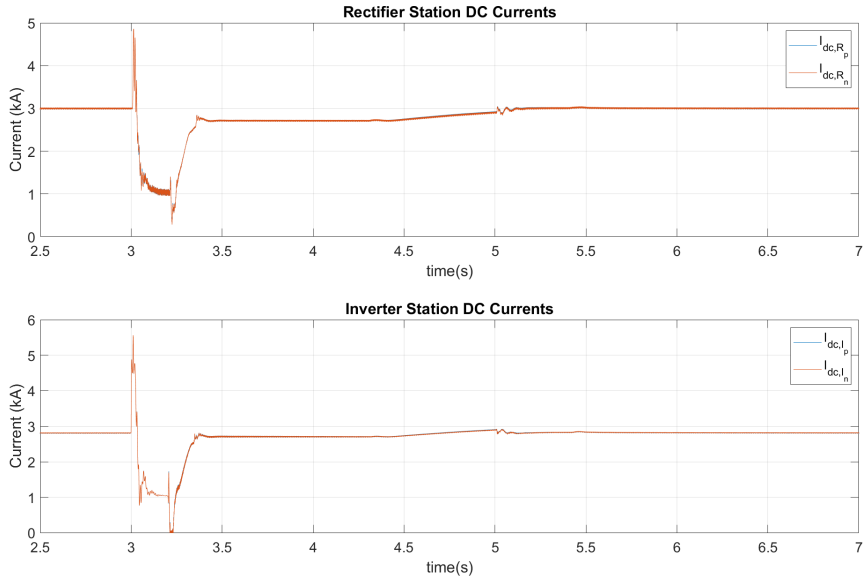


Figure 4.32: DC Currents of LCC-HVDC System during a Three phase AC Fault at the Inverter Station with pre-fault loading scenario $P_{dc,p} = P_{dc,n} = 0\ MW$

As mentioned previously, the variation of the firing and extinction angles were a good measure of the severity of an AC fault. For rectifier side AC fault, the symmetrical AC fault was the most severe. However, the symmetrical AC fault at the inverter side was as severe if not more. Both extinction angles, $\gamma_{I,p}$ and $\gamma_{I,n}$ were quickly dropped to zero while both of the firing angles increased to above 120°. As the fault cleared, $\alpha_{R,p}$ and $\alpha_{R,n}$, dropped to 5° and then went back to its nominal values during power tapping after several seconds. For $\gamma_{I,p}$ and $\gamma_{I,n}$, they initially increased to 61° and then gradually dropped to steady state values. Towards the end of plots in Figure 4.33, $\alpha_{R,p}$ and $\alpha_{R,n}$ were at 18.1° and 17.5° respectively. As for $\gamma_{I,p}$ and $\gamma_{I,n}$ were at 20.5° for both.

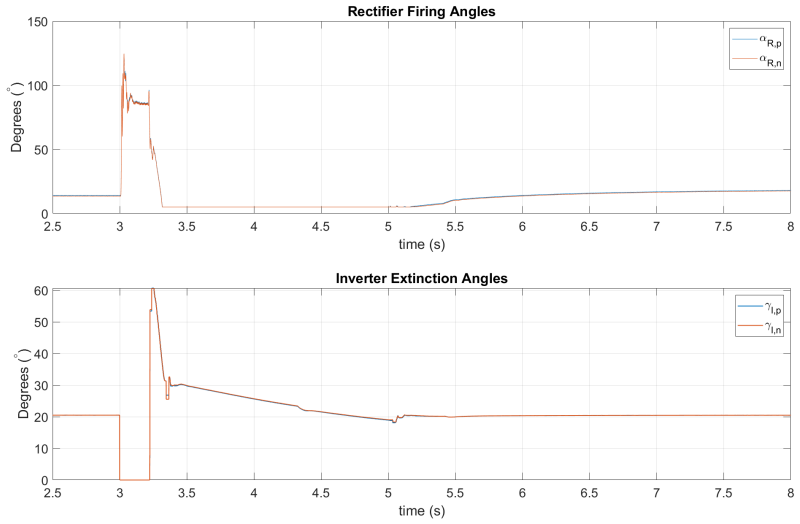


Figure 4.33: Firing Angles and Extinction Angles Variations during a Three phase AC Fault at the Inverter Station with pre-fault loading scenario $P_{dc,p} = P_{dc,n} = 0\ MW$

For the tapping stations, the main quantities that were different were the arm voltages mostly as they followed the same variations of the HVDC DC-link voltages. The result is shown in Figure 4.34. Again, when the fault was cleared while the SMs capacitors were blocked, the arm voltages were equal to the DC tapping voltages. The capacitor voltages as well as the DC currents of the tapping stations had the same variations as previously described.

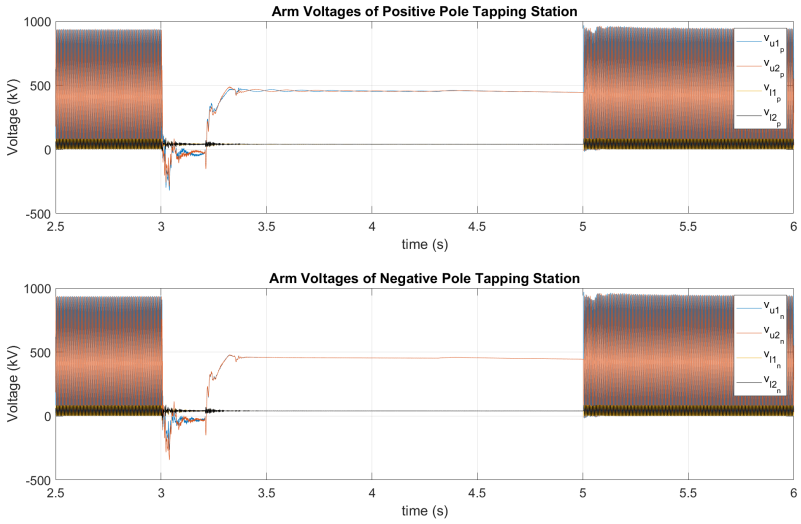


Figure 4.34: Arm Voltage Variations of Tapping Stations during a Three phase AC Fault at the Inverter Statio nwith pre-fault loading scenario $P_{dc,p} = P_{dc,n} = 0\ MW$

4.4 Summary

Two types of DC faults were studied in this chapter: a DC line-to-ground fault on the HVDC positve pole DC link, and a line-to-ground fault on the MVDC side of the positive pole tapping station. Symmetrical tapping was set in both cases considering $P_{dc} = 0\ MW$ and $P_{dc} = 75\ MW$. A voltage threshold of 400 kV was set as part of the controls system of the tapping stations to detect the faults. When such drops were detected, the SMs semiconductor switches were blocked to stop the propagation of the fault current through the M2DC-CTs, enabled by the use of full-bridge SMs in the upper arms. This blocked state would remain until the fault was cleared and after a set delay before a restart was attempted to ensure the LCC-HVDC Bipole system had recovered to its pre-fault loading scenario. If successful, the tapping stations would start tapping power at the same rate and amount as before the fault stage happened. As for MVDC side faults, they did not affect the tapping station on the opposing pole. The firing angles and the extinction angles at the rectifier and inverter respectively underwent some transients since, from the point of view of the LCC-HVDC bipole system, the changes that happened

were essentially increasing the inverter side DC currents back to their rated values of 3 kA due to P_{dc} dropping to 0 MW.

As for AC faults, two types of faults were discussed: one was a single line-to-ground fault on phase A of the rectifier side AC voltages, and the other one was a three phase line-to-ground AC fault at the rectifier side. Inverter side AC faults were also verified to check for any major differences the location of the fault might have on the HVDC DC-link at either pole. In the case of a symmetrical AC fault at the inverter, the system did not operate at a reduced voltage but in fact the DC link voltages collapsed to zero with some minor voltage ripples. The influence of VDCOL and RAML on the fault response and recovery was crucial for both DC and AC type faults. As for the tapping stations, the recovery period could also be altered by varying the delay after detecting a reduced voltage. It was also shown that as long as the tapping stations operated within power limits, the modes of operation of the LCC-HVDC bipole system did not change due to the tapping stations' control systems response to a fault, irrespective of the type and severity of the fault.

Chapter 5

Conclusion

Newer long distance power transmission systems are being implemented using HVDC technology whether they are LCC based or VSC based. Modern VSC based HVDC systems near exclusively use MMCs for their modularity and scalability. Tapping LCC-HVDC systems to extract a small amount of power (defined as 5% or less) from the main transmission lines can provide remote communities with power. To date, the majority of research regarding tapping has focused on single stage AC tapping methods that directly link the HVDC bus to an AC output bus ready for distribution networks. Little attention has been paid to the emerging topic of DC tapping using high step ratio DC-DC converters.

This thesis demonstrates the feasibility of independent two-stage DC tapping operation through the use of MMC based DC-DC converters connected in parallel to a pre-exisiting LCC-based HVDC Bipole system. This hybrid LCC-VSC HVDC system was implemented using a detailed 3 $GW, \pm 500$ kV LCC system based on the 3-Gorges LCC-Bipole system in China (available through RTDS), and two MMC based tapping stations. Each tapping station was equipped with a high voltage ratio (500 to 40) step down DC-DC converter (M2DC-CT) creating an output side 40 kV MVDC bus.

Several power flow tapping scenarios were investigated through both symmetrical and asymmetrical tapping as well as power flow reversal. During symmetrical tapping, the power demand in both tapping stations were the same ($P_{dc,p} = P_{dc,n}$) while for asymmetrical tapping, $P_{dc,p} \neq P_{dc,n}$. Revers-

ing the power flow represented power injection into the LCC system through the tapping station M2DC-CTs. Both AC and DC faults were also studied. For AC faults, both symmetrical and asymmetrical line-to-ground faults were triggered at either the rectifier station or the inverter station AC networks. As for DC faults, one type of DC fault was a line-to-ground fault on the DC link of the LCC HVDC system at the positive pole. The other DC fault was a line-to-ground fault on the MVDC bus side of the M2DC-CT on the positive pole tapping station.

5.1 Thesis Contribution

The following list summarizes the main contributions of this thesis:

1. A new hybrid LCC-VSC HVDC Bipole system was developed starting with the detailed LCC-HVDC bipole system available through RTDS (based on the 3-Gorges system in China). This LCC-HVDC system was augmented by adding two tapping stations, one per pole, connected in parallel with the LCC-HVDC lines at their halfway points. Each tapping station comprises a high step ratio modular multilevel dc-dc converter (M2DC-CT) designed to create a $\pm 40\ kV$ MVDC bus. The resulting hybrid LCC-VSC HVDC Bipole was used as a benchmark system to carry out power flow studies, fault studies as well as renewable energy integration feasibility. Simulating this hybrid system on the RTDS NovaCor simulator provided a more realistic study as compared to other tapping simulation studies in the literature, due to (i) the high level of detail in the LCC-HVDC model and its associated controls that are reflective of real-world systems, and (ii) the ability to operate the tapping stations independently. Parameters and modes of operation can be changed simultaneously during the runtime and thus the results obtained highlight flexibility of this hybrid system with regards to different types of studies.

2. With the M2DC-CTs operating at any power tapping demand up to the rated power of 75 MW, it was confirmed that the existing LCC-based

Bipole HVDC system control modes of operation did not change. This is critically important to verify as the tapping stations should not alter the performance of the LCC-HVDC system. The main observed changes were a decrease in the inverter side DC current equal to the tapping DC current of the tapping station at the respective pole, as expected. There were minor changes to the transformer tap position to accomodate for these decreases in inverter DC currents, and therefore power tapping may impact life cycle operation of onload transformer tap changers.

3. The power tapping operations of both tapping stations were confirmed to be independent of the other. Whether $P_{dc,p} = P_{dc,n}$ or not, the response of one power tapping station does not directly affect that of the other except in terms of higher order harmonics. Therefore, the MVDC output bus can handle unbalanced loads.

4. Using two independently operating power tapping stations (one on each pole) to tap power simultaneously was found to increase second order and fourth order harmonics in the entire system (with respect to the fundamental frequency of the M2DC-CT, i.e 150 Hz). When one station is tapping power from the LCC system while the other is injecting power into the system, harmonics decrease significantly as the harmonic currents now flow in opposite directions. Maximum harmonics cancellation occurred when one tapping station tapped rated power while the other one injected rated power. Passive filters were designed to mitigate the unwanted harmonics at the input side of the M2DC-CTs.

5. A power ramp rate of 750 MW/s was confirmed to be appropriate for tapping applications. Increasing this rate does increase the transient amplitudes and overshoots in some quantities, as would be expected. Even if higher ramp rates do result in faster systems (lower settling times), the difference in settling times is not substantial when comparing the 750 MW/s power demand ramp rate to the most severe case of 3000 MW/s one.

6. The presence of tapping stations does not negatively affect the response of the existing LCC-based HVDC bipole system to AC or DC faults. With the proper response from the controls of the M2DC-CTs upon fault detection, there are very minor differences in the responses. Even when the fault was on the 40 kV side of the M2DC-CTs, the effect on the LCC system was fairly small. That is, the M2DC-CTs are able to block faults as needed, courtesy of using full-bridge SMs in the upper arms.

From these studies and the results obtained, the LCC-based HVDC bipole system functions as expected with or without the tapping stations. There were no changes to modes of operation when investigating different power flow scenarios as demonstrated in Chapter 3. This validates the normal and continuous operation of both the LCC-HVDC system regarding balanced and unbalanced loads. Also, by injecting power into the LCC-HVDC system, renewable energy integration as well as distributed energy resources were shown to be feasible. In AC or DC fault scenarios, both tapping stations and the LCC system fully recovered and resumed pre-fault loading scenarios. With the tapping stations functioning independently, having faults on the MVDC bus did not require any changes to be made to the LCC-HVDC system as it continued its normal operation with the proper control modes still active and unchanged. By validating all the aforementioned scenarios, the hybrid LCC-VSC HVDC system can be implemented without making any control changes to the existing LCC system and this opens up even more possibilities for future studies.

5.2 Future Work

1. Building upon this exising model of a hybrid LCC-VSC HVDC Bipole system, the downstream MVDC buses can be integrated with distribution AC networks via interfacing DC-AC converters. This will give a direct insight into real world applications of power tapping.

2. Hardware in the loop control studies can be implemented using the real

time simulation model to study the detailed bipole system even further, with focus on the testing of the tapping controls on physical hardware.

3. Additional fault studies can be carried out after implementing AC distribution networks connected to the MVDC bus, and their effects on the main LCC-HVDC system can be analyzed.

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Appendix A

Background Material

Rectifier Side Symmetrical AC Faults Results with and without tapping stations:

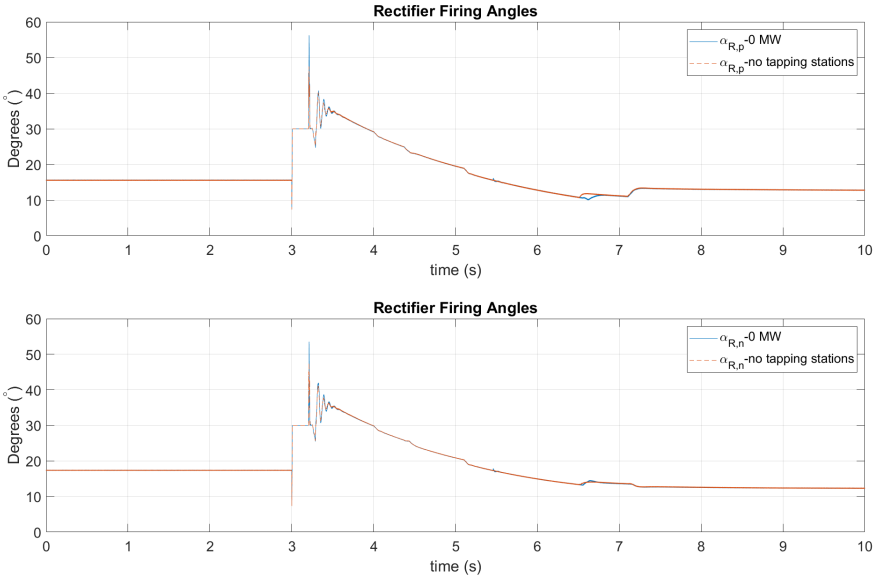

Figure A.1: Comparison of Rectifier Firing Angles with and without the presence of tapping stations

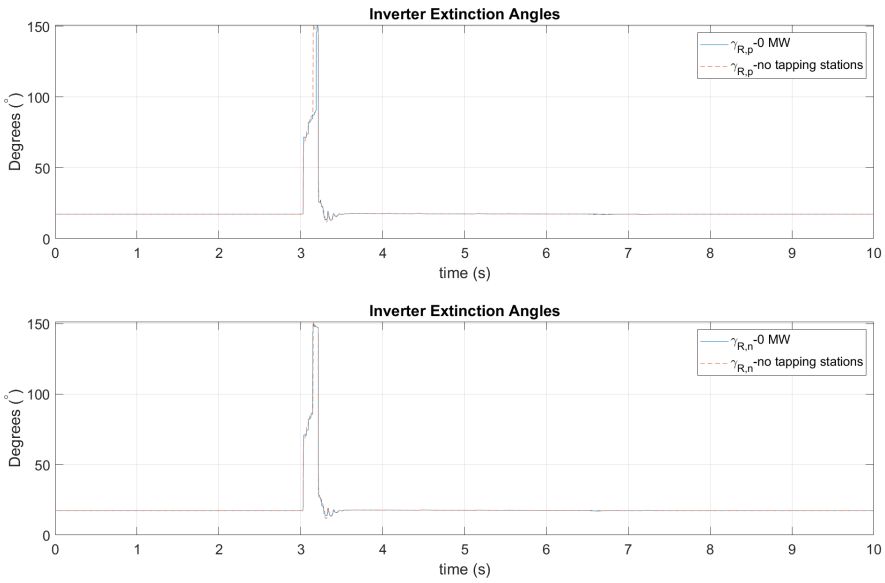

Figure A.2: Comparison of Inverter Extinction Angles with and without the presence of tapping stations