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Design and Realization of a Novel Class of Highly Stable High-Resolution Oversampled Σ-Δ A/D Converter Configurations

by

Neil A. Fraser 

A thesis submitted to the Faculty of Graduate Studies and Research in partial fulfillment of the requirements for the degree of **Master of Science.**

Department of Electrical and Computer Engineering

Edmonton, Alberta
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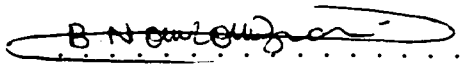

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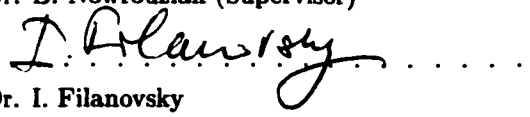

Dr. I. Filanovsky

Dr. L. K. Stewart

Date: June 12, 2001

I dedicate this thesis to my parents Robert and Donna Fraser and to my sister Alison Fraser

Abstract

This thesis is concerned with the design and realization of higher-order high-resolution oversampled Σ-Δ analog-to-digital (A/D) converter configurations. The design and realization of a set of hitherto feedforward and multiple-feedback Σ-Δ A/D converters is first reviewed. This is followed by an investigation of the achievable signal-to-quantization-noise ratio, dynamic range, and stability of the corresponding switched-capacitor (SC) hardware implementation for this set of Σ-Δ A/D converter configurations. A novel statistical approach for the estimation of the maximum DC input signal level for stable A/D converter operation is then presented. The hitherto Σ-Δ A/D converters are usually based on, a) complementary signal and noise transfer functions, and/or b) unit-circle noise transfer function zeros. This thesis is further concerned with the development of novel Σ-Δ A/D converters having, instead, magnitude-squared or magnitude complementary signal and noise transfer functions. The proposed A/D converters exhibit resolution and dynamic range properties similar to those of the existing feedforward and multiple-feedback Σ-Δ A/D converters, but offer increased stability performance in the presence of capacitor mismatches in the corresponding SC hardware implementations. In addition, the SC hardware implementation of the resulting A/D converters leads to a capacitance spread which is comparable to that of hitherto Σ-Δ A/D converters.

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Chapter 1

Introduction

In its most general sense, a signal is used to convey information. One can distinguish between two classes of signals. The signals within the first class have a value defined at all times and are referred to as continuous-time signals. An example of such a signal is the reading from a thermometer which can be taken at any time. The signals within the second class have values defined only at specified time instances and are referred to as discrete-time signals. A typical example of this type of signal is a graph of daily precipitation as functions of time.

One can further characterize continuous-time and discrete-time signals in terms of their range of values. If a signal can take on any value within a specified range, it is referred to as a continuous-amplitude (non-quantized) signal. On the other hand, if the signal can take on only a finite number of values from a specified range, it is referred to as a discrete-amplitude (quantized) signal. An example of a continuous-amplitude signal is the reading taken from a mercury thermometer. If the temperature reading was taken from a thermometer with a digital display, then this would be a discrete-amplitude signal.

Two important types of signals exist, namely, analog signals and digital signals. An analog signal is a signal which is both continuous in time and amplitude, whereas a digital signal is a signal which is both discrete in time and amplitude. The images, sounds, and smells that we perceive everyday are examples of analog signals. An example of a digital signal is a photograph taken with a digital camera as the photograph is stored in memory inside the camera.

With the invention of transistors and eventually the modern-day digital computers (digital signal processors (DSP)), digital signals are found in a wide variety of applications. Given that all perceived signals are analog signals and that they are to be processed digitally (using a digital signal processor), some type of conversion between the two types of signals is required. The process of converting an analog signal to a digital signal is referred to as analog-to-digital (A/D) conversion. The digital output of such a system is then processed by a DSP and may then be converted to an analog signal through the reverse process called digital-to-analog (D/A) conversion. Figure 1.1 shows a simple block diagram of a typical digital signal processing system.

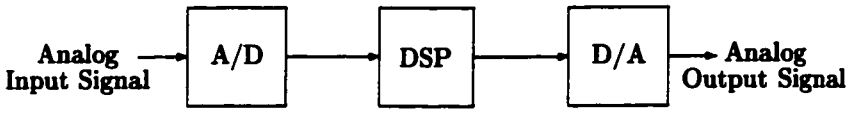

Figure 1.1: Typical Digital Signal Processing System

One can distinguish between two types of A/D converters[1], namely, Nyquist-rate and oversampled A/D converters. Nyquist-rate converters are used in high-speed applications, such as video and radar signal processing, as they convert the minimum possible number of analog input signal samples to their corresponding digital counterparts. However, the precision of the analog components constituent in the hardware implementation of the Nyquist-rate A/D converters limits the resolution (i.e. the number of bits) in the digital output signal samples. Further difficulties are encountered with the anti-aliasing filter as it must realize a sharp transition band to bandlimit the input signal spectrum. Oversampled converters, on the other hand, find application in lower speed applications such as digital hearing aids, as they convert a larger number of analog input signal samples to their corresponding digital representations. As a result of taking more input signal samples, the anti-aliasing filter can be realized in a straightforward fashion. Moreover, oversampled A/D converters can achieve high-resolution by using even low tolerance analog components, making them easier to implement than their Nyquist-rate counterpart.

The present thesis is concerned with a practical representative type of oversampled A/D converters, namely, the Σ-Δ A/D converters. Section 1.1 introduces the process of sampling and quantization. Section 1.2 is concerned with Nyquist-rate A/D converters while Section 1.3 is concerned with oversampled A/D converters. Section 1.4 introduces the basic concepts of oversampled Σ-Δ A/D converters. The hardware implementation of Σ-Δ A/D converters is then considered in Section 1.5. Section 1.6 is concerned with a discussion of some existing problems associated with Σ-Δ A/D converters. Finally, an overview of this thesis is presented in Section 1.7.

1.1 A/D Conversion

All A/D converters must convert a continuous-time continuous-amplitude (analog) signal to a discrete-time discrete-amplitude (digital) signal. The first task may be accomplished through a process called sampling, while the second task may be accomplished through a process called quantization. The general process is shown in Fig. 1.2, where an analog input signal $u(t)$ is first sampled by a switch which opens and closes at the sampling frequency f_s to produce a discrete-time continuous-amplitude signal $u^*(n)$. The signal $u^*(n)$ is then quantized to produce the digital signal $u(n)$.

The function of the quantizer is to map a signal defined over a continuous range of amplitudes to a signal defined over a discrete set of amplitudes. The simplest quantizer is the one-bit quantizer

[1]The same considerations apply to the corresponding D/A converters.

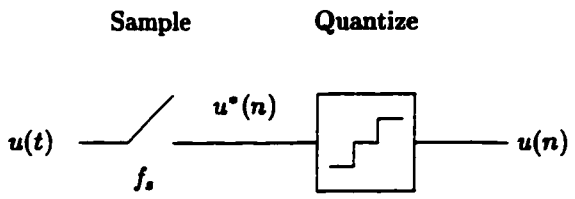

Figure 1.2: Generalized A/D Converter

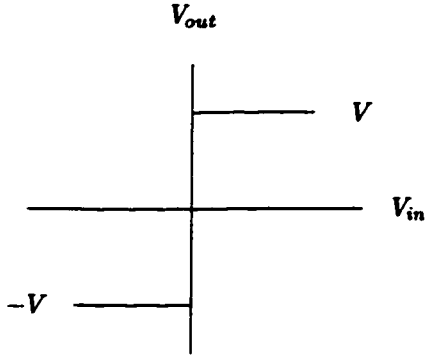

Figure 1.3: One-Bit Quantizer

shown in Fig. 1.3, having only two output levels V and $-V$ corresponding to the digital output '1' and '0', respectively. When the quantizer input signal is less than zero, the quantizer generates an output $-V$, and when the quantizer input signal is greater than or equal to zero, the quantizer generates an output V.

The quantizer is characterized by the number of output bits N and the quantization step size Δ. The number of bits N produced by the quantizer determines the number of quantizer levels Q in accordance with

$$Q = 2^N. \tag{1.1}$$

The quantization step size Δ is in turn determined by the maximum output (input) signal amplitude V and the number of quantization levels Q in accordance with

$$\Delta = \frac{2V}{Q-1}. \tag{1.2}$$

By replacing Q in Eqn. 1.2 from Eqn. 1.1, one obtains

$$\Delta = \frac{2V}{2^N - 1} \approx \frac{2V}{2^N} \quad for \quad N \gg 1. \tag{1.3}$$

The process of quantization may be most easily described by example.

Example: A quantizer which produces a two-bit ($N = 2$) output has four output levels Q ($Q = 2^2$, c.f. Eqn. 1.1) corresponding to the quantizer shown in Fig. 1.4, where the quantizer step size Δ can

Table 1.1: Quantizer Output Signal Levels

$v(n_1)$	Output Level	Output Code
$-V \leq v(n_1) < -V + \Delta$	$-V$	00
$-V + \Delta \leq v(n_1) < 0$	$-V + \Delta$	01
$0 \leq v(n_1) < V - \Delta$	$V - \Delta$	10
$V - \Delta \leq v(n_1) < V$	V	11

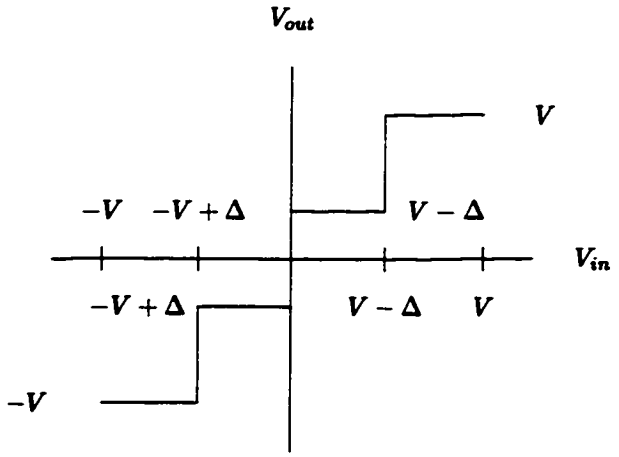

Figure 1.4: Four-Bit Quantizer

be determined from Eqn. 1.3 as

$$\Delta = \frac{2V}{2^2 - 1} \tag{1.4}$$

$$= \frac{2V}{3}. \tag{1.5}$$

Consider the quantizer input signal $v(n)$ at sample time n_1. The corresponding output of the quantizer may be determined from Table 1.1.

As far as the sampling process is concerned, one may distinguish between two classes of A/D converters, namely Nyquist-rate A/D converters and oversampled A/D converters.

1.2 Nyquist-rate A/D Converters

Nyquist-rate A/D converters sample the analog input signal at the Nyquist-rate $f_s = 2f_b$, where f_b is the highest frequency component of the input signal (Oppenheim et. al., [1]). If the input signal is not bandlimited to f_b, an anti-aliasing filter must be used before the sampling process takes place (to prevent aliasing). Figure 1.5 shows the spectrum of the sampled input signal. A typical frequency response of the anti-aliasing filter is shown in Fig. 1.6. Notice that the response of the anti-aliasing filter must have a very narrow transition band to ensure that the filtered signal is not

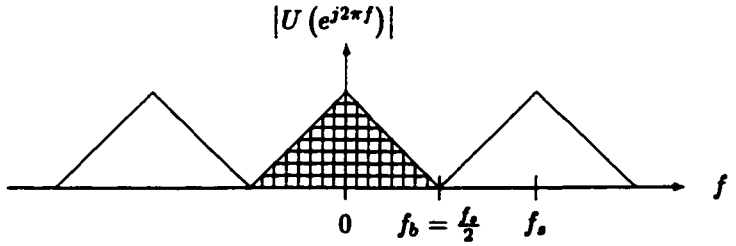

Figure 1.5: Frequency Spectrum of Input Signal

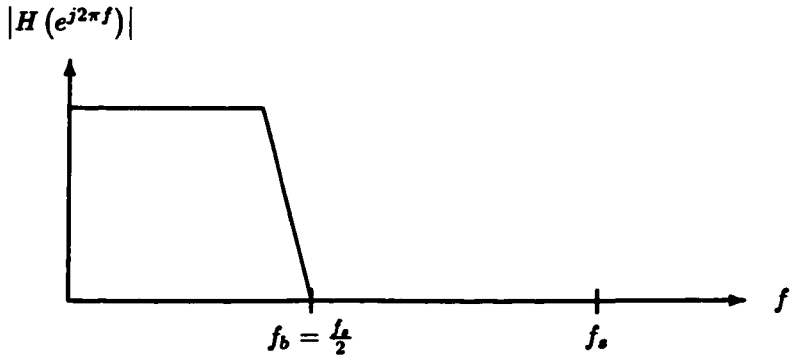

Figure 1.6: Anti-Aliasing Filter Requirement for Nyquist-Rate A/D Converters

magnitude distorted and does not contain any frequency components above $\frac{f_s}{2}$. The necessity of a narrow transition band makes the anti-aliasing filter difficult to realize.

Due to the nonlinear nature of the quantizer, any system employing a quantizer becomes complicated to analyse. Since the quantizer is introducing an error into the system, one may regard it as an additive white noise source, characterized by a quantization noise signal $e(n)$, with equal probability of lying anywhere in the range $\pm\frac{\Delta}{2}$. As a result of this characterization, one may determine the quantization noise power to be (Candy et. al., [2])

$$\sigma_{es}^2 = \frac{\Delta^2}{12}. \tag{1.6}$$

An important performance measure of any A/D converter is the signal-to-quantization-noise ratio ($SQNR$). It is most generally defined as the ratio between the signal power σ_u^2 and the quantization noise power σ_{es}^2 as

$$SQNR = \frac{\sigma_u^2}{\sigma_{es}^2}. \tag{1.7}$$

By substituting Eqn. 1.3 into Eqn. 1.6, one may find the quantization noise power σ_{es}^2 as

$$\sigma_{es}^2 = \frac{V^2}{3(2^{2N})}. \tag{1.8}$$

By substituting Eqn. 1.8 into Eqn. 1.7, one is led to the well known result

$$SQNR_{dB} = 10log_{10}\frac{\sigma_u^2}{V^2} + 6.02N + 4.77. \tag{1.9}$$

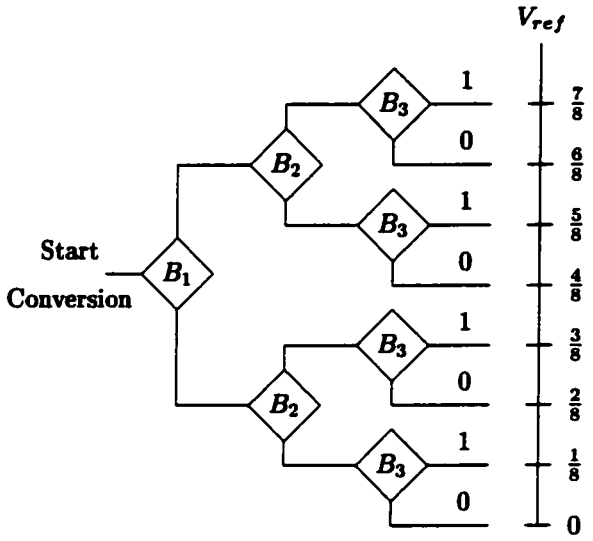

Figure 1.7: Successive Approximation Search Path

It is easily noticed from the above equation that each additional bit of quantization increases the $SQNR$ by 6 dB.

Example: Consider a standard compact disc which requires a sampling frequency of 44.1 *kHz (to sample the 20 kHz bandlimited input signal) and* 96 *dB of SQNR. Using the largest sinusoidal input signal possible (with an amplitude of V and the power* $\frac{V^2}{2}$*) and solving for N in Eqn. 1.9, one finds that a* 16*-bit quantizer is required (i.e.* $N = 16$*).*

Nyquist-rate A/D converters can fall into one of two broad categories, namely serial and parallel (J. M. Demler [3]). Typical examples of serial converters include successive approximation, bit-serial pipelined, and algorithmic A/D converters. The most popular type of Nyquist-rate A/D converter is a parallel converter known as a flash A/D converter. The basic operation of the successive approximation and flash A/D converters will be discussed in the following two subsections.

1.2.1 Successive Approximation A/D Converters

The most widely used type of Nyquist-rate A/D converter is the successive approximation converter (J. M. Demler, [3]). After each clock period, one bit of the digital word is resolved with the most-significant-bit first. This type of conversion is best described as a tree-type search as shown in Fig. 1.7 (J. M. Demler, [3]). In this example, at the start of the conversion cycle, the input voltage level V_{in} is compared to half the reference voltage V_{ref}. If V_{in} is greater than half of V_{ref}, then B_1 is set to 1 and the search continues up the tree. Otherwise, B_1 is set to 0 and the search continues down the tree. In this way, if B_1 was set to one, then in the next iteration the input voltage level V_{in} is compared to three quarters of the reference voltage V_{ref} to determine B_2. A N-bit result requires N comparisons of this nature.

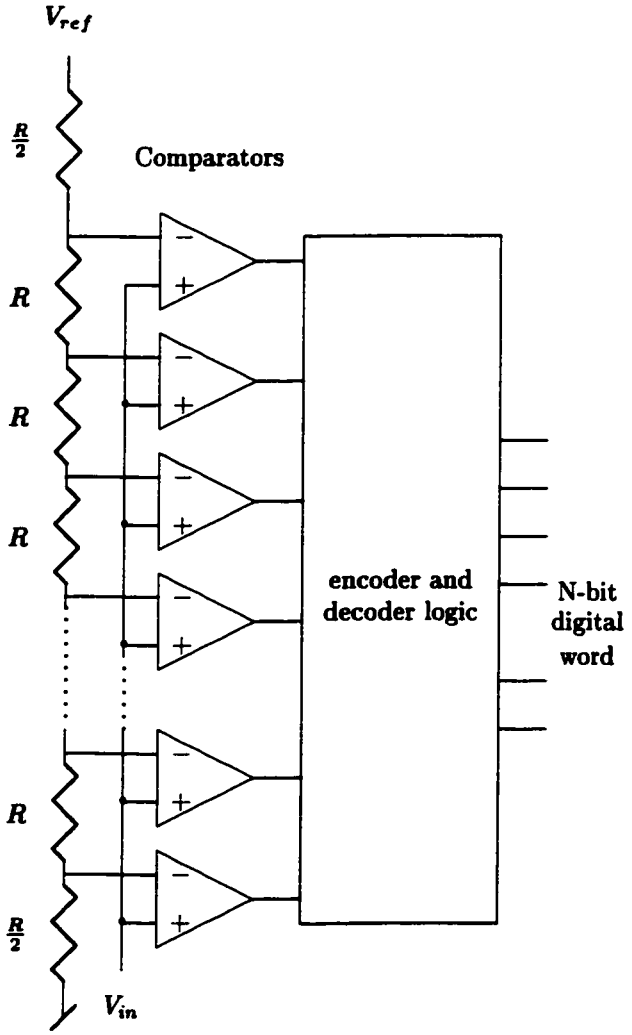

Figure 1.8: Flash A/D Generalized Architecture

1.2.2 Flash A/D Converters

The flash A/D converter outputs a digital word every clock period, making it the fastest A/D converter (J. M. Demler, [3]). The basic flash A/D converter configuration is as shown in Fig. 1.8. For a N-bit output word, $(2^N - 1)$ comparators are required making this type of A/D converter very expensive in terms of hardware. Every additional bit of resolution that is added doubles the amount of circuitry required, thus increasing power consumption (J. M. Demler, [3]). The resistor string is responsible for generating each quantizer voltage level from the reference voltage V_{ref}. Each comparator compares the input voltage V_{in} level to the corresponding quantizer voltage level. If the input voltage V_{in} is less than the quantizer voltage level, the comparator outputs the voltage level corresponding to the digital bit 0. Otherwise, the comparator outputs the voltage corresponding to the digital bit 1. The input to the encoder and decoder logic is a $(2^N - 1)$ bit thermometer code which is then coded into N-bits.

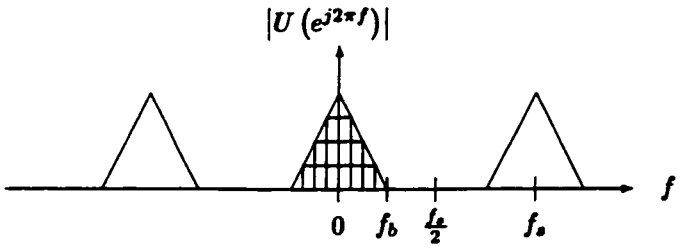

Figure 1.9: Frequency Spectrum of Input Signal

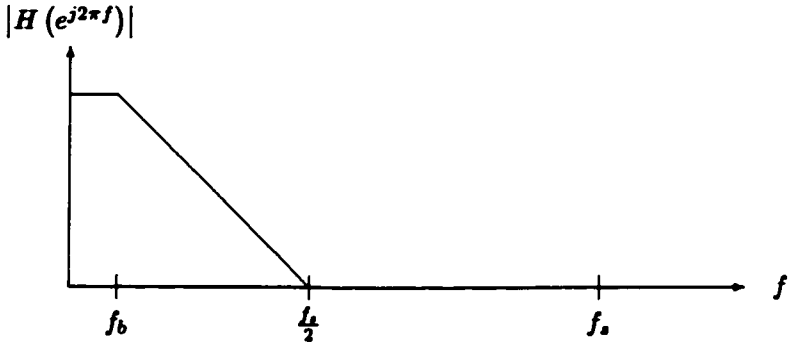

Figure 1.10: Anti-Aliasing Filter Requirement for Oversampled A/D Converter

1.3 Oversampled A/D Converters

Oversampled A/D converters sample the input signal at a rate higher than the Nyquist-rate. The degree to which the input signal is oversampled is referred to as the oversampling ratio (OSR) defined in accordance with

$$OSR = \frac{f_s}{2f_b}. \tag{1.10}$$

The spectrum of the sampled input signal in oversampled A/D converters is shown in Fig. 1.9. Notice that to ensure the analog input signal is bandlimited to f_b, an anti-aliasing filter with a frequency response as shown in Fig. 1.10 is required. One may notice from the figure that the transition band of the anti-aliasing filter can be significantly relaxed as compared to that of Fig. 1.6 for the Nyquist-rate A/D converter. In the remainder of this thesis, it is assumed that the analog input signals to all A/D converters have been filtered by an appropriate anti-aliasing filter to avoid undesirable aliasing effects.

The noise power $\sigma_{e_s}^2$ in the case of Nyquist A/D converters was given by Eqn. 1.6. In the case of oversampled A/D converters, the noise power $\sigma_{e_s}^2$ is given by (Candy et. al., [2])

$$\sigma_{e_s}^2 = \frac{\Delta^2}{12 \times OSR}. \tag{1.11}$$

By substituting for Δ from Eqn. 1.3 into Eqn. 1.11, and, in turn, by substituting the result into the expression for $SQNR$ from Eqn. 1.7, one gets

$$SQNR_{dB} = 10log_{10}\frac{\sigma_u^2}{V^2} + 6.02N + 10log_{10}OSR + 4.7712. \tag{1.12}$$

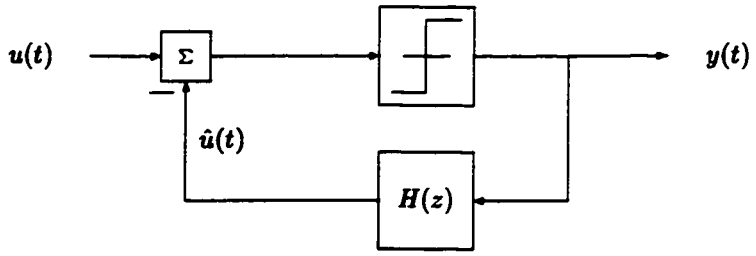

Figure 1.11: Generic Δ-Modulator

This result implies that the noise power is inversely proportional to the sampling frequency f_s. Consequently, a doubling of the sampling frequency leads to a 3 dB increase in $SQNR$.

Example: Consider a standard 20 kHz audio signal. In order to achieve 96 dB of SQNR, Eqn. 1.12 implies that a $N = 12$-bit quantizer employing an oversampling ratio of $OSR = 160$ is required (assuming a sinusoidal signal with amplitude V and with the power $\frac{V^2}{2}$).

Two widely used types of oversampled A/D converters exist, namely, a) Δ-modulators, and b) Σ-Δ A/D converters.

1.3.1 Oversampled Δ-Modulators

A widely used oversampled A/D converter is known as a Δ-modulator. A simple block diagram of a Δ-modulator is shown in Fig. 1.11 (B. P. Lathi et. al., [4]). In this configuration, the quantizer is in the feedforward path while the integrator is in the feedback path. The difference between the input signal $u(t)$ and feedback signal $\hat{u}(t)$ is quantized. The signal $\hat{u}(t)$ tries to follow the input signal. Δ-modulation suffers from a condition known as slope overload. In this condition, the input signal $u(t)$ changes too fast for the feedback signal $\hat{u}(t)$ to follow it. The maximum change that $\hat{u}(t)$ can track is given by $f_s\Delta$, where f_s is the sampling frequency and Δ is the quantizer step size. As an example consider a sinusoidal input signal

$$u(t) = A cos\omega t. \tag{1.13}$$

Then, the maximum slope of the input signal $u(t)$ may be determined as

$$\frac{du(t)}{dt} = -A\omega sin(\omega t), \tag{1.14}$$

$$\left|\frac{du(t)}{dt}\right| = A\omega. \tag{1.15}$$

In order to avoid the slope overload condition, it is required that

$$A\omega < f_s\Delta. \tag{1.16}$$

The next section is concerned with oversampled Σ-Δ A/D converters, the main theme of the present thesis.

1.4 Σ-Δ A/D Converters

1.4.1 First-Order Σ-Δ A/D Converter

The general configuration of an oversampled Σ-Δ A/D converter contains a loop filter $H(z)$ and a one-bit quantizer embedded in a feedback loop as shown in Fig. 1.12, where $u(n)$ represents the

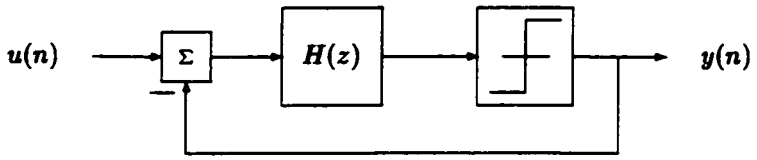

Figure 1.12: Generic Σ-Δ A/D Converter Configuration

input signal and $y(n)$ represents the corresponding output signal. In its simplest form, $H(z)$ is an integrator as indicated in Fig. 1.13. By inspection of this Σ-Δ A/D converter one may obtain an expression for the output signal $y(n)$ in terms of the input signal $u(n)$ and quantizer noise signal $e(n)$ (defined in Section 1.2) (Candy et. al., [2]) as

$$y(n) = u(n-1) + e(n) - e(n-1). \tag{1.17}$$

Through the application of the z-transform, one may obtain the expression

$$Y(z) = z^{-1}U(z) + E(z)(1 - z^{-1}) \tag{1.18}$$

where $Y(z)$ represents the z-transformed output signal, $U(z)$ represents the z-transformed input signal, and $E(z)$ represents the z-transformed quantization noise.

Let us define the signal transfer function as

$$STF(z) \equiv \frac{Y(z)}{U(z)}, \tag{1.19}$$

and the noise transfer function as

$$NTF(z) \equiv \frac{Y(z)}{E(z)}. \tag{1.20}$$

Then, from Eqn. 1.18 it follows that

$$STF(z) = z^{-1}, \tag{1.21}$$

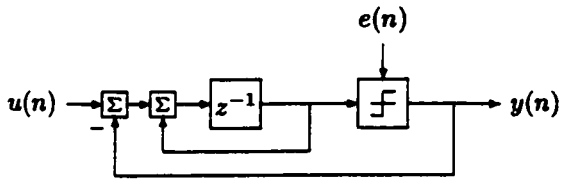

Figure 1.13: Single-loop Σ-Δ A/D Converter Configuration

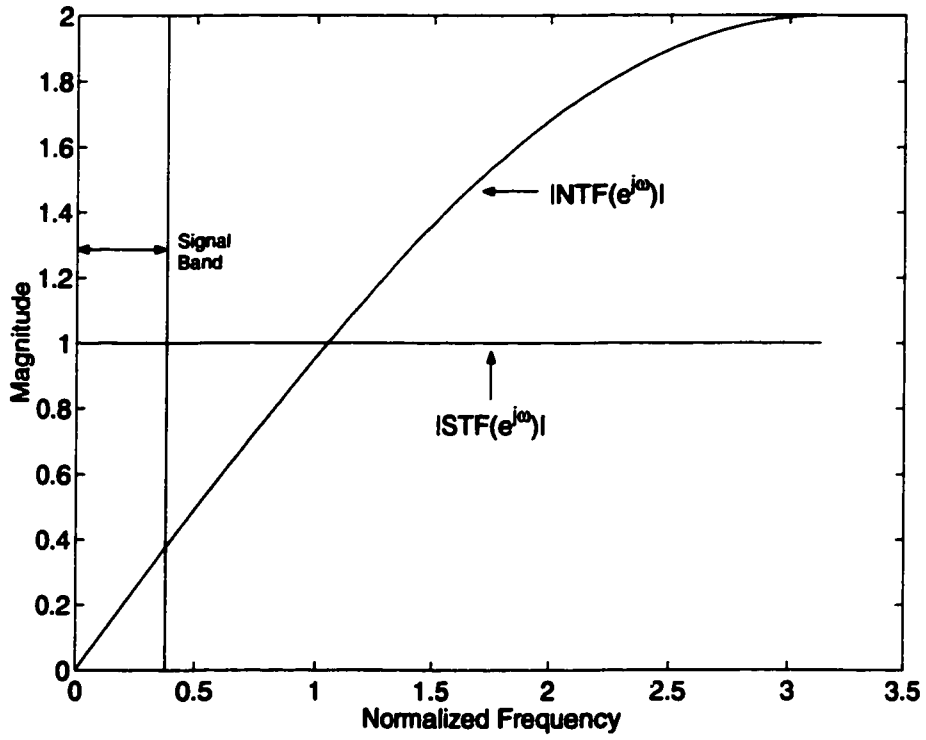

Figure 1.14: Signal and Noise Transfer Function for Single-Loop Σ-Δ A/D Converter Configuration

and

$$NTF(z) = 1 - z^{-1}. \tag{1.22}$$

This A/D converter is referred to as a first-order Σ-Δ A/D converter as the maximum power of z^{-1} in the noise transfer function is 1. A magnitude-frequency plot of $STF(z)$ and $NTF(z)$ is shown in Fig. 1.14. As is evident from Fig. 1.14, the noise gain is very small at low frequencies (in the signal band) and becomes larger at higher frequencies. For this reason, Σ-Δ A/D converters are known as noise shaping converters, meaning that the noise is shaped away from the signal band. Furthermore, since the noise has a highpass characteristic, this converter is known as a lowpass Σ-Δ A/D converter. As explained in the previous section, the quantizer may be replaced by a uniformly distributed additive white noise source $e(n)$. An analysis of the first-order Σ-Δ A/D converter reveals that the quantization noise is given by (Candy et. al., [2])

$$\sigma_{es}^2 = \frac{\Delta^2}{12}\frac{\pi^2}{3}(2\frac{f_b}{f_s})^3. \tag{1.23}$$

Substituting the definition of OSR given by Eqn. 1.10 into the definition of $SQNR$ given by Eqn. 1.7 results in

$$SQNR_{dB} = 10log_{10}\frac{\sigma_u^2}{V^2} + 30log_{10}OSR - 0.4. \tag{1.24}$$

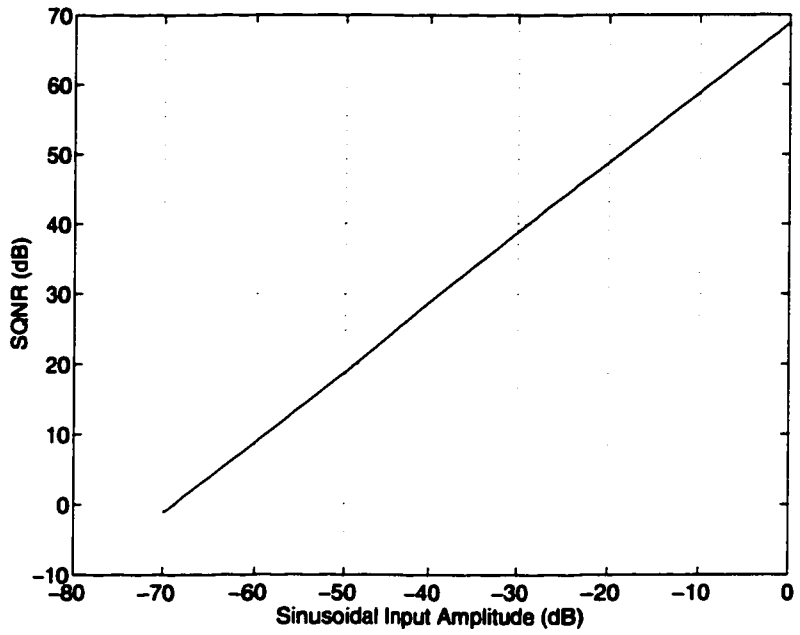

Figure 1.15: Theoretical $SQNR$ versus Input Signal Amplitude

From the above equation, each doubling of the oversampling ratio improves the $SQNR$ by 9 dB.

A plot of Eqn. 1.24 is shown in Fig. 1.15 for $OSR = 256$. As evident from Fig. 1.15 the peak-$SQNR$ ($PSQNR$) of 68.8 dB is achieved with an input amplitude of 1. It is expedient at this time to define the dynamic range (DR) as the negative of the input amplitude where 0 dB $SQNR$ is achieved (Norsworthy et. al., [5]). In this case a DR of 68.8 dB is observed.

Example: Consider a standard 20 kHz audio signal. If a SQNR of 96 dB is to be achieved, Eqn. 1.24 implies a sampling frequency of 81.92 MHz is required (assuming a sinusoidal signal of amplitude V and the power $\frac{V^2}{2}$).

1.4.2 Motivation for Σ-Δ A/D Converters

The main motivation behind employing Σ-Δ A/D converters is the ability to obtain high $SQNRs$ by using a very simple (coarse) one-bit quantizer. Furthermore, the A/D converter may be implemented using high tolerance analog components, implying that they are not sensitive to noise and interference.

1.4.3 Disadvantages of Σ-Δ A/D Converters

From the generic Σ-Δ A/D converter shown in Fig. 1.12, it is possible to rearrange the loop filter $H(z)$ and produce the equivalent model shown in Fig. 1.16. Notice that the Δ-modulator is exactly the same as the Σ-Δ A/D converter with the exception that the input signal $u(t)$ is filtered by $H(z)$ before the summing block.

Given that Σ-Δ A/D converters are based on Δ-modulators, a similar phenomenon to slope

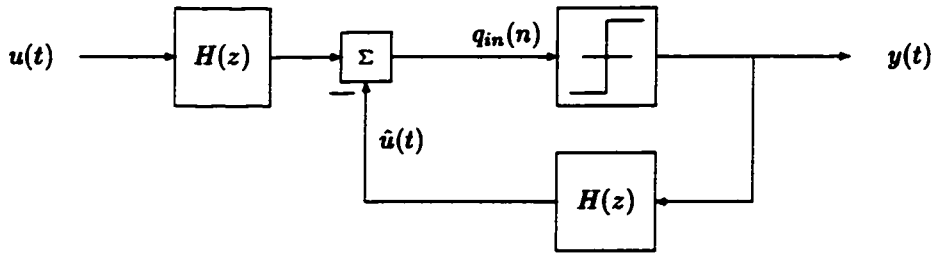

Figure 1.16: Generic Σ-Δ A/D Converter Configuration

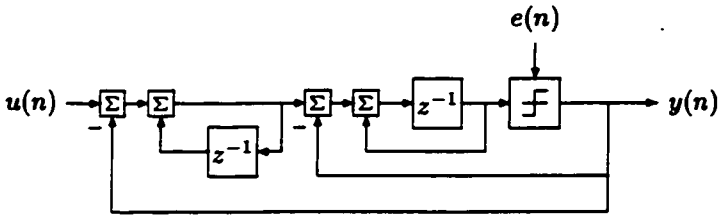

Figure 1.17: A Second-order Σ-Δ A/D Converter

overload is observed, namely, instability. In (Borsodi, [6]), the quantizer is said to be overloaded when

$$|q_{in}(n)| > Q\frac{\Delta}{2}, \tag{1.25}$$

where $q_{in}(n)$ represents the input signal to the quantizer. As a result it was shown in (Borsodi, [6]) that in the case of a first-order Σ-Δ A/D converter, the maximum input amplitude A_1 is defined in accordance with

$$A_1 \leq (Q-1)\frac{\Delta}{2}. \tag{1.26}$$

When this relationship is not satisfied, the Σ-Δ A/D converter exhibits unstable operation. In higher-order Σ-Δ A/D converters, no analytic solution of the maximum input signal exists and must be discovered through extensive simulations. Therefore, the design of stable higher-order Σ-Δ A/D converters is usually done through a trial-and-error process by experienced designers.

1.4.4 Higher-Order Σ-Δ A/D Converters

The motivation to employ higher-order Σ-Δ A/D converters is to obtain an improvement in the noise attenuation in the signal band without increasing the sampling frequency. As a result of this improved noise attenuation, the $SQNR$ is increased as compared to the first-order Σ-Δ A/D converter. The simplest case of a higher-order converter is the second-order Σ-Δ A/D converter shown in Fig. 1.17.

The output of this type of Σ-Δ A/D converter can be determined to be (Candy et. al., [2])

$$y(n) = u(n-1) + (e(n) - 2e(n-1) + e(n-2)). \tag{1.27}$$

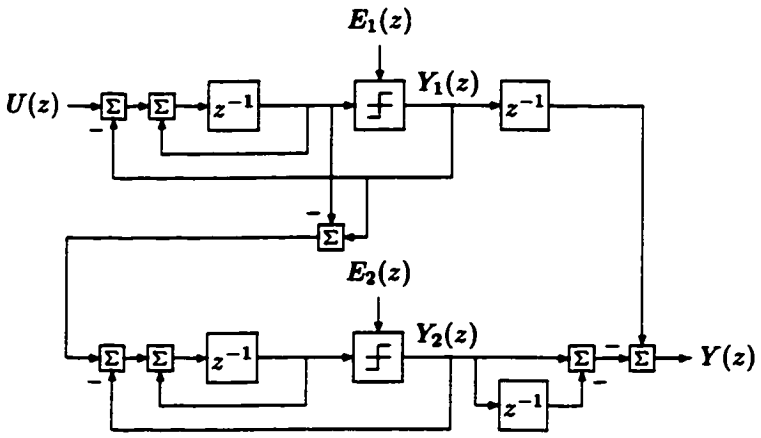

Figure 1.18: Cascaded Σ-Δ A/D Converter Configuration

A further analysis of this A/D converter reveals that the quantization noise power is given by (Candy et. al., [2])

$$\sigma_{es}^2 = \frac{\Delta^2}{12}\frac{\pi^4}{5}\frac{f_b}{f_s}^5. \tag{1.28}$$

By employing a one-bit quantizer, the following expression is obtained for $SQNR$

$$SQNR_{dB} = 10log_{10}\frac{\sigma_u^2}{V_2} + 1.82 + 50log_{10}OSR. \tag{1.29}$$

This result implies that the $SQNR$ is increased by 15 dB for every doubling of the oversampling ratio (OSR).

Example: Consider a standard 20 kHz audio signal. If a SQNR of 96 dB is to be achieved, Eqn. 1.29 implies that a sampling frequency of only 3.52 MHz is required (assuming a sinusoidal signal of amplitude V and the power $\frac{V^2}{2}$).

1.4.5 Cascaded Σ-Δ A/D Converters

A very widely used form of Σ-Δ A/D converters is the cascaded configuration shown in Fig. 1.18 (Aziz et. al., [7]). In this configuration, the quantization error from the first converter is the input to the second converter. The output signal from each converter is then summed in an attempt to cancel the noise from the first converter. A simple analysis of the configuration leads to the following expressions for the two quantizer output signals $Y_1(z)$ and $Y_2(z)$

$$Y_1(z) = U(z)z^{-1} + E_1(z)(1 - z^{-1}), \tag{1.30}$$

$$Y_2(z) = E_1(z)z^{-1} + E_2(z)(1 - z^{-1}). \tag{1.31}$$

The overall output of the system is given by

$$Y(z) = Y_1(z)z^{-1} - Y_2(z)(1 - z^{-1}) \tag{1.32}$$

$$= U(z)z^{-2} - E_2(z)(1 - z^{-1})^2. \tag{1.33}$$

Notice from Eqn. 1.33 that the noise term $E_1(z)$ has been eliminated. In this way, the noise in the output signal $Y(z)$ has been reduced without resorting to higher order structures where stability may be a problem. However, this type of configuration is highly susceptible to component mismatches (Aziz et. al., [7]).

1.4.6 Bandpass Σ-Δ A/D Conversion

Thus far, only lowpass Σ-Δ A/D converters have been discussed. In particular, the noise transfer function has had a highpass magnitude-frequency characteristic while the signal transfer function has had a lowpass magnitude-frequency characteristic. Another type of converter is known as a bandpass Σ-Δ A/D converter, as first introduced in (Schreier et. al., [8]). This type of converter features a bandstop noise transfer function and a bandpass signal transfer function. Such converters find applications in AM digital radios or receivers for digital cellular mobile radios (Aziz et. al., [7]).

Recall that in the case of lowpass Σ-Δ A/D converters, the oversampling ratio is a function of both the sampling frequency f_s and the bandlimiting frequency f_b of the input signal. In order to have a large oversampling ratio with a high bandlimiting frequency f_b, the sampling frequency f_s must also be large.

Example: Assume $OSR = 64$ and $f_b = 400$ kHz. In accordance with the definition of OSR from Eqn. 1.10, a sampling frequency of $f_s = 51.2\ MHz$ must be employed.

In the case where the input signal does not have frequency content in the region 0 to f_a ($f_a \ll f_b$), noise may be shaped into this region. The oversampling ratio is then defined as

$$OSR' = \frac{f_s}{2(f_b - f_a)}. \tag{1.34}$$

In this way, the oversampling ratio is a function of the sampling frequency f_s and the signal bandwidth $f_b - f_a$ (as opposed to the bandlimiting frequency f_b only). As a result, if the bandlimiting frequency f_b is large, as long as $f_a \gg 0$, the sampling frequency does not need to be excessively large.

Example: Assume $OSR = 64$, $f_b = 400$ kHz, and $f_a = 300$ kHz. In accordance with the definition of OSR' from Eqn. 1.34, a sampling frequency of $f_s = 12.8MHz$ must be employed.

In the case of lowpass A/D converters, the noise was attenuated at frequencies in the range 0 to f_b. This was done by placing the zeros of the noise transfer function in this frequency range. In the case of bandpass A/D converters, on the other hand, the signal occupies a frequency range f_a to f_b, where $f_a < f_b$. In this way, the noise may occupy the frequencies from 0 to f_a and from f_b to $f_s/2$. To facilitate this characteristic, the zeros of the noise transfer function must be moved to the frequency region f_a to f_b.

Feedforward and multiple-feedback Σ-Δ A/D converters are a class of converters which are capable of realizing bandpass signal transfer functions and bandstop noise transfer functions. Typical examples include the cascade-of-integrators, the cascade-of-resonators, and their combination, namely the cascade-of-resonators/integrators (see Section 3.2).

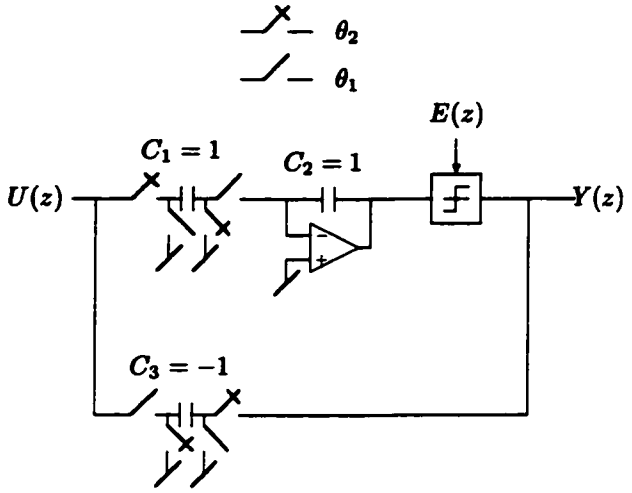

Figure 1.19: First-Order Σ-Δ A/D Converter SC Hardware Implementation

1.5 Switched-Capacitor Hardware Implementation of Oversampled Σ-Δ A/D Converter Configurations

For the most part, Σ-Δ A/D converters are implemented using switched-capacitor (SC) circuits (Candy et. al., [2]). Such circuits are widely used in digital signal processing and are relatively cheap to manufacture as compared to continuous-time implementations. Furthermore, SC circuit hardware implementations are advantageous for low-power low-voltage applications (Shahriar et. al., [9]).

Consider the SC hardware implementation of the first-order Σ-Δ A/D converter shown in Fig. 1.19. An analysis of this circuit reveals that

$$\frac{Y(z)}{U(z)} = \frac{\frac{C_1}{C_2}}{z - 1 - \frac{C_3}{C_2}}, \tag{1.35}$$

$$\frac{Y(z)}{E(z)} = \frac{z - 1}{z - 1 - \frac{C_3}{C_2}}. \tag{1.36}$$

When $C_1 = 1$, $C_2 = 1$, and $C_3 = -1$, the signal and noise transfer functions are equivalent to those previously determined for the first-order Σ-Δ A/D converter. However, during the manufacturing process, these capacitors may differ from their nominal values by up to 0.5% (Schreier et. al., [10]). As a result, different signal and noise transfer functions are realized which may affect the achievable $SQNR$ and dynamic range performance of the A/D converter. In fact, the effect of capacitor tolerances may even result in unstable A/D converter operation.

1.6 Open Problems in Σ-Δ A/D Conversion

1.6.1 Design

The design of Σ-Δ A/D converters is heavily based on a trial-and-error process. After a signal and noise transfer function have been obtained (by approximation), extensive simulations are required to ensure that the A/D converter provides adequate $SQNR$ and DR performance. In addition, Monte-Carlo analysis is required to determine the effect of capacitor mismatches in a corresponding SC hardware implementation on the achievable $SQNR$, DR, and stability performance of the resulting A/D converter. Several attempts have been made to address the problem of achieving a desired $SQNR$ and DR performance level. These attempts rely on extensive simulations to determine a set of guidelines relating the oversampling ratio and the order of the converter to the achievable $SQNR$. The most notable set of guidelines was made by (Kuo et. al., [11]). Other attempts by (Lee, [12]) and (W. M. Snelgrove et. al., [13]) amount to limiting the out-of-band noise transfer function gain so as to achieve high stability. However, the design of high-resolution, high-dynamic range oversampled Σ-Δ A/D converters having low sensitivity to capacitor mismatches in a corresponding SC hardware implementation still remains an open problem.

1.6.2 Stability Prediction

As mentioned in the previous subsection, the successful design of Σ-Δ A/D converters is heavily dependent on extensive simulations to determine the achievable $SQNR$ and dynamic range. The problem of predicting dynamic range has also been studied in the hitherto literature, the most notable was the statistical estimation technique by (Ardalan et. al., [14]). This technique provides an estimation of the maximum DC input signal to the A/D converter. However, this technique is suitable for Σ-Δ A/D converters having Gaussian distributed quantizer input signals. Extending this technique to arbitrarily distributed quantizer input signals still remains an open problem.

1.7 Overview of the Thesis

Chapter 2 is concerned with the characterization of five practical feedforward and multiple-feedback Σ-Δ A/D converter configurations. These configurations are characterized in terms of two important features, namely, a) the location of their noise transfer function zeros with respect to the unit-circle in the complex z-plane, and b) the relationship between their constituent signal and noise transfer functions.

Chapter 3 presents a design procedure for feedforward and multiple-feedback Σ-Δ A/D converter configurations. This design procedure is based on a set of high-level system design specifications and proceeds in a step-by-step manner. Each of the five feedforward and multiple-feedback A/D converters are then designed and simulated to determine, a) the effect of the noise transfer function zeros on the achievable $SQNR$ and dynamic range (DR), and b) the effect of capacitor mismatch on

the $SQNR$ and DR in a corresponding SC hardware implementation using Monte-Carlo analysis. To estimate the maximum DC input signal level, a hitherto statistical technique is employed. This statistical technique is based on several assumptions, the most restricting of which is that the quantizer input signal is Gaussian distributed. A novel statistical approach is then presented which generalizes the hitherto technique to the case of arbitrary quantizer input signal distributions. Design examples are presented to demonstrate and compare the hitherto and proposed statistical techniques.

Chapter 4 is concerned with the design and realization of a novel class of Σ-Δ A/D converters based on magnitude-squared or magnitude complementary signal and noise transfer functions. These novel Σ-Δ A/D converter configurations are obtained by modifying the existing configurations.

Chapter 5 is concerned with an investigation of the proposed class of Σ-Δ A/D converters. It is demonstrated that the A/D converters in this class exhibit a high degree of stability in the presence of capacitor mismatches in their corresponding SC hardware implementation when compared to the existing converters. It will further be demonstrated that the achievable $SQNR$ and DR remain very similar to that achieved by the feedforward and multiple feedback converters.

Chapter 6 presents the final conclusions of this thesis and presents some research topics suitable for future work.

Chapter 2

Feedforward and Multiple-feedback Σ-Δ A/D Converter Configurations

2.1 Introduction

A generic Σ-Δ A/D converter is shown in Fig. 2.1, where $U(z)$ represents the z-transformed input signal, and where $Y(z)$ represents the z-transformed output signal. In design situations, the

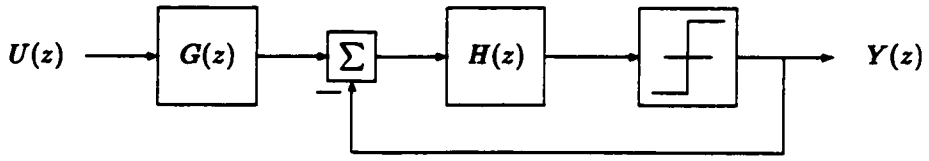

Figure 2.1: Generic Σ-Δ A/D Converter Configuration

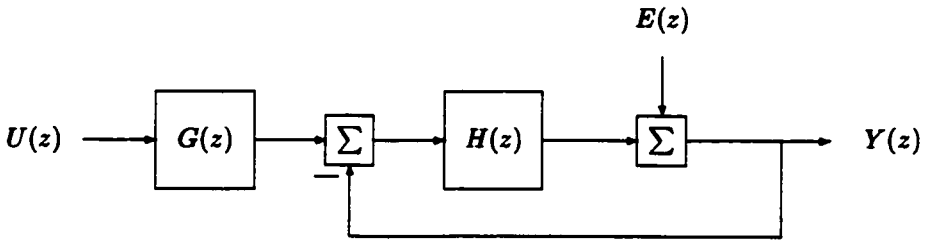

Figure 2.2: Generic Linear Σ-Δ A/D Converter Configuration

constituent quantizer is usually replaced by a uniformly distributed additive white noise source (Candy et. al., [2]) as shown in Fig. 2.2, where $E(z)$ represents the (z-transformed) quantization noise. Then, the A/D converter may be characterized by the signal transfer function $STF(z)$ and the noise transfer function $NTF(z)$ in accordance with

$$STF(z) = \frac{G(z)H(z)}{1 - H(z)} \equiv G(z)\frac{S(z)}{D(z)}, \tag{2.1}$$

$$NTF(z) = \frac{1}{1 - H(z)} \equiv \frac{N(z)}{D(z)}. \tag{2.2}$$

From the definition of $NTF(z)$ given in Eqn. 2.2, one may express $H(z)$ in accordance with

$$H(z) = \frac{N(z) - D(z)}{N(z)}. \tag{2.3}$$

By substituting this expression for $H(z)$ into Eqn. 2.1, one gets

$$STF(z) = \frac{G(z)\,(N(z) - D(z))}{D(z)}. \tag{2.4}$$

If $G(z)$ is assumed to be a polynomial in z, then one may note from Eqns. 2.4 and 2.2 that the signal and noise transfer functions share a common denominator. Furthermore, if $G(z) = 1$ then, the numerator of the signal transfer function may be formed in accordance with,

$$S(z) = N(z) - D(z). \tag{2.5}$$

A relationship between the signal and noise transfer functions may then be formed in accordance with

$$NTF(z) - STF(z) = 1. \tag{2.6}$$

When a given signal and noise transfer function satisfy Eqn. 2.6, they are said to be complementary transfer functions. One of the main practical advantages of such a pair of transfer functions is that by deriving the noise transfer function (or the signal transfer function) the signal transfer function (or the noise transfer function) can be easily obtained from Eqn. 2.6, thus eliminating the need to derive both transfer functions.

It is expedient to recast the polynomial $D(z)$ in the form

$$D(z) = \mathcal{Z}^T \mathcal{D}, \tag{2.7}$$

and the polynomials $N(z)$ and $S(z)$ in the forms

$$N(z) = \mathcal{Z}^T \mathcal{N}, \tag{2.8}$$

$$S(z) = \mathcal{Z}^T \mathcal{S}, \tag{2.9}$$

where $\mathcal{Z}^T = [z^0, z^{-1}, z^{-2}, \cdots, z^{-N}]$, where $\mathcal{D}$, $\mathcal{N}$, and $\mathcal{S}$ are column vectors of length $(N+1)$ whose entries depend on the system parameters of the Σ-Δ A/D converter, and where N is the order of the A/D converter. In this way, by invoking Eqns. 2.7, 2.8, and 2.9 in Eqn. 2.5, one obtains

$$\mathcal{D} = \mathcal{N} - \mathcal{S}. \tag{2.10}$$

In addition to the relationship between the signal and noise transfer functions, the position of the noise transfer function zeros is also of particular practical interest. The zeros of the noise transfer function $NTF(z)$ are directly related to the poles of the loop transfer function $H(z)$. For maximum noise attenuation, the zeros of the noise transfer function must be located directly on the unit circle.

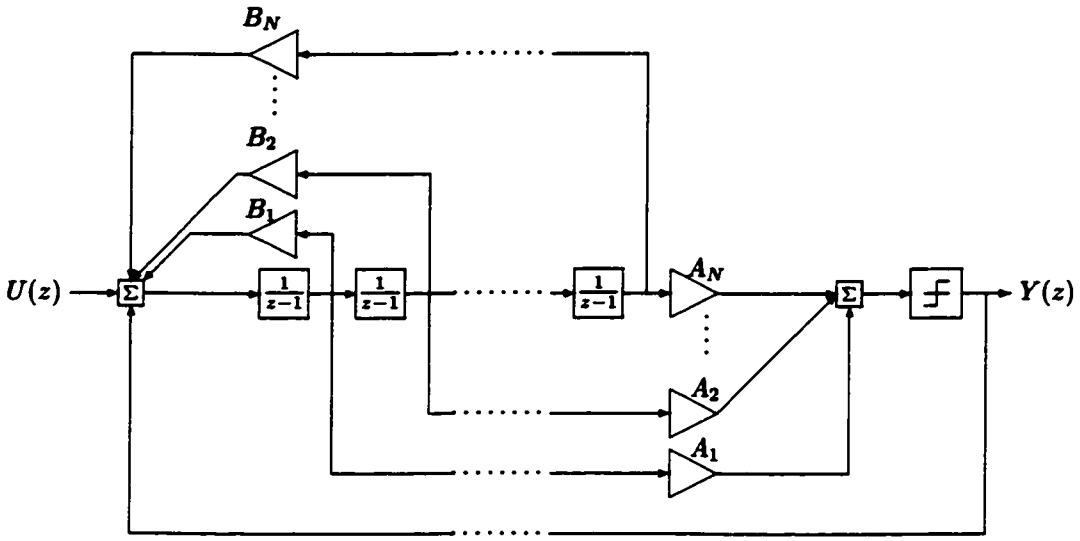

Figure 2.3: Cascade-of-Integrators Σ-Δ A/D Converter Configuration

This chapter is concerned with characterization and practical realization of five widely used feedforward and multiple-feedback Σ-Δ A/D converter configurations. In particular, Section 2.2 introduces these Σ-Δ A/D converter configurations, and characterizes them in terms of the complementarity of their signal and noise transfer functions and in terms of the location of their noise transfer function zeros. It will be shown that three cases exist with respect to the complementarity of the signal and noise transfer functions and that three different cases exist with respect to the location of the noise transfer function zeros. In addition, a technique is presented to determine the parameters of each Σ-Δ A/D converter configuration starting from given signal and/or noise transfer functions. Finally, a simple method is described for obtaining the corresponding SC hardware implementation associated with each Σ-Δ A/D converter configuration.

2.2 Five Widely Used Feedforward and Multiple-Feedback Σ-Δ A/D Converter Configurations

2.2.1 Cascade-of-Integrators Σ-Δ A/D Converter Configuration

The cascade-of-integrators (COI) Σ-Δ A/D converter configuration, developed in (Lee et. al., [15]) and shown in Fig. 2.3, features both feedforward and feedback signal paths. In order to determine the contribution of the multiplier coefficients A_{1-N} and B_{1-N} on the signal and noise transfer functions, a detailed analysis of the COI Σ-Δ A/D converter configuration can be undertaken. The results of this analysis show that the numerator of the signal transfer function is given by

$$S(z) = \sum_{i=1}^{N} A_i (z-1)^{N-i}, \tag{2.11}$$

the numerator of the noise transfer function is given by

$$N(z) = (z-1)^N - \sum_{i=1}^{N} B_i (z-1)^{N-i}, \tag{2.12}$$

and the denominator of the signal and noise transfer functions is given by

$$D(z) = N(z) - S(z). \tag{2.13}$$

Evidently, the COI Σ-Δ A/D converter configuration guarantees the complementarity of the signal and noise transfer functions (c.f. Eqns. 2.13 and 2.5). Furthermore, the multiplier coefficients B_{1-N} determine the location of the noise transfer function zeros and the multiplier coefficients A_{1-N} determine the location of the signal transfer function zeros (c.f. Eqns. 2.12 and 2.11, respectively).

To realize a given signal or noise transfer function, one must determine the corresponding A and B multiplier values. It can be shown that these multiplier values are given in accordance with

$$\mathcal{A}^T = \mathcal{C}_{1COI}^{-1} \mathcal{S} \tag{2.14}$$

$$\mathcal{B}^T = \mathcal{C}_{2COI}^{-1} \mathcal{N}, \tag{2.15}$$

where $\mathcal{A} = [0, A_1, A_2, \cdots, A_N]$, where $\mathcal{B} = [1, B_1, B_2, \cdots, B_N]$, and where $\mathcal{C}_{1COI}$ and $\mathcal{C}_{2COI}$ are $(N+1) \times (N+1)$ matrices. Moreover, the matrices $\mathcal{C}_{1COI}$ and $\mathcal{C}_{2COI}$ may be determined as described in the following.

First, let us form the polynomials $L_i(z) = (1 - z^{-1})^i$ for $i = 1, 2, \cdots, N$. Then, by recasting these polynomials in the form $L_i(z) = \mathcal{Z}^T \mathcal{L}_i$, one obtains the column vectors $\mathcal{L}_i$ of length $(i+1)$. It can be shown that the matrices $\mathcal{C}_{1COI}$ and $\mathcal{C}_{2COI}$ have the forms

$$\mathcal{C}_{1COI} = \begin{bmatrix} 0 & 0 & 0 & \cdots & 0 & 0 \\ 0 & \mathcal{L}_{N-1} & 0 & \cdots & 0 & 0 \\ 0 & & \mathcal{L}_{N-2} & \ddots & 0 & 0 \\ \vdots & & & \ddots & \vdots & \vdots \\ 0 & & & & \mathcal{L}_1 & 0 \\ 0 & & & & & \mathcal{L}_0 \end{bmatrix} \tag{2.16}$$

$$\mathcal{C}_{2COI} = \begin{bmatrix} \mathcal{L}_N & 0 & 0 & \cdots & 0 \\ & -\mathcal{L}_{N-1} & 0 & \cdots & 0 \\ & & -\mathcal{L}_{N-2} & \ddots & 0 \\ & & & \ddots & \vdots \\ & & & & -\mathcal{L}_0 \end{bmatrix} \tag{2.17}$$

The salient features of these matrices are, a) they are lower triangular, reducing the computational cost required for their inversion, and b) they are independent of the multiplier coefficients A and B.

As an example, by considering the case of $N = 4$, one has

$$C_{1COI} = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 & 0 \\ 0 & -3 & 1 & 0 & 0 \\ 0 & 3 & -2 & 1 & 0 \\ 0 & -1 & 1 & -1 & 1 \end{bmatrix} \tag{2.18}$$

and

$$C_{2COI} = \begin{bmatrix} 1 & 0 & 0 & 0 & 0 \\ -4 & -1 & 0 & 0 & 0 \\ 6 & 3 & -1 & 0 & 0 \\ -4 & -3 & 2 & -1 & 0 \\ 1 & 1 & -1 & 1 & -1 \end{bmatrix}. \tag{2.19}$$

The COI Σ-Δ A/D converter configuration must be replaced to its corresponding SC hardware implementation for practical realization. By inspection of the COI A/D converter configuration, one may note that the configuration is composed of three primary elements, namely, a) an integrator, b) a multiple weighted input adder, and c) a combined adder (with multiple weighted inputs [1]) and an integrator. The corresponding SC hardware implementation of each of these elements is shown in Fig. 2.4. As an example consider the 2-nd order COI A/D converter configuration shown in Fig. 2.5, where the each primary element has been enclosed in a dashed box. Then, by replacing the primary elements by their corresponding SC hardware implementations as shown in Fig. 2.4, one obtains the overall SC hardware implementation of the second-order COI A/D converter configuration as shown in Fig. 2.6, where the dashed boxes enclose the corresponding SC hardware primary elements.

[1] Later in this chapter it will be shown that some inputs to the adder are weighted by a constant and a unit-advance term z.

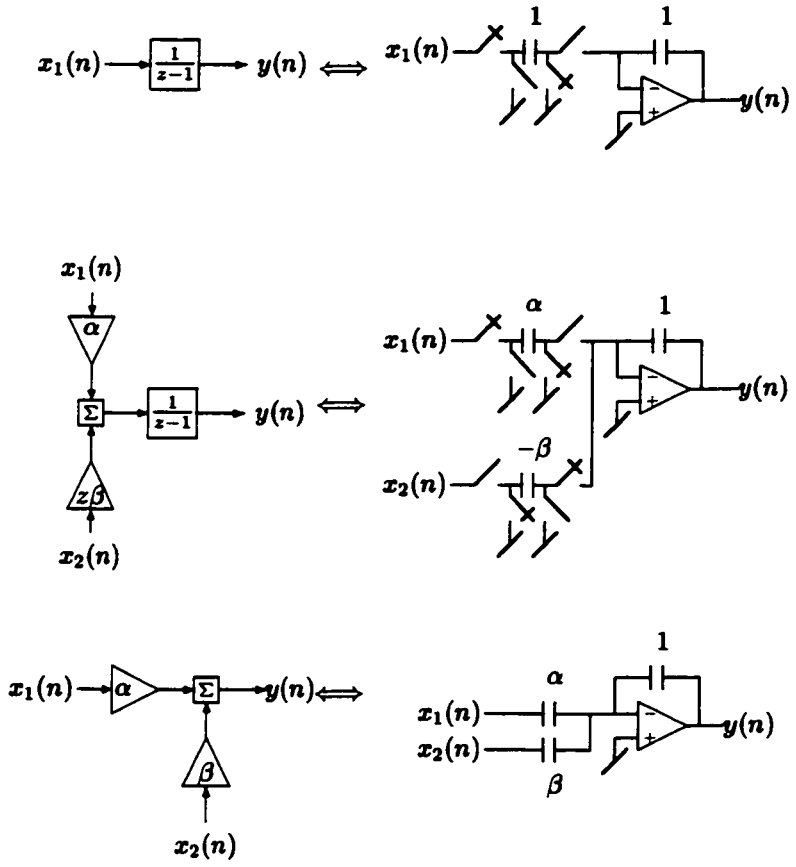

Figure 2.4: Basic SC Hardware Implementation Building Blocks

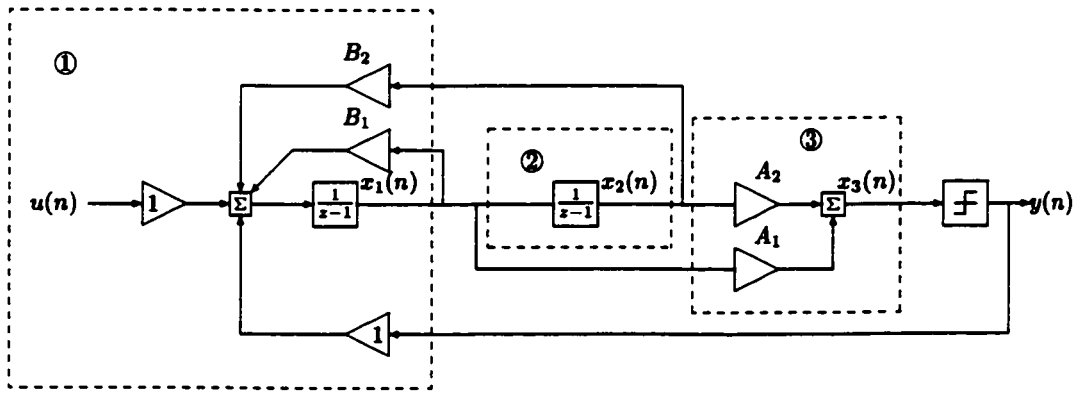

Figure 2.5: Identification of the Primary Elements in a 2-nd Order COI A/D Converter

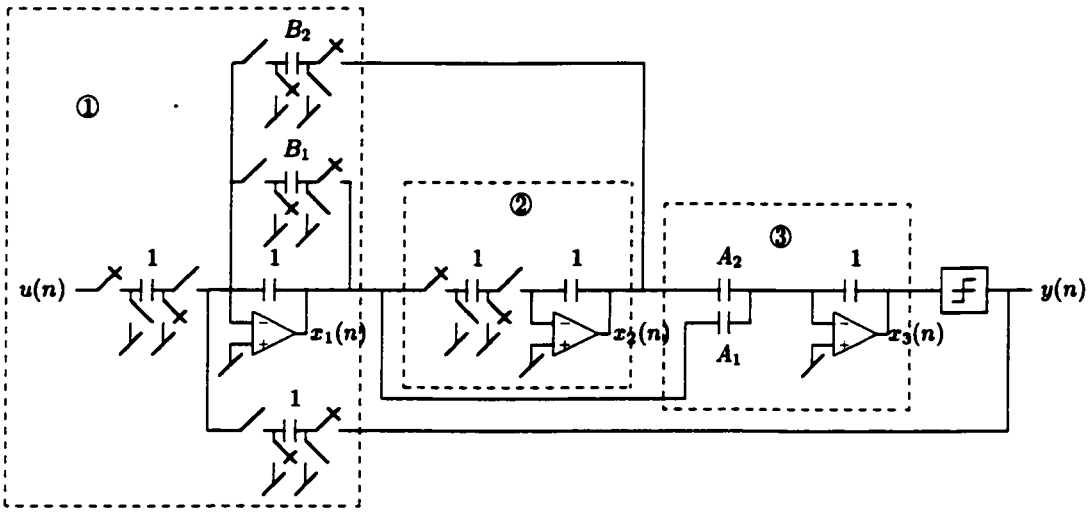

Figure 2.6: Corresponding SC Hardware Implementation of a 2-nd Order COI Σ-Δ A/D Converter

Table 2.1: Cascade-of-Integrator Nominal Capacitor Values

Capacitor	Value	Capacitor	Value	Capacitor	Value	Capacitor	Value
CB_1	B_1	CA_1	A_1	CX_1	1	CF_1	1
CB_2	B_2	CA_2	A_2	CX_2	1	CF_2	1
$\vdots$	$\vdots$	$\vdots$	$\vdots$	$\vdots$	$\vdots$	$\vdots$	$\vdots$
CB_N	B_N	CA_N	A_N	CX_{N+1}	1	CF_{N+1}	1

Applying the building blocks in Fig. 2.4 to a 6-th order COI A/D converter, one arrives at the SC hardware implementation shown in Fig. 2.7 where the nominal capacitor values are given in Table 2.1 [2]. In this way, $(N+1)$ operational amplifiers are required for the implementation of an N-th order COI Σ-Δ A/D converter.

2.2.2 Cascade-of-Resonators Σ-Δ A/D Converter Configuration

The cascade-of-resonators (COR) Σ-Δ A/D converter configuration shown in Fig. 2.8 first appeared in (Adams et. al., [16]), where it was used as a lowpass Σ-Δ A/D converter. This type of configuration is commonly referred to as an inverted configuration (due to the nature of the feedback path) and offers the advantage of no additional summing element (op-amp) which exists in the non-inverted COI Σ-Δ A/D converter [3]. This configuration was later successively employed for the realization of bandpass Σ-Δ A/D converters in (R. Schreier et. al., [10]) and subsequently in (W. M. Snelgrove et. al., [13]).

The COR Σ-Δ A/D converter configuration automatically places the zeros of $NTF(z)$ on the unit-circle in accordance with (Botteron et. al., [17])

$$N(z) = \prod_{k=1}^{\frac{N}{2}} \left[1 - (2 + R_k)z^{-1} + z^{-2}\right], \tag{2.20}$$

for even orders N and

$$N(z) = (1 - z^{-1}) \prod_{k=1}^{\lfloor \frac{N}{2} \rfloor} (1 - (2 + R_k)z^{-1} + z^{-2}) \tag{2.21}$$

for odd orders N. Evidently, the zeros of $NTF(z)$ depend on the values of multiplier coefficients R_k (for $k = 1, 2, \ldots, \lfloor \frac{N}{2} \rfloor$) only.

Further analysis of the COR Σ-Δ A/D converter configuration leads to the expressions for $S(z)$

[2] In the practical realisation of the SC hardware implementation, the capacitor values are scaled and will not directly correspond to the multiplier coefficients to be discussed in Chapter 3.

[3] This summing element also appears in the non-inverted CRI and FF Σ-Δ A/D configurations to be discussed later.

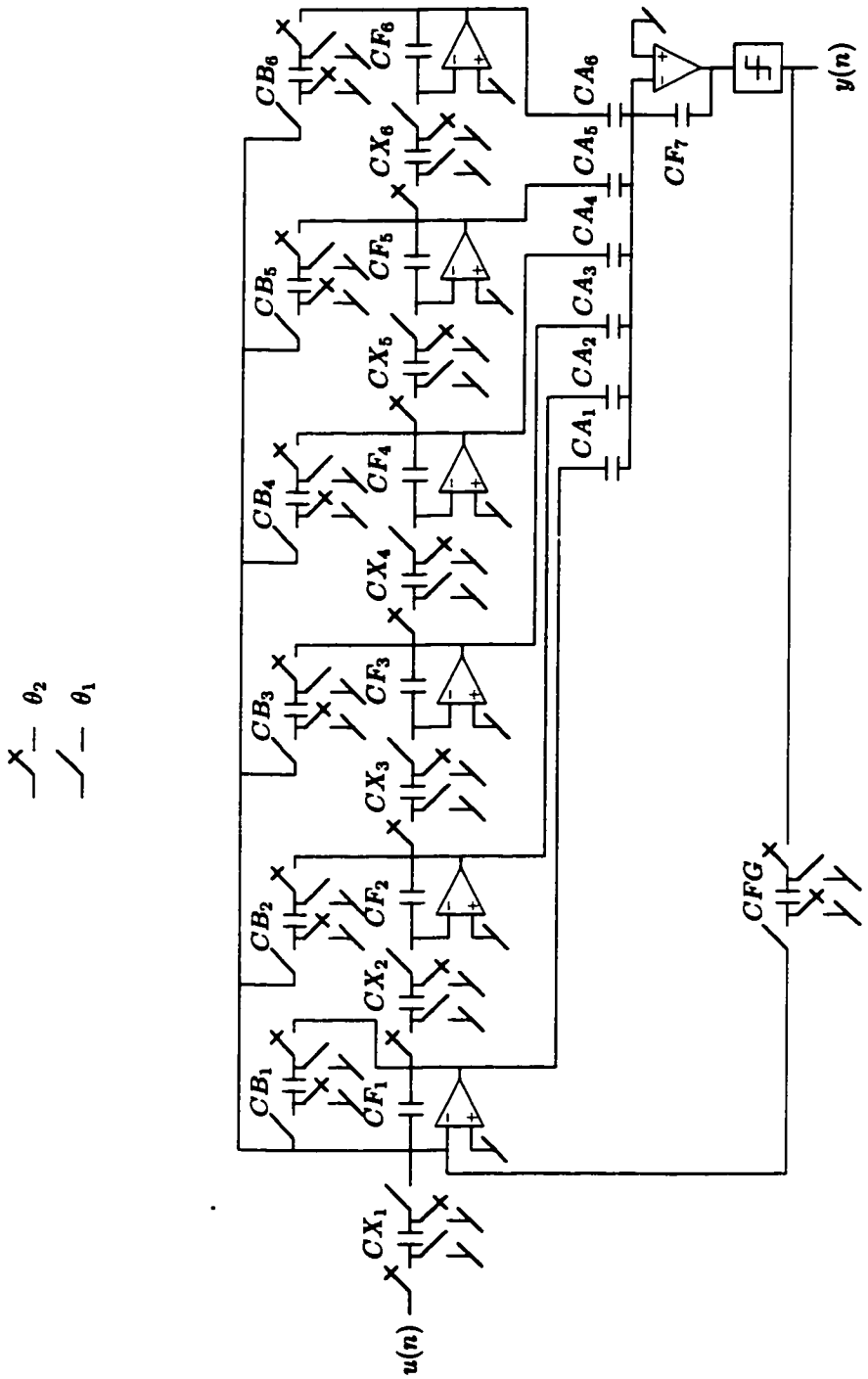

Figure 2.7: Cascade-of-Integrators SC Hardware Implementation

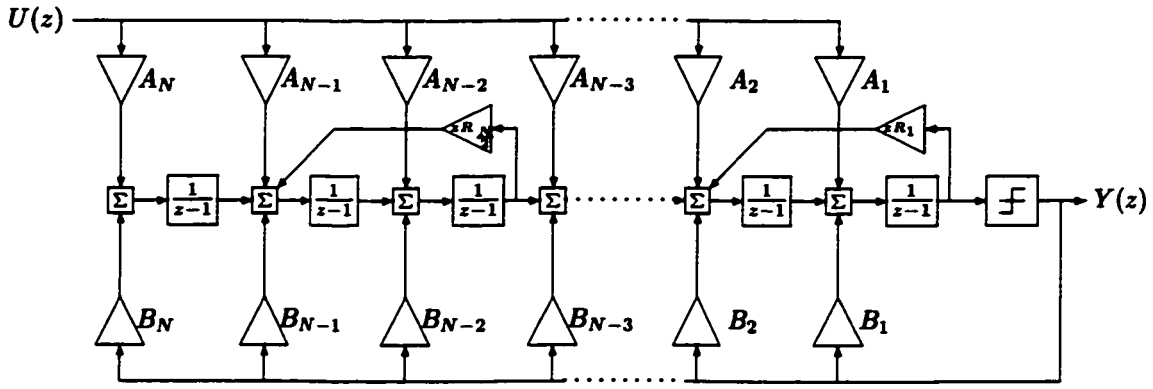

Figure 2.8: Cascade-of-Resonators Σ-Δ A/D Converter Configuration

and $D(z)$ as

$$S(z) = \sum_{i=1}^{\frac{N}{2}} (A_{2i-1}z + (-A_{2i-1} + A_{2i})) \prod_{j=i+1}^{\frac{N}{2}} (z^2 - (2 + R_j)z + 1), \tag{2.22}$$

$$D(z) = \prod_{i=1}^{\frac{N}{2}} (z^2 - (2 + R_i)z + 1) - \sum_{i=1}^{\frac{N}{2}} (B_{2i-1}z + (-B_{2i-1} + B_{2i})) \prod_{j=i+1}^{\frac{N}{2}} (z^2 - (2 + R_j)z + 1). \tag{2.23}$$

for even orders N, and

$$S(z) = \sum_{i=0}^{\lfloor \frac{N}{2} \rfloor} A_{2i+1} \left(z^2 - 2z + 1\right) \prod_{j=i+2}^{\lfloor \frac{N}{2} \rfloor} (z^2 - (2 + R_j)z + 1) + \sum_{i=1}^{\lfloor \frac{N}{2} \rfloor} A_{2i} (z - 1) \prod_{j=i+1}^{\lfloor \frac{N}{2} \rfloor} (z^2 - (2 + R_j)z + 1), \tag{2.24}$$

$$D(z) = N(z) - \left[\sum_{i=0}^{\lfloor \frac{N}{2} \rfloor} B_{2i+1} \left(z^2 - 2z + 1\right) \prod_{j=i+2}^{\lfloor \frac{N}{2} \rfloor} (z^2 - (2 + R_j)z + 1) + \sum_{i=1}^{\lfloor \frac{N}{2} \rfloor} B_{2i} (z - 1) \prod_{j=i+1}^{\lfloor \frac{N}{2} \rfloor} (z^2 - (2 + R_j)z + 1) \right] \tag{2.25}$$

for odd orders N. From Eqns. 2.20, 2.22, and 2.23 (and Eqns. 2.21, 2.24, and 2.25), the signal and noise transfer functions can be forced to be complementary by ensuring that the A_{1-N} and B_{1-N} multiplier values are pairwise equal.

As was the case for the COI Σ-Δ A/D converter configuration, one must be able to determine the R, A and B multiplier values given desired signal and/or noise transfer functions. The R multiplier values may be determined from the frequencies of the noise transfer function zeros f_0 in accordance

with

$$R_k = 2cos\left(2\pi\frac{f_0}{f_s}\right) - 2 \quad \text{for} \quad k = 0 \quad \text{to} \quad \left\lfloor\frac{N}{2}\right\rfloor, \tag{2.26}$$

where f_s represents the sampling frequency. The multiplier values A_{1-N} and B_{1-N} can be determined in accordance with

$$\mathcal{A}^T = \mathcal{C}_{1COR}^{-1}\mathcal{S}, \tag{2.27}$$

$$\mathcal{B}^T = \mathcal{C}_{2COR}^{-1}\mathcal{D}, \tag{2.28}$$

where $\mathcal{A} = [0, A_1, A_2, \cdots, A_N]$, where $\mathcal{B} = [1, B_1, B_2, \cdots, B_N]$ and where $\mathcal{C}_{1COR}$ and $\mathcal{C}_{2COR}$ are $(N+1) \times (N+1)$ matrices as discussed in the following.

The following expression can be derived for the numerator of the signal transfer function $S(z)$,

$$S(z) = KM \tag{2.29}$$

where $K = [A_1\ A_2 \cdots A_N]$, and where M is a column vector with N rows in accordance with

$$M = \frac{1}{z^N}\begin{bmatrix} (z-1)\prod_{i=N/2}^{2}(z-1)^2 - (z-1)R_i - Ri \\ \prod_{i=N/2}^{2}(z-1)^2 - (z-1)R_i - Ri \\ \vdots \\ (z-1)[(z-1)^2 - (z-1)R_{N/2} - R_{N/2}] \\ (z-1)^2 - (z-1)R_{N/2} - R_{N/2} \\ (z-1) \\ 1 \end{bmatrix}. \tag{2.30}$$

Then, by factoring out the z coefficients from M to form $\tilde{M}$ in accordance with

$$\tilde{M} = \mathcal{Z}^T M, \tag{2.31}$$

the matrix $\mathcal{C}_{1COR}$ can be expressed in terms of $\tilde{M}$ as

$$\mathcal{C}_{1COR} = \begin{bmatrix} 0 & 0 \\ 0 & \tilde{M} \end{bmatrix} \tag{2.32}$$

For example, by considering the case of $N = 4$, the matrix $\mathcal{C}_{1COR}$ is obtained as

$$\mathcal{C}_{1COR} = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 & 0 \\ 0 & -(3+R_2) & 1 & 0 & 0 \\ 0 & (3+R_2) & -(R_2+2) & 1 & 0 \\ 0 & -1 & 1 & -1 & 1 \end{bmatrix}. \tag{2.33}$$

Similarly, the matrix C_{2COR} can be expressed in terms of $\tilde{M}$ in accordance with

$$C_{2COR} = \begin{bmatrix} & \vdots & 0 \\ \mathcal{L} & \vdots & -\tilde{M} \end{bmatrix} \tag{2.34}$$

where $\mathcal{L}$ is a column vector with $(N+1)$ rows determined from

$$L(z) = \mathcal{Z}^T \mathcal{L}, \tag{2.35}$$

where

$$L(z) = \prod_{i=1}^{N/2} \left[1 - (2 + R_i)z^{-1} + z^{-2}\right]. \tag{2.36}$$

For example, the matrix C_{2COR} is given by

$$C_{2COR} = \begin{bmatrix} 1 & 0 & 0 & 0 & 0 \\ -4 - R_1 - R_2 & -1 & 0 & 0 & 0 \\ 6 + 2R_1 + 2R_2 + R_1R_2 & 3 + R_2 & -1 & 0 & 0 \\ -4 - R_1 - R_2 & -(3 + R_2) & 2 + R_2 & -1 & 0 \\ 1 & 1 & -1 & 1 & -1 \end{bmatrix} \tag{2.37}$$

for the case of $N = 4$. Evidently, the matrices C_{1COR} and C_{2COR} are lower triangular matrices having elements independent of the A and B multiplier values.

The practical implementation of the COR Σ-Δ A/D converter configuration involves its SC hardware realization. By inspection of the COR A/D converter configuration, one may note that it is composed of summing elements (having inputs weighted by constants or constants and unit-advance term z) followed by integrators. Therefore, the SC hardware implementation may be determined by applying the building blocks in Fig. 2.4 to obtain the SC circuit shown in Fig. 2.9, where the capacitor values are determined in accordance with Table 2.2. One may note that only N operational amplifiers are required to implement an N-th order COR A/D converter.

2.2.3 Cascade-of-Resonators/Integrators Σ-Δ A/D Converter Configuration

The cascade-of-resonators/integrators (CRI) Σ-Δ A/D converter configuration in Fig. 2.10 was developed in (Botteron et. al., [17]) and combines the salient practical features of the COR and CRI Σ-Δ A/D converter configurations, namely it ensures that the signal and noise transfer functions $STF(z)$ and $NTF(z)$ are made complementary by the A/D converter configuration proper, and that the zeros of $NTF(z)$ are automatically placed on the unit-circle, again by the configuration proper itself. This is a non-inverted configuration and thus requires an additional summing element.

The polynomials $N(z)$, $S(z)$, and $D(z)$ may be formed in terms of the multiplier coefficients

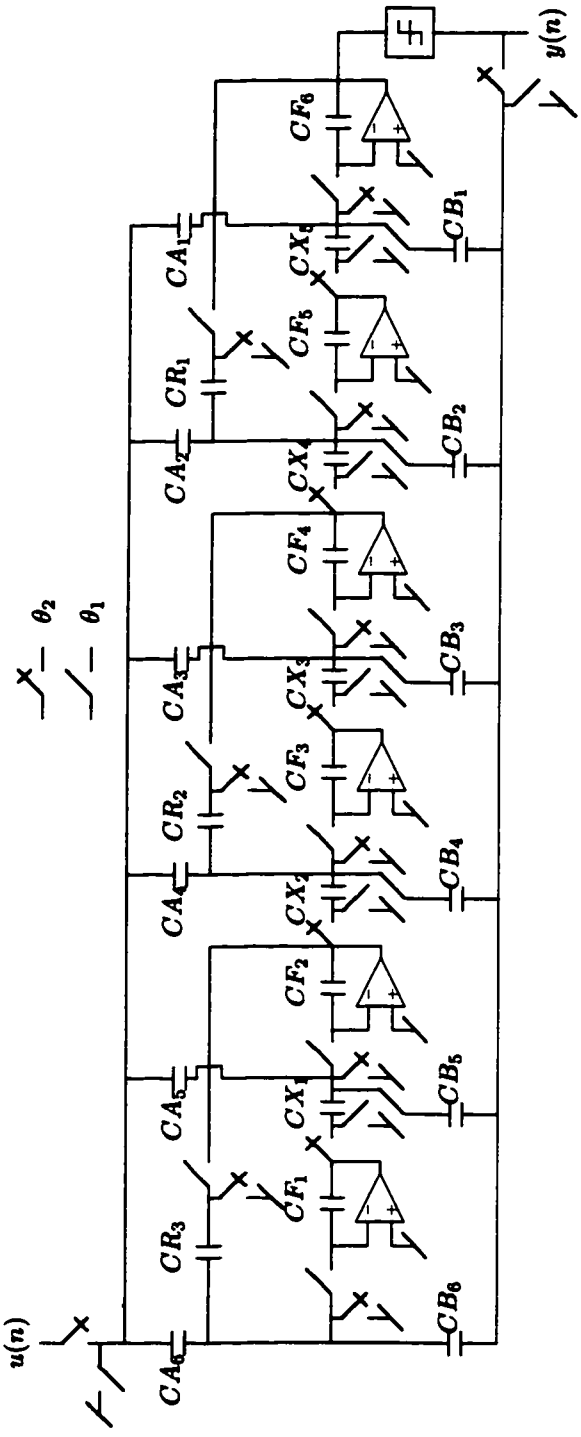

Figure 2.9: Cascade-of-Resonators SC Hardware Implementation

Table 2.2: Cascade-of-Resonators Nominal Capacitor Values

Capacitor	Value	Capacitor	Value	Capacitor	Value
CB_1	B_1	CA_1	A_1	CX_1	1
CB_2	B_2	CA_2	A_2	CX_2	1
$\vdots$	$\vdots$	$\vdots$	$\vdots$	$\vdots$	$\vdots$
CB_N	B_N	CA_N	A_N	CX_{N+1}	1
CF_1	1	CR_1	$-R_1$		
CF_2	1	CR_2	$-R_2$		
$\vdots$	$\vdots$	$\vdots$	$\vdots$		
CF_{N+1}	1	$CR_{\frac{N}{2}}$	$-R_{\frac{N}{2}}$		

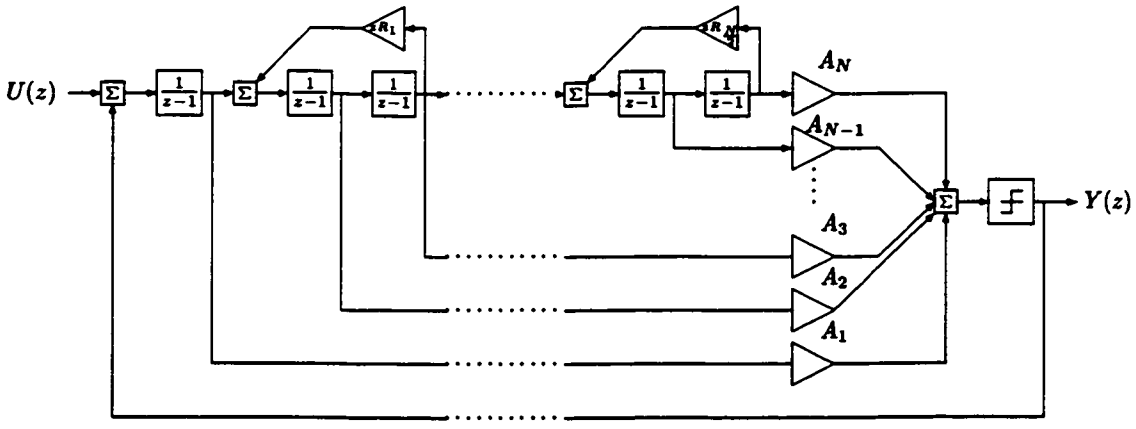

Figure 2.10: Cascade-of-Resonators/Integrators Σ-Δ A/D Converter Configuration

A_{1-N}, B_{1-N}, and $R_{1-\lfloor N/2 \rfloor}$ in accordance with

$$N(z) = \prod_{i=1}^{\frac{N}{2}} (z^2 - (2 + R_i)z + 1), \tag{2.38}$$

$$S(z) = \sum_{i=1}^{\frac{N}{2}} (A_{2i-1}z + (-A_{2i-1} + A_{2i})) \prod_{j=i+1}^{\frac{N}{2}} (z^2 - (R_j + 2)z + 1), \tag{2.39}$$

$$D(z) = N(z) - S(z), \tag{2.40}$$

for an even order N, and in accordance with

$$N(z) = (z - 1) \prod_{i=1}^{\lfloor \frac{N}{2} \rfloor} (z^2 - (2 + R_i)z + 1), \tag{2.41}$$

$$S(z) = A_1 \prod_{i=1}^{\lfloor \frac{N}{2} \rfloor} (z^2 - (2 + R_i)z + 1) + \sum_{i=1}^{\lfloor \frac{N}{2} \rfloor} (A_{2i}z + (-A_{2i} + A_{2i+1})) \prod_{j=i+1}^{\lfloor \frac{N}{2} \rfloor} (z^2 - (R_j + 2)z + 1), \tag{2.42}$$

$$D(z) = N(z) - S(z). \tag{2.43}$$

for an odd order N.

The multiplier coefficients of the CRI Σ-Δ A/D converter configuration may be determined based on a given signal and noise transfer function as discussed in the following.

The determination of the $R_{1-\lfloor N/2 \rfloor}$ multiplier coefficients may be achieved by employing Eqn. 2.26. Furthermore, it can be shown that the multiplier coefficients A_{1-N} may be determined in accordance with

$$\mathcal{A}^T = \mathcal{C}_{CRI}^{-1} \mathcal{S} \tag{2.44}$$

where $\mathcal{A} = [0, A_1, A_2, \cdots, A_N]$, and where $\mathcal{C}_{CRI}$ is a $(N + 1)$ by $(N + 1)$ matrix. Furthermore, it can be shown that $\mathcal{C}_{CRI} = \mathcal{C}_{1COR}$. As a result $\mathcal{C}_{CRI}$ is a lower triangular matrix of order $(N + 1)$ with unity diagonal elements and off diagonal elements independent of the multiplier coefficients $\mathcal{A}$. For example, the matrix $\mathcal{C}_{CRI}$ for the case of $N = 4$ is given by

$$\mathcal{C}_{CRI} = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 & 0 \\ 0 & -(3 + R_2) & 1 & 0 & 0 \\ 0 & (3 + R_2) & -(R_2 + 2) & 1 & 0 \\ 0 & -1 & 1 & -1 & 1 \end{bmatrix} \tag{2.45}$$

The CRI Σ-Δ is composed of both summing elements followed by integrators and summing elements. Employing the building blocks shown in Fig. 2.4 for a 6-th order CRI A/D converter

Table 2.3: Cascade-of-Resonators-Integrator Nominal Capacitor Values

Capacitor	Value	Capacitor	Value	Capacitor	Value	Capacitor	Value
CA_1	A_1	CX_1	1	CF_1	1	CR_1	$-R_1$
CA_2	A_2	CX_2	1	CF_2	1	CR_2	$-R_2$
$\vdots$	$\vdots$	$\vdots$	$\vdots$	$\vdots$	$\vdots$	$\vdots$	$\vdots$
CA_N	A_N	CX_{N+1}	1	CF_{N+1}	1	$CR_{\frac{N}{2}}$	$-R_{\frac{N}{2}}$

configuration, one may arrive at the SC hardware implementation shown in Fig. 2.11, where the nominal capacitor values are determined in accordance with Table 2.3. One may note that $(N+1)$ operational amplifiers are required to implement an N-th order CRI A/D converter.

2.2.4 Feedforward Σ-Δ A/D Converter Configuration

The feedforward (FF) Σ-Δ A/D converter was presented in (Norsworthy et. al., [5]) and is as shown in Fig. 2.12. The FF Σ-Δ A/D converter is a non-inverted configuration and thus requires an additional summing element. This configuration is identical to the CRI Σ-Δ A/D converter configuration with the exception that the R multiplier coefficients are not multiplied by a unit-advance term z. For an even-order N, the numerator of the noise transfer function can be expressed in terms of the R multiplier coefficients in accordance with

$$N(z) = \prod_{k=1}^{\frac{N}{2}} [1 - 2z^{-1} + (1 - R_k)z^{-2}], \tag{2.46}$$

and for an odd order N, in accordance with

$$N(z) = (1 - z^{-1}) \prod_{k=1}^{\frac{N}{2}} [1 - 2z^{-1} + (1 - R_k)z^{-2}]. \tag{2.47}$$

Evidently, the zeros of $N(z)$ are guaranteed to be located on the line $Re(z) = 1$ by the configuration proper. The numerator $S(z)$ of the signal transfer function can be written in terms of the multiplier coefficients A_{1-N} in accordance with

$$S(z) = \sum_{i=1}^{\frac{N}{2}} [A_{2i-1}z + (-A_{2i-1} + A_{2i})] \prod_{j=i+1}^{\frac{N}{2}} [z^2 - 2z + (1 - R_j)]. \tag{2.48}$$

for even orders N, and in accordance with

$$S(z) = A_1 \prod_{i=1}^{\lfloor \frac{N}{2} \rfloor} (z^2 - 2z + (1 - R_i)) + \sum_{i=1}^{\lfloor \frac{N}{2} \rfloor} (A_{2i}z + (-A_{2i} + A_{2i+1})) \tag{2.49}$$

$$\prod_{j=i+1}^{\lfloor \frac{N}{2} \rfloor} (z^2 - 2z + (1 - R_j)), \tag{2.50}$$

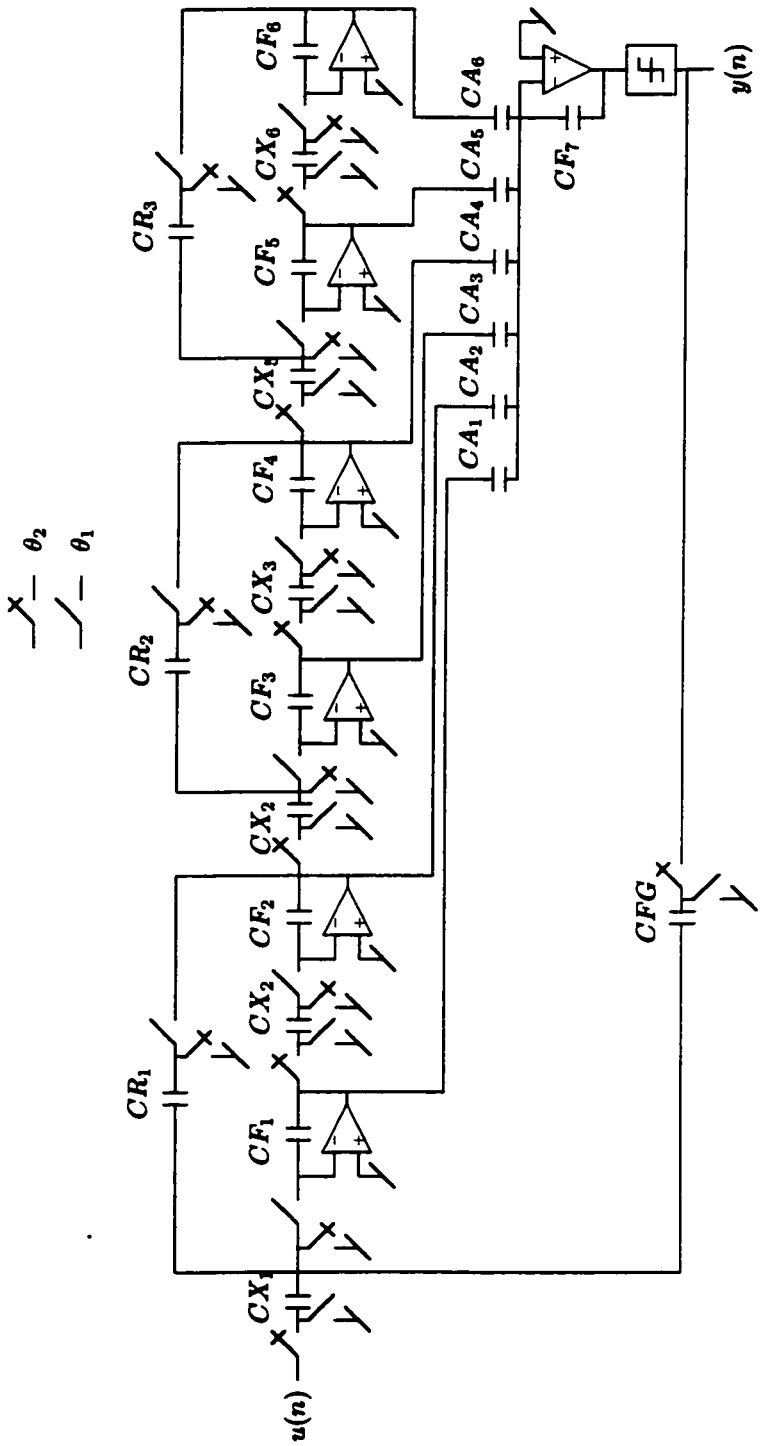

Figure 2.11: Cascade-of-Resonators/Integrators SC Hardware Implementation

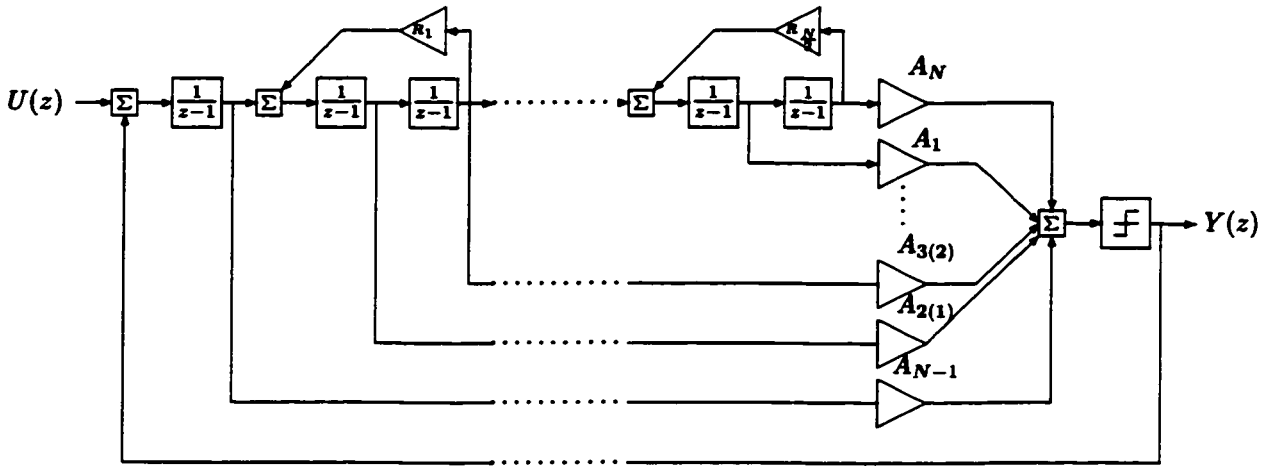

Figure 2.12: Feedforward Σ-Δ A/D Converter Configuration

for odd orders N. Moreover, the denominator $D(z)$ of the signal and noise transfer functions can be determined in accordance with Eqn. 2.5. As a result, the FF Σ-Δ A/D converter configuration proper guarantees the complementarity of the signal and noise transfer functions.

Given a signal or noise transfer function, the multiplier coefficients R_k (for $k = 0$ to $\lfloor N/2 \rfloor$) and A_{1-N} may be determined as discussed in the following.

The R_k multiplier coefficients may be expressed in terms of the angles of the zeros θ_k of $NTF(z)$ in accordance with

$$R_k = tan^2(\theta_k). \tag{2.51}$$

Moreover, through a detailed analysis of the FF Σ-Δ A/D converter configuration, it can be shown that if $\mathcal{A} = [0, A_1, A_2, \cdots, A_N]$, then $\mathcal{S} = C_{FF}\mathcal{A}^T$. To determine C_{FF}, let the numerator $S(z)$ of the signal transfer function be given by

$$S(z) = KM \tag{2.52}$$

where $K = [A_1\ A_2 \cdots A_N]$, and where M is a certain column vector with N rows. First, let us define M in accordance with

$$M = \frac{1}{z^N} \begin{bmatrix} (z-1)\prod_{i=N/2}^{2}(z^2 - 2z + (1 - R_i)) \\ \prod_{i=N/2}^{2}(z^2 - 2z + (1 - R_i)) \\ \vdots \\ (z-1)(z^2 - 2z + (1 - R_{N/2})) \\ z^2 - 2z + (1 - R_{N/2}) \\ (z-1) \\ 1 \end{bmatrix} \tag{2.53}$$

Table 2.4: Feedforward Nominal Capacitor Values

Capacitor	Value	Capacitor	Value	Capacitor	Value	Capacitor	Value
CA_1	A_1	CX_1	1	CF_1	1	CR_1	R_1
CA_2	A_2	CX_2	1	CF_2	1	CR_2	R_2
$\vdots$	$\vdots$	$\vdots$	$\vdots$	$\vdots$	$\vdots$	$\vdots$	$\vdots$
CA_N	A_N	CX_{N+1}	1	CF_{N+1}	1	$CR_{\frac{N}{2}}$	$R_{\frac{N}{2}}$

Then, by factoring out the z coefficients from M to form $\tilde{M}$

$$\tilde{M} = \mathcal{Z}^T M, \tag{2.54}$$

it is possible to form the matrix C_{FF} in terms of the matrix $\tilde{M}$ in accordance with

$$C_{FF} = \begin{bmatrix} 0 & 0 \\ 0 & \tilde{M} \end{bmatrix} \tag{2.55}$$

For example, in the case of $N = 4$, one has

$$C_{FF} = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 & 0 \\ 0 & -3 & 1 & 0 & 0 \\ 0 & 3 - R_2 & -2 & 1 & 0 \\ 0 & -1 + R_1 & 1 - R_2 & -1 & 1 \end{bmatrix}. \tag{2.56}$$

Evidently, C_{FF} is a lower triangular matrix of order $(N + 1)$ having unity as its diagonal elements, and having its off-diagonal elements as being independent of the multiplier coefficients A_{1-N} [4].

The similarity between the CRI and FF Σ-Δ A/D converter configurations aids in the determination of the corresponding SC hardware implementation of the FF A/D converter. Due to the absence of the unit-advance terms z multiplying the R_k coefficients, the phasing of the corresponding switches reverses resulting in the SC hardware implementation shown in Fig. 2.13 for a 6-th order converter configuration. The nominal capacitor values are given in Table 2.4. One may note that $(N + 1)$ operational amplifiers are required to implement an N-th order FF Σ-Δ A/D converter.

2.2.5 Multiple-Feedback Σ-Δ A/D Converter Configuration

The multiple-feedback (MF) Σ-Δ A/D converter configuration in Fig. 2.14 was presented in (Norsworthy et. al., [5]) and is an inverted configuration (not requiring an additional summing element). The polynomial $N(z)$ may be expressed in terms of the coefficients R_k (for $k = 0$ to $\lfloor N/2 \rfloor$) in

[4] The off-diagonal elements depend solely on the multiplier coefficients R_k.

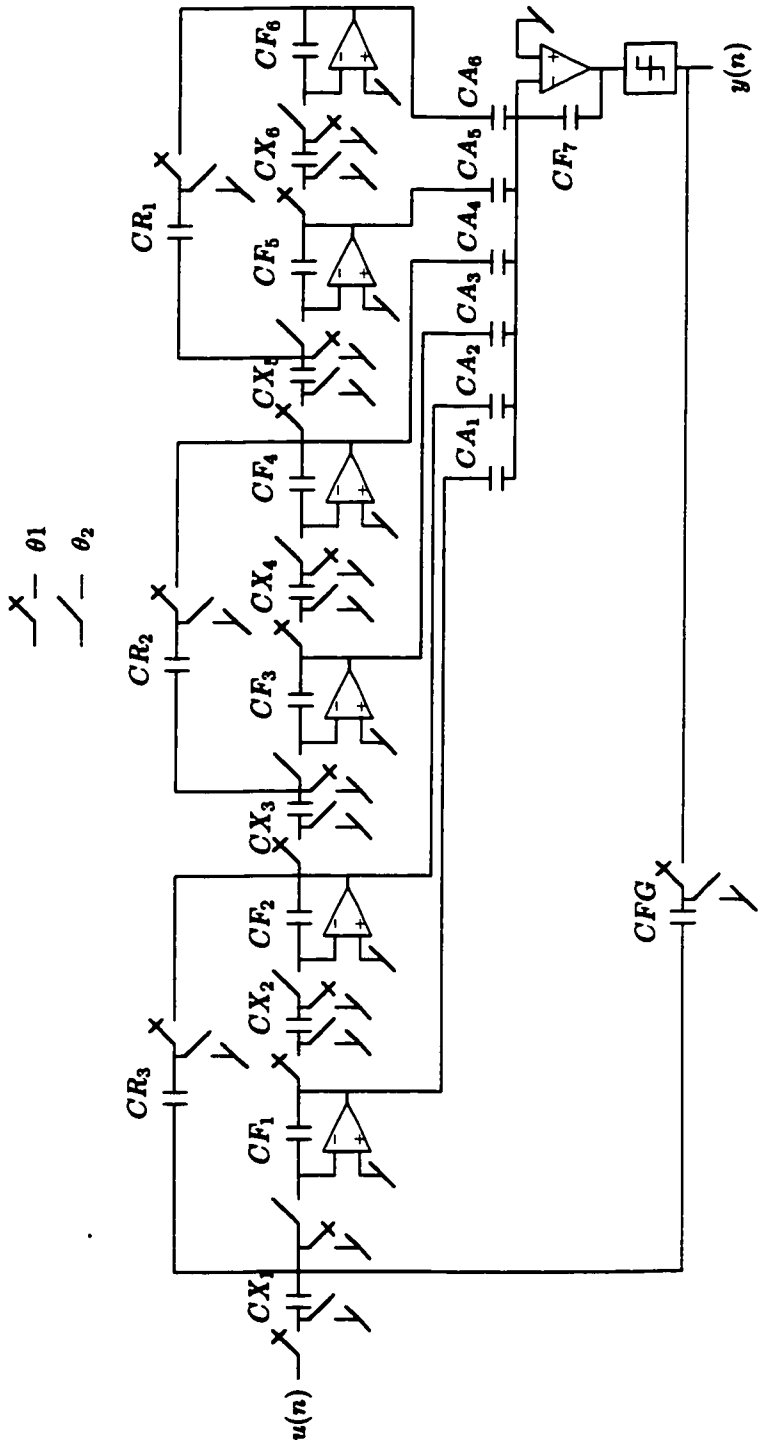

Figure 2.13: Feedforward SC Hardware Implementation

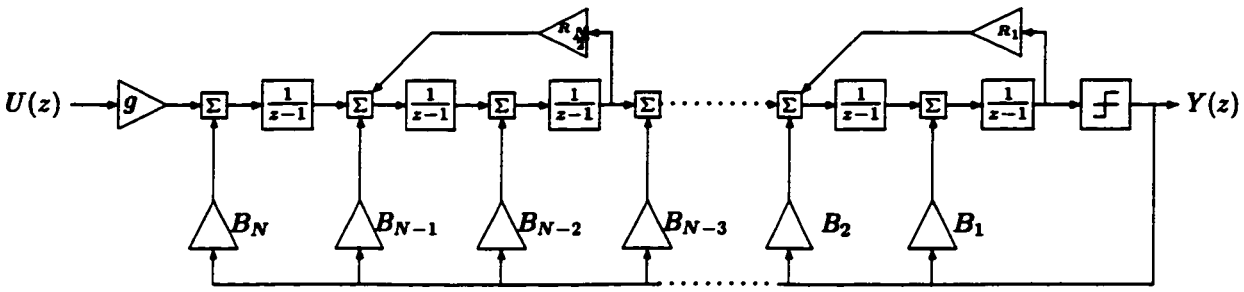

Figure 2.14: Multiple-Feedback Σ-Δ A/D Converter Configuration

accordance with

$$N(z) = \prod_{k=1}^{\frac{N}{2}} [1 - 2z^{-1} + (1 - R_k)z^{-2}] \tag{2.57}$$

for even orders N, and in accordance with

$$N(z) = (1 - z^{-1}) \prod_{k=1}^{\frac{N}{2}} [1 - 2z^{-1} + (1 - R_k)z^{-2}] \tag{2.58}$$

for odd orders N. As a result, the zeros of $N(z)$ are guaranteed to be located on the line $Re(z) = 1$ by the configuration proper. Further analysis of the MF A/D converter configuration leads to

$$S(z) = gz^{-N}, \tag{2.59}$$

and

$$D(z) = \prod_{i=1}^{\frac{N}{2}} [1 - 2z^{-1} + (1 - R_i)z^{-2}] + \tag{2.60}$$

$$\sum_{i=1}^{\frac{N}{2}} [B_{2i-1}z^{-2i+1} + (-B_{2i-1} + B_{2i})z^{-2i}] \prod_{j=i+1}^{\frac{N}{2}} [1 - 2z^{-1} + (1 - R_i)z^{-2}] \tag{2.61}$$

for even orders N and

$$D(z) = N(z) - \left[\sum_{i=0}^{\lfloor \frac{N}{2} \rfloor} B_{2i+1} \left(z^2 - 2z + 1\right) \prod_{j=i+2}^{\lfloor \frac{N}{2} \rfloor} (z^2 - 2z + (1 - R_j)) \right.$$

$$\left. + \sum_{i=1}^{\lfloor \frac{N}{2} \rfloor} B_{2i} (z - 1) \prod_{j=i+1}^{\lfloor \frac{N}{2} \rfloor} (z^2 - 2z + (1 - R_j)) \right] \tag{2.62}$$

for odd orders N. This configuration cannot be designed to have complementary signal and noise transfer functions $STF(z)$ and $NTF(z)$.

Starting from given signal and noise transfer functions, the multiplier coefficients g, R_k for $k = 0$ to $\lfloor N/2 \rfloor$, and B_{1-N} may be determined as discussed in the following.

The gain element of value g is placed at the signal input to the A/D converter to reduce the signal transfer function passband gain to (approximately) unity, where

$$g = |STF(e^{jw})|^{-1}\big|_{w=w_p}, \tag{2.63}$$

where w_p is a representative frequency in the input signal passband[5]. The R_k multiplier coefficients may be expressed in terms of the angles of the zeros θ_k of $NTF(z)$ in accordance with

$$R_k = tan^2(\theta_k). \tag{2.64}$$

Moreover, through a detailed analysis of the MF Σ-Δ A/D converter configuration it can be shown that if $\mathcal{B} = [1, B_1, B_2, \cdots, B_N]$, then

$$\mathcal{B}^T = \mathcal{C}_{MF}^{-1}\mathcal{D} \tag{2.65}$$

where $\mathcal{C}_{MF}$ is a matrix of order $(N+1)$ determined as described in the following.

First, let us express the denominator $D(z)$ of the signal and noise transfer functions as

$$D(z) = \mathcal{B}M \tag{2.66}$$

where M is a certain column vector with $(N+1)$ rows. Then, let M be defined in accordance with

$$M = \frac{1}{z^N}\begin{bmatrix} \prod_{i=1}^{N/2}(z^2 - 2z + (1 - R_i)) \\ -(z-1)^{N-1} \\ \vdots \\ -(z-1)^3 \\ -(z-1)^2 \\ -(z-1) \\ -1 \end{bmatrix} \tag{2.67}$$

In this way, by factoring out the z coefficients from M, one forms

$$\tilde{M} = \mathcal{Z}^T M, \tag{2.68}$$

leading to the determination of the matrix $\mathcal{C}_{MF}$ as

$$\mathcal{C}_{MF} = \tilde{M}. \tag{2.69}$$

As an example, for the case of $N = 4$, the matrix $\mathcal{C}_{MF}$ is given as

$$\mathcal{C}_{MF} = \begin{bmatrix} 1 & 0 & 0 & 0 & 0 \\ -4 & -1 & 0 & 0 & 0 \\ 6 - R_1 - R_2 & 3 & -1 & 0 & 0 \\ -4 - 2R_1 - 2R_2 & -3 + R_2 & 2 & -1 & 0 \\ 1 + R_1R_2 - R_1 - R_2 & 1 - R_2 & -1 + R_2 & 1 & -1 \end{bmatrix}. \tag{2.70}$$

[5]Since the gain in the input signal passband is almost constant, any frequency in the passband should serve the purpose.

Table 2.5: Multiple-Feedback Nominal Capacitor Values

Capacitor	Value	Capacitor	Value	Capacitor	Value	Capacitor	Value
CB_1	B_1	CX_1	1	CF_1	1	CR_1	R_1
CB_2	B_2	CX_2	1	CF_2	1	CR_2	R_2
$\vdots$	$\vdots$	$\vdots$	$\vdots$	$\vdots$	$\vdots$	$\vdots$	$\vdots$
CB_N	B_N	CX_{N+1}	1	CF_{N+1}	1	$CR_{\frac{N}{2}}$	$R_{\frac{N}{2}}$

Evidently, the matrix C_{MF} is a lower triangular matrix having unity as its first diagonal element and -1 as its remaining diagonal elements, and having its off-diagonal elements as being independent of the multiplier coefficients B_k.

Inspection of the MF Σ-Δ A/D converter configuration reveals that it is composed of summing elements followed by integrators. Using the corresponding SC hardware building blocks shown in Fig. 2.4 one arrives at the SC hardware implementation shown in Fig. 2.15 for the case of $N = 6$. The nominal capacitor values are given in Table 2.5. One may note that only N operational amplifiers are required to implement an N-th order MF A/D converter.

2.2.6 Concluding Remarks

This chapter has been concerned with the characterization and practical realization of five widely used feedforward and multiple-feedback Σ-Δ A/D converter configurations. It was shown that, in so far as the complementarity of the signal and noise transfer functions is concerned, one can distinguish between three different cases, namely, a) the converter configuration proper guarantees the complementarity of the signal and noise transfer functions (COI,CRI,FF), b) the complementarity of $STF(z)$ and $NTF(z)$ is no longer guaranteed by the Σ-Δ A/D converter configuration proper, but it can be forced through a judicious choice of parameters for the A/D converter as obtained by numerical optimization (COR), and c) the complementarity of $STF(z)$ and $NTF(z)$ is neither guaranteed by the Σ-Δ A/D converter configuration proper nor can it be forced through numerical optimization (MF). Furthermore, it was shown that three cases exist as far as the location of the noise transfer function zeros are concerned, namely, a) the noise transfer function zeros are guaranteed to be on the unit-circle by the configuration proper (COR,CRI), b) the noise transfer function zeros are not guaranteed to be on the unit-circle but may be placed there through a judicious choice of parameters for the A/D converter as obtained by numerical optimization (COI), and c) the noise transfer function zeros are guaranteed to be on the line $Re(z) = 1$ by the configuration proper (FF,MF).

A detailed procedure was given to determine the parameters of each Σ-Δ A/D converter configuration given a signal and/or a noise transfer function.

Finally, the SC hardware implementation of each A/D converter configuration was presented

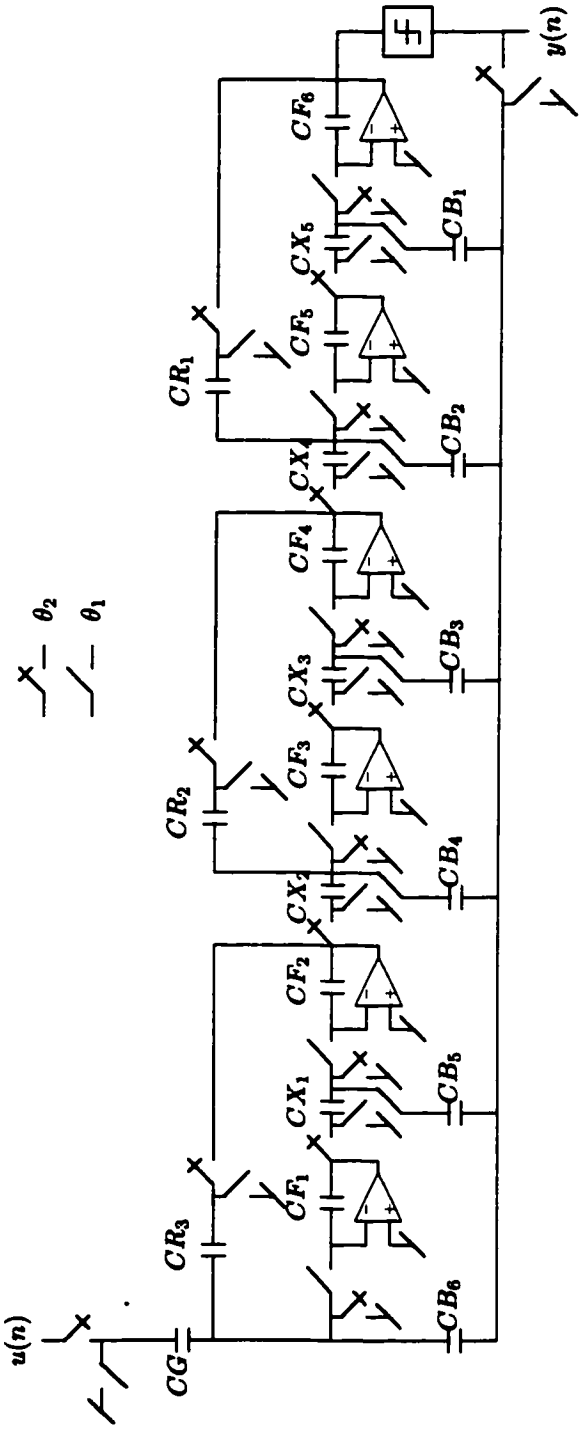

Figure 2.15: Multiple-Feedback SC Hardware Implementation

along with their corresponding nominal capacitor values. It was shown that the non-inverted configurations (COI, CRI, and FF) required an additional operational amplifier as compared to the inverted configurations (COR and MF).

The next chapter is concerned with the design and empirical analysis and investigation of each of the above five Σ-Δ A/D converter configurations in order to determine the significance of the complementarity of the signal and noise transfer functions and the location of the noise transfer function zeros on their achievable $SQNR$ and DR. This will then be followed by an investigation of the $SQNR$ and DR performance in the presence of capacitor tolerances in corresponding switched-capacitor hardware implementations.

Chapter 3

Design of Feedforward and Multiple-Feedback Σ-Δ A/D Converter Configurations

3.1 Introduction

The previous chapter was concerned with the characterization of five different practical feedforward and multiple-feedback Σ-Δ A/D converters in terms of two important features, namely, a) the location of their constituent noise transfer function zeros with respect to the unit-circle in the complex z-plane, and b) the complementarity (or lack thereof) of their constituent signal and noise transfer functions. This chapter, on the other hand, is concerned with the design and empirical analysis and investigation of each of the five Σ-Δ A/D converter configurations in order to determine the significance of the aforementioned features on their achievable signal-to-quantization-noise ratio ($SQNR$) and their dynamic range (DR). This is followed by an investigation of the $SQNR$ and DR performance in the presence of capacitor mismatches in corresponding switched-capacitor hardware implementations.

Section 3.2 is concerned with the approximation of the signal and noise transfer functions from a set of high-level system design specifications. Section 3.3 presents a hitherto statistical technique to estimate the maximum DC input signal for stable Σ-Δ A/D converter operation. This statistical technique is based on several assumptions, the most restricting of which is that the quantizer input signal is Gaussian distributed. Section 3.4 is concerned with the design and simulation of each of the five hitherto Σ-Δ A/D converters to determine the achievable $SQNR$ and DR. A Monte-Carlo analysis is also performed to determine the $SQNR$ and DR performance in the presence of capacitor mismatches. A novel statistical approach is then presented in Section 3.5 which generalizes the hitherto technique to the case of arbitrary quantizer input signal distributions. A demonstration of the accuracy of the proposed statistical approach is then presented in Section 3.6. Finally, the main conclusions of this chapter are given in Section 3.7.

Table 3.1: System Design Specifications

Sampling Frequency	f_s Hz
Signal Bandwidth	BW Hz
Signal Center Frequency	f_c Hz
$SQNR$	$SQNR$ dB
Order	N

3.2 Design Procedure

3.2.1 System Design Specifications

The design of feedforward and multiple-feedback Σ-Δ A/D converters starts from a set of high-level system design specifications. This set of design specifications includes the sampling frequency f_s, the signal bandwidth BW, the signal center frequency f_c, the desired $SQNR$ and the order N of the converter, as tabulated in Table 3.1. In the case of lowpass Σ-Δ A/D converter design, the bandlimiting frequency of the input signal f_b is used in place of the bandwidth BW and the signal center frequency f_c.

3.2.2 Approximation of Signal and Noise Transfer Functions

The approach to the design of Σ-Δ A/D converters as advocated in this thesis is first to obtain a noise transfer function $NTF(z)$ through conventional approximation, and then obtain a complementary signal transfer function $STF(z)$ by invoking Eqn. 2.6 (or from $S(z) = z^{-N}$ in the case of the MF Σ-Δ A/D converter configuration). In general, one must resort to a constrained optimization to approximate the noise transfer function $NTF(z)$ (except if a classical transfer function is used [1]) as discussed in the following (Fraser et. al., [18]). To develop this optimization, let us express the denominator of the signal and noise transfer function $D(z)$ in accordance with

$$D(z) = (1 - p_1 z^{-1})(1 - p_1^* z^{-1}) \cdots (1 - p_{\frac{N}{2}} z^{-1})(1 - p_{\frac{N}{2}}^* z^{-1}), \tag{3.1}$$

for the case of even order N, or

$$D(z) = (1 - p_1 z^{-1})(1 - p_1^* z^{-1}) \cdots (1 - p_{\frac{N}{2}} z^{-1})(1 - p_{\frac{N}{2}}^* z^{-1})(1 - r_k z^{-1}), \tag{3.2}$$

for the case of odd order N, where $p_k = r_k e^{jw_{pk}}$ represents the k-th complex pole, and where $*$ represents complex conjugation.

Moreover, in the case of the COR, COI, and CRI Σ-Δ A/D converters, let us express the numerator of the noise transfer function $N(z)$ in accordance with

$$N(z) = (1 - z_1 z^{-1})(1 - z_1^* z^{-1}) \cdots (1 - z_{\frac{N}{2}} z^{-1})(1 - z_{\frac{N}{2}}^* z^{-1}), \tag{3.3}$$

[1] e.g. Butterworth, Chebyshev, Elliptic

for the case of even order N, or

$$N(z) = (1 - z_1 z^{-1})(1 - z_1^* z^{-1}) \cdots (1 - z_{\frac{N}{2}} z^{-1})(1 - z_{\frac{N}{2}}^* z^{-1})(1 - z^{-1}), \tag{3.4}$$

for the case of odd order N, where $z_k = e^{jw_{zk}}$ represents the k-th zero. Otherwise, i.e. in the case of the FF and MF Σ-Δ A/D converters, express $N(z)$ as

$$N(z) = \prod_{k=1}^{\frac{N}{2}} [1 - 2z^{-1} + (1 - R_k)z^{-2}] \tag{3.5}$$

for the case of even order N, or

$$N(z) = (1 - z^{-1}) \prod_{k=1}^{\frac{N}{2}} [1 - 2z^{-1} + (1 - R_k)z^{-2}] \tag{3.6}$$

for the case of odd order N. The purpose of the optimization is to determine the noise transfer function subject to certain constraints on $|NTF(e^{jw})|$ (c.f. Eqns. 3.8 and 3.10 in the following). The variables of optimization include either, (a) the zero frequencies ω_{zk} and the pole radii r_k and pole frequencies ω_{pk}, or (b) the coefficients R_k and the pole radii r_k and pole frequencies ω_{pk}. The optimization constraints are determined as discussed in the following.

The $SQNR$ is determined by the amount of noise attenuation in the signal band. In (W. M. Snelgrove et. al., [13]) it was shown that the $SQNR$ may be determined from

$$SQNR = 20log_{10}\left(\frac{V_{in}}{V_{ref}}\right) - 10log_{10}\left(\frac{1}{3}\right) + 10log_{10}(OSR) - 20log_{10}(NTF_{in-band}), \tag{3.7}$$

where V_{in} is the maximum input signal level (usually chosen as $\frac{V_{ref}}{2}$, where V_{ref} is the quantizer output level, and $NTF_{in-band}$ refers to the in-band noise (assumed to be constant). In this way, the desired $SQNR$ may be obtained by constraining the noise gain in the signal band to be below $NTF_{in-band}$,

$$|NTF(e^{j2\pi f})|_{f_c - BW/2 \le f \le f_c + BW/2} < NTF_{in-band}. \tag{3.8}$$

It has been shown in (Lee, [12]) that a good rule of thumb is to ensure that the magnitude of the noise transfer function is constrained by

$$|NTF(e^{jw})| \le 2 \tag{3.9}$$

throughout the whole frequency band (so as to reduce the likelihood of the Σ-Δ A/D converter becoming unstable). It was further demonstrated in (W. M. Snelgrove et. al. [13]) that

$$|NTF(e^{jw})| \le 1.6 \quad (4.1\ dB) \tag{3.10}$$

leads to better stability results. In this thesis, $|NTF(e^{jw})|$ is constrained in accordance with Eqn. 3.10 since it provides a more stable converter operation. One may also constrain the zeros of $NTF(z)$ to stay within the input signal band so as to limit the optimization search space,

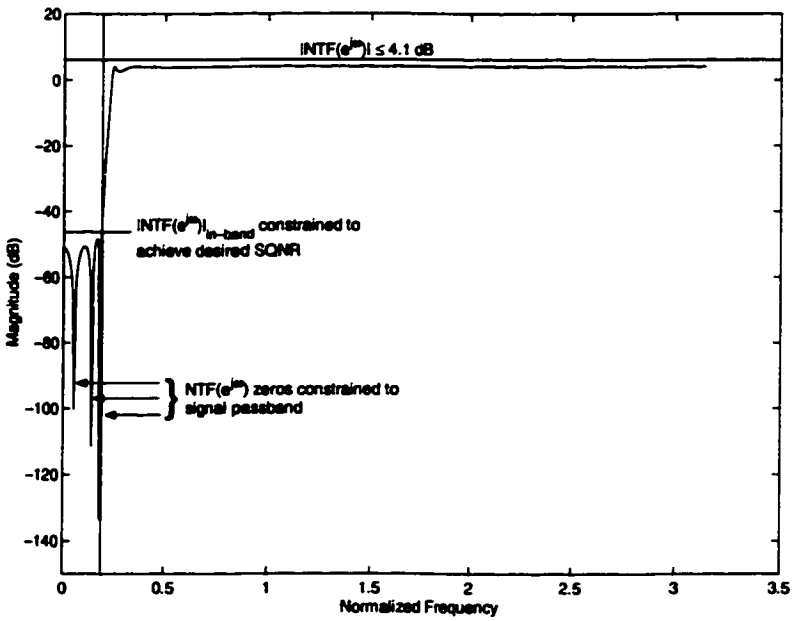

Figure 3.1: Illustration of Noise Transfer Function Constraints

and, ultimately, achieve higher in-band noise reduction. To illustrate the constraints, consider the magnitude-response of the optimized noise transfer function $NTF(z)$ as shown in Fig. 3.1.

Upon the successful completion of the optimization process, the resulting $N(z)$ and $D(z)$ may be substituted into Eqn. 2.5 to obtain the polynomial $S(z)$ (except in the case of the MF Σ-Δ A/D converter, where $S(z) = gz^{-N}$). The next step in the design process involves the synthesis of a Σ-Δ A/D converter configuration for nonlinear simulation. The nonlinear simulation is at present the only practical approach for determining the actual performance of the designed Σ-Δ A/D converter.

3.2.3 Realization of Signal and Noise Transfer Functions

By employing one of the five Σ-Δ A/D converter configurations described in the previous chapter, the constituent multiplier coefficients can be determined as follows:

Case a) COR Σ-Δ A/D converters: The multiplier coefficients R_k are obtained from the zero frequencies ω_{zk} in accordance with (Botteron et. al., [17])

$$R_k = 2cos(\frac{\omega_{zk}}{f_s}) - 2. \tag{3.11}$$

Then, $\mathcal{A} = \mathcal{C}_{1COR}^{-1}\mathcal{S}$ and $\mathcal{B} = \mathcal{C}_{2COR}^{-1}\mathcal{D}$.

Case b) COI Σ-Δ A/D converters: $\mathcal{A} = \mathcal{C}_{1COI}^{-1}\mathcal{S}$ and $\mathcal{B} = \mathcal{C}_{2COI}^{-1}\mathcal{N}$.

Case c) CRI Σ-Δ A/D converters: The multiplier coefficients R_k are determined in much the same way as for the COR Σ-Δ A/D converters. Then, $\mathcal{A} = \mathcal{C}_{CRI}^{-1}\mathcal{S}$.

Case d) FF Σ-Δ A/D converters: The multiplier coefficients R_k are determined directly through the optimization of the noise transfer function $NTF(z)$. Then, $\mathcal{A} = \mathcal{C}_{FF}^{-1}\mathcal{D}$.

Case e) MF Σ-Δ A/D converters: The multiplier coefficients R_k are determined in the same way as

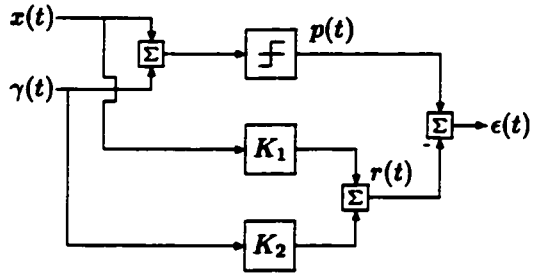

Figure 3.2: Describing Function Method

for the FF Σ-Δ A/D converters. Then, $\mathcal{B} = \mathcal{C}_{MF}^{-1}\mathcal{D}$. The multiplier coefficient g can be determined from Eqn. 2.63 with $w_p = 0$ rad/s.

3.3 Hitherto Stability Estimation Technique

As is obvious from the above design procedure, limiting the out-of-band noise gain (c.f. Eqn. 3.10) is the only precaution taken to attempt to ensure that the resulting Σ-Δ A/D converter exhibits stable operation. However, the exact point of instability remains unknown until extensive simulations are performed. It would be beneficial to know at what DC input signal level instability occurs (without recourse to extensive and time consuming simulations). To address this problem, in (Ardalan et. al., [14]) and (L. Risbo, [19]) a statistical technique was developed to estimate the maximum DC input signal amplitude for stable Σ-Δ A/D converter operation. The details of this statistical technique are discussed in the following.

In control theory, nonlinear systems are often analysed using the describing function method. In this method, the nonlinear element is replaced by an accurate linear model. Booton (Booton, [20]) suggested to replace the nonlinear element by an equivalent gain element. Consider the system shown in Fig. 3.2, here $x(t)$ represents a DC signal and $\gamma(t)$ represents a zero mean stochastic signal. The two gain elements K_1 and K_2 are chosen to minimize the mean squared error between the output of the nonlinearity $p(t)$ and the output of the linear approximation $r(t)$. Although the error $\epsilon(t)$ generated by the approximation is usually ignored in control theory, when applying this method to the analysis of Σ-Δ A/D converters, $\epsilon(t)$ becomes an important quantity which cannot be ignored (Ardalan et. al., [14]). If $\epsilon(t)$ is assumed to have a white spectrum, then the quantizer may be replaced by a variable gain element k and a white additive noise source $\epsilon(t)$. In this way, one obtains the new linear Σ-Δ A/D converter model as shown in Fig. 3.3, where $Q(z)$ represents the (z-transformed) error $\epsilon(t)$.

In the design of feedforward and multiple-feedback Σ-Δ A/D converters, having determined the noise transfer function $NTF(z) = \frac{N(z)}{D(z)}$ (starting from a set of system design specifications), a modified noise transfer function can be defined in terms of the variable gain element k in accordance

with

$$\widetilde{NTF}(z) = \frac{N(z)}{kD(z) - kN(z) + N(z)}. \tag{3.12}$$

This gives rise to the definition of the noise power gain (NPG) in accordance with (L. Risbo, [19])

$$NPG = \frac{2}{\pi}\int_{-\pi}^{\pi} |\widetilde{NTF}(e^{jwT})|^2 dw. \tag{3.13}$$

From this equation, one can obtain a graphical representation of NPG versus k, leading to an important empirical result for higher order Σ-Δ A/D converters, namely that NPG is a convex function of k with a minimum occurring, say, at NPG_{min}. For example, consider the NPG versus k curve shown in Fig. 3.4. This NPG_{min} point is of interest as it demonstrates a very important relationship between the variable gain element k and the stability of the Σ-Δ A/D converter. The case when k is such that NPG corresponds to NPG_{min} is referred to as the point of equilibrium. When k increases slightly, this causes an increase in NPG resulting in more noise appearing at the quantizer input. This in turn causes a decrease in k which returns the system to the equilibrium point. Now consider the case when k decreases slightly from the equilibrium point. A decrease in k causes an increase in NPG which results in an increase in the noise at the quantizer input. This in turn causes k to decrease even more. As is evident, k will never return to the point of equilibrium and the system becomes unstable. Thus, one may conclude that NPG_{min} corresponds to the minimal allowable value of k for stable operation. In the statistical technique, a relationship is derived between NPG_{min} and the maximum DC input signal amplitude $m_{u_{max}}$ based on the following three assumptions, a) that the input signal $u(n)$ is a DC signal of amplitude m_u, b) that the quantizer input signal $e(n)$ is the sum of a zero mean Gaussian distributed component G_e and a DC bias m_e, and c) that the quantization noise $Q(z)$ is a uniformly distributed white noise with zero mean.

Based on the above assumptions, the variance of the output signal $y(n)$ can be calculated in two ways, namely,

$$\sigma_y^2 = E\left\{y(n)^2\right\} - E^2\left\{y(n)\right\} = 1 - m_u^2, \tag{3.14}$$

or

$$\sigma_y^2 = \sigma_N^2 NPG, \tag{3.15}$$

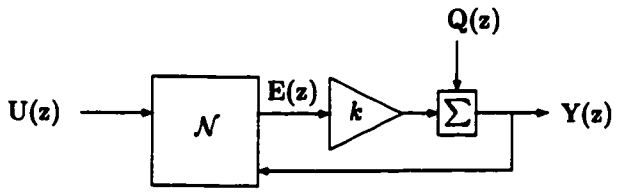

Figure 3.3: Linearized Σ-Δ A/D Converter

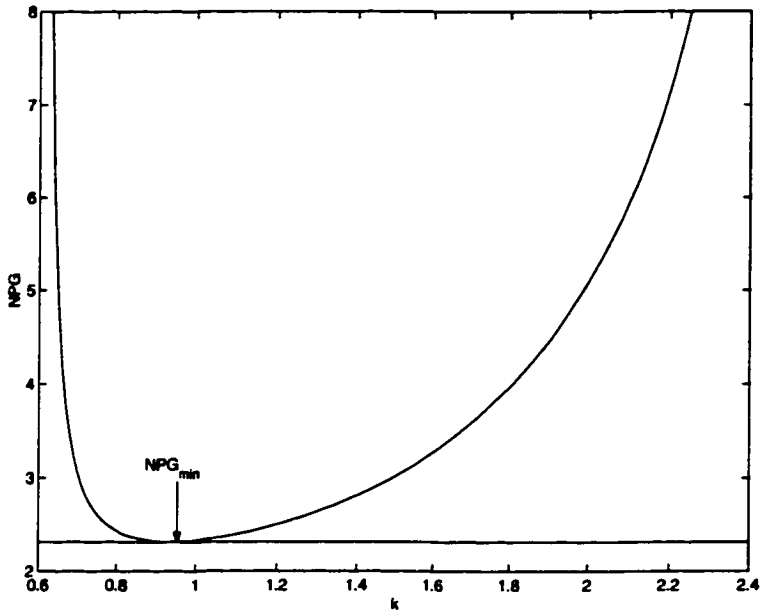

Figure 3.4: Noise Power Gain versus k

where $E\{\cdot\}$ is the expectation operator. By combining Eqns. 3.14 and 3.15, one obtains the relationship

$$NPG = \frac{1 - m_u^2}{\sigma_N^2}. \tag{3.16}$$

Next, it is desired to determine σ_N^2 in terms of the DC input signal amplitude m_u. To this end, from Fig. 3.3, the output signal $y(n)$ can be expressed

$$y(n) = ke(n) + q(n). \tag{3.17}$$

But, since $q(n)$ has zero mean, and since the mean of $y(n)$ is m_u, $y(n)$ can be written in the form

$$y(n) = m_u + k[e(n) - m_e] + q(n). \tag{3.18}$$

Moreover, in (Ardalan et. al., [14]) it was argued that since the quantizer input signal $e(n)$ is an integration of the white noise $q(n)$, its distribution can be assumed to be Gaussian. In this way, let G_e represent the zero mean Gaussian distributed component of the quantizer input signal $e(n)$ given by $G_e = e(n) - m_e$. Then, Eqn. (3.18) can be written as

$$y(n) = m_u + kG_e + q(n). \tag{3.19}$$

The variance of $y(n)$ may be determined from Eqn. (3.18) as

$$\begin{aligned} \sigma_y^2 &= E\left\{[m_u + kG_e + q(n)]^2\right\} - E^2\left\{m_u + kG_e + q(n)\right\} \\ &= k^2\sigma_{G_e}^2 + \sigma_N^2. \end{aligned} \tag{3.20}$$

By substituting σ_y^2 from Eqn. (3.14) into (3.20) (L. Risbo, [19]), one gets

$$\sigma_N^2 = 1 - m_u^2 - k^2\sigma_{G_e}^2. \tag{3.21}$$

To determine the value of k in terms of the DC input amplitude m_u, it is convenient to ensure that the white noise $q(n)$ is uncorrelated with the Gaussian component of the quantizer input G_e, yielding $E\{G_eN(n)\} = 0$. The variable gain k may then be determined from

$$\begin{aligned} Cov\{G_e, y(n)\} &= E\{(G_e - E\{G_e\})(y(n) - m_u)\} \\ &= k\sigma_{G_e}^2. \end{aligned} \tag{3.22}$$

By rearranging Eqn. 3.22, one can write

$$k = \frac{Cov\{G_e, y(n)\}}{\sigma_{G_e}^2} = \frac{1}{\sigma_{G_e}^2}\int_{-\infty}^{\infty} \frac{G_e y(n)}{\sigma_{G_e}\sqrt{2\pi}} e^{\frac{-G_e^2}{2\sigma_{G_e}^2}} dG_e \tag{3.23}$$

(by taking into account the fact that G_e has a Gaussian distribution). This integral can be simplified if one realizes that $y(n)$ will be -1 if the input to the quantizer is negative and $+1$ if the input to the quantizer is positive, leading to

$$k = \frac{1}{\sigma_{G_e}^2}\left[-\int_{-\infty}^{-m_e} G_e \frac{1}{\sigma_{G_e}\sqrt{2\pi}} e^{\frac{-G_e^2}{2\sigma_{G_e}^2}} dG_e + \int_{-m_e}^{\infty} G_e \frac{1}{\sigma_{G_e}\sqrt{2\pi}} e^{\frac{-G_e^2}{2\sigma_{G_e}^2}} dG_e\right] \tag{3.24}$$

$$= \frac{1}{\sigma_{G_e}^2}\left[2\int_{m_e}^{\infty} G_e \frac{1}{\sigma_{G_e}\sqrt{2\pi}} e^{\frac{-G_e^2}{2\sigma_{G_e}^2}} dG_e\right]. \tag{3.25}$$

By carrying out the integration, one arrives at the same result reported in (Ardalan et. al., [14])

$$k = \frac{2}{\sigma_{G_e}\sqrt{2\pi}} e^{\frac{-m_e^2}{2\sigma_{G_e}^2}}. \tag{3.26}$$

Next, the mean of the output m_y can be determined as the probability that the quantizer input is positive (leading to $+1$ output) minus the probability that the quantizer input is negative (leading to -1 output) (Vogels et. al., [21])

$$m_y = P(e(n) > 0) - P(e(n) < 0) \tag{3.27}$$

$$= P(G_e > -m_e) - P(G_e < -m_e). \tag{3.28}$$

But, since G_e has a Gaussian distribution, m_y may be expressed as

$$m_y = \frac{1}{2}\left[1 + erf(\frac{m_e}{\sigma_{G_e}\sqrt{2}})\right] - \frac{1}{2}\left[1 + erf(\frac{-m_e}{\sigma_{G_e}\sqrt{2}})\right] \tag{3.29}$$

$$= erf(\frac{m_e}{\sqrt{2}\sigma_{G_e}}). \tag{3.30}$$

By substituting m_u for m_y in Eqn. 3.30, one obtains the relationship

$$m_u = erf(\frac{m_e}{\sqrt{2}\sigma_{G_e}}) \tag{3.31}$$

$$\frac{m_e}{\sqrt{2}\sigma_{G_e}} = erf^{-1}(m_u). \tag{3.32}$$

By substituting Eqn. 3.32 into Eqn. 3.26, one gets

$$k = \frac{2}{\sigma_{G_e}\sqrt{2\pi}} e^{-2[erf^{-1}(m_u)]^2}. \tag{3.33}$$

By substituting k from Eqn. 3.33 into Eqn. 3.21, the following expression is obtained for σ_N^2

$$\sigma_N^2 = 1 - m_u^2 - \frac{2}{\pi} e^{-2[erf^{-1}(m_u)]^2}. \tag{3.34}$$

Now σ_N^2 is a function of the DC input level m_u only. Substituting σ_N^2 from Eqn. 3.34 into Eqn. 3.16

$$NPG = \frac{1 - m_u^2}{1 - m_u^2 - \frac{2}{\pi} e^{-2[erf^{-1}(m_u)]^2}} \tag{3.35}$$

which is the same as the result reported in (L. Risbo, [19]). A graphical representation of NPG versus m_u can be obtained from 3.35 and is shown in Fig. 3.5. By using the method presented in (L. Risbo, [19]), the maximum DC input signal amplitude $m_{u_{max}}$ corresponds to NPG_{min}.

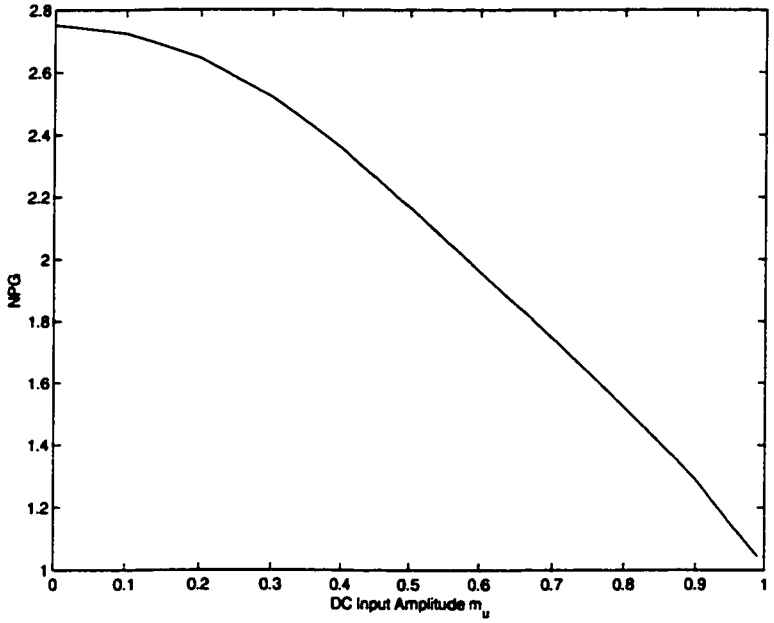

Figure 3.5: NPG versus m_u Curve

3.4 Application to the Design and Investigation of Feedforward and Multiple-Feedback Σ-Δ A/D Converter Configurations

This section presents the design and computational investigation of the FF, MF, COR, COI, CRI Σ-Δ A/D converters satisfying the high-level system design specifications given in Table 3.2. This investigation includes the determination of the impact of the complementarity of the signal and noise transfer functions and the relative position of the noise transfer function zeros with respect to the unit-circle on the achievable $SQNR$ and the stability of the Σ-Δ A/D converter.

Table 3.2: Lowpass Σ-Δ A/D Converter Design Specifications

Sampling Frequency	640 kHz
Passband Edge Frequency	20 kHz
Desired $SQNR$	60 dB
Order	6

Table 3.3: COI, COR, CRI Noise and Signal Transfer Function Coefficients

a_1	−5.94328676651853	a_2	14.77398202742605
a_3	−19.66138848176253	a_4	14.77398202742605
a_5	−5.94328676651853	a_6	1
b_1	−5.01674259948316	b_2	10.60088164334243
b_3	−12.06101474655878	b_4	7.78768867203415
b_5	−2.70579462641319	b_6	0.39572200430432
c_1	−0.92654416703537	c_2	4.17310038408362
c_3	−7.60037373520375	c_4	6.98629335539190
c_5	−3.23749214010534	c_6	0.60427799569568

The signal and noise transfer functions $STF(z)$ and $NTF(z)$ were determined using the design procedure outlined in the previous section, leading to

$$NTF(z) = \frac{1 + a_1 z^{-1} + a_2 z^{-2} + a_3 z^{-3} + a_4 z^{-4} + a_5 z^{-5} + a_6 z^{-6}}{1 + b_1 z^{-1} + b_2 z^{-2} + b_3 z^{-3} + b_4 z^{-4} + b_5 z^{-5} + b_6 z^{-6}}, \tag{3.36}$$

$$STF(z) = \frac{0 + c_1 z^{-1} + c_2 z^{-2} + c_3 z^{-3} + c_4 z^{-4} + c_5 z^{-5} + c_6 z^{-6}}{1 + b_1 z^{-1} + b_2 z^{-2} + b_3 z^{-3} + b_4 z^{-4} + b_5 z^{-5} + b_6 z^{-6}}, \tag{3.37}$$

where the coefficients a_1 through a_6, b_1 through b_6, and c_1 through c_6 are shown for the COI, COR, CRI A/D converters in Table 3.3, for the FF A/D converter in Table 3.4, and for the MF A/D converter in Table 3.5. A plot of the magnitudes of the signal and noise transfer functions $STF(z)$ and $NTF(z)$ is shown in Figs. 3.6, 3.7, and 3.8 for the COI, COR, CRI A/D converters, for the FF A/D converter, and for the MF A/D converter, respectively.

The multiplier coefficients associated with each of the five Σ-Δ A/D converters can be determined as tabulated in Tables 3.6 to 3.10.

An estimation of the maximum DC input signal amplitude can be made for each the five Σ-Δ A/D converter configurations as discussed in (Fraser et. al., [22]). The plot of noise power gain NPG versus k is as shown in Fig. 3.4 for the COI, COR, and CRI Σ-Δ A/D converters, and in Fig. 3.9 for the FF and MF A/D converters. In the case of the COI, COR, and CRI A/D converters, the minimum noise power gain is $NPG_{min} = 2.3139$, and in the case of the FF and MF converters the minimum noise power gain is $NPG_{min} = 2.3201$. Using the NPG versus m_u curve shown in

Table 3.4: FF Noise and Signal Transfer Function Coefficients

a_1	-6	a_2	15.05450564724798
a_3	-20.21802258899191	a_4	15.32783163869487
a_5	-6.21961809940591	a_6	1.05530529079727
b_1	-5.06741976440183	b_2	10.80969686910854
b_3	-12.41401211472861	b_4	8.09073970446889
b_5	-2.83633028749370	b_6	0.41770386131672
c_1	-0.93258023559817	c_2	4.24480877813944
c_3	-7.80401047426331	c_4	7.23709193422597
c_5	-3.38328781191221	c_6	0.63760142948055

Table 3.5: MF Noise and Signal Transfer Function Coefficients

a_1	-6	a_2	15.05450564724798
a_3	-20.21802258899191	a_4	15.32783163869487
a_5	-6.21961809940591	a_6	1.05530529079727
b_1	-5.06741976440183	b_2	10.80969686910854
b_3	-12.41401211472861	b_4	8.09073970446889
b_5	-2.83633028749370	b_6	0.41770386131672
c_1	.0003782682700190776	c_2	0
c_3	0	c_4	0
c_5	0	c_6	0

Table 3.6: Cascade-of-Integrators Nominal Multiplier Coefficients

A_1	-0.92654416703537	A_2	-0.45962045109323
A_3	-0.17341386922298	A_4	-0.04166721607133
A_5	-0.00634593377516	A_6	-0.00073830717325
B_1	-0.05671323348147	B_2	-0.05754819483339
B_3	-0.00167196275635	B_4	-0.00084108150945
B_5	-0.00000612015753	B_6	-0.00000204005251

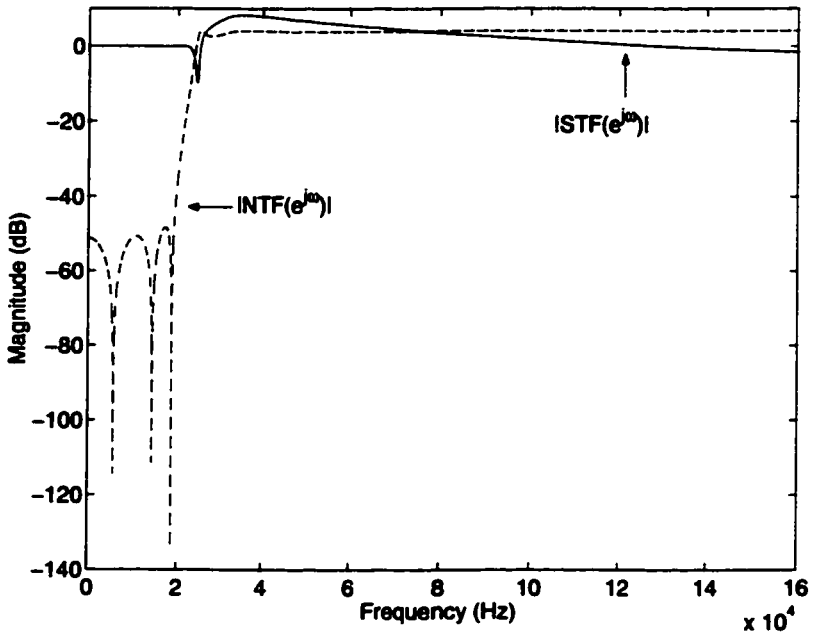

Figure 3.6: COI, COR, CRI $NTF(z)$ and $STF(z)$

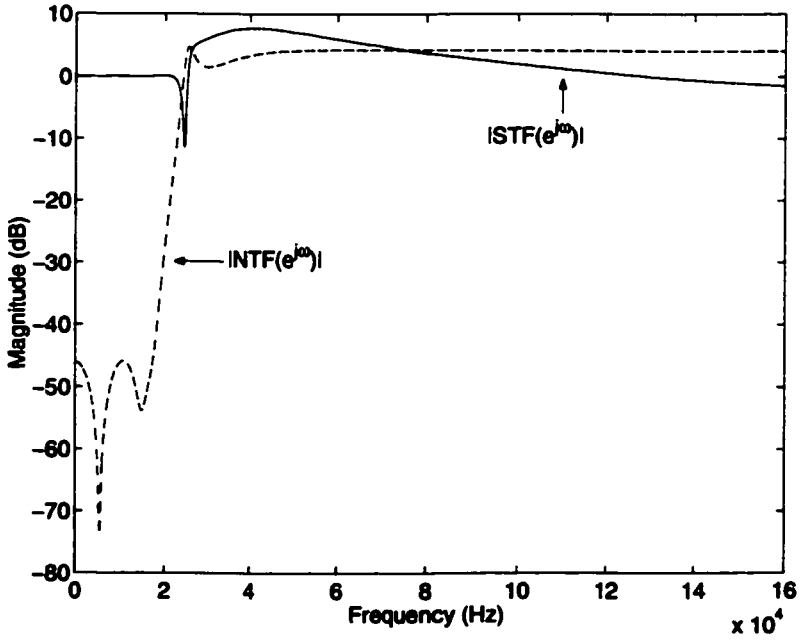

Figure 3.7: FF $NTF(z)$ and $STF(z)$

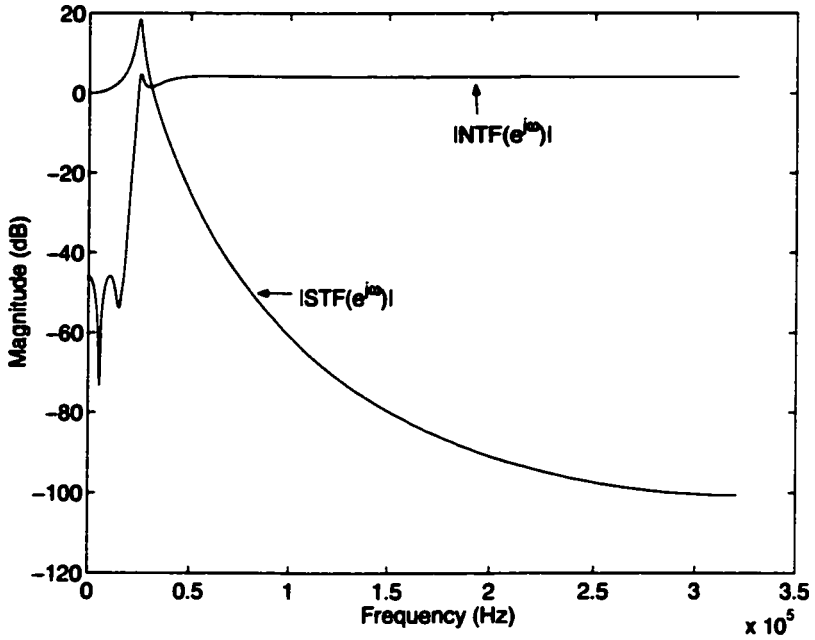

Figure 3.8: MF $NTF(z)$ and $STF(z)$

Table 3.7: Cascade-of-Resonators/Integrators Nominal Multiplier Coefficients

A_1	-0.92654416703537	A_2	-0.43838026849507
A_3	-0.14206827654349	A_4	-0.03104811402208
A_5	-0.00571151995615	A_6	-0.00061758532218
R_3	-0.03378914270000	R_2	-0.01988834394359
R_1	-0.00303574683789		

Table 3.8: Cascade-of-Resonators Nominal Multiplier Coefficients

A_1	-0.92654416703537	A_2	-0.43838026849507
A_3	-0.14206827654349	A_4	-0.03104811402208
A_5	-0.00571151995615	A_6	-0.00061758532218
B_1	-0.92654416703537	B_2	-0.43838026849507
B_3	-0.14206827654349	B_4	-0.03104811402208
B_5	-0.00571151995615	B_6	-0.00061758532218
R_1	-0.03378914270000	R_2	-0.01988834394359
R_3	-0.00303574683789		

Table 3.9: Feedforward Nominal Multiplier Coefficients

A_1	-0.93258023559817	A_2	-0.41809239985141
A_3	-0.10246763078235	A_4	-0.01032056324723
A_5	-0.00111897652411	A_6	0.00020433107546
R_1	-0.00291749958148	R_2	-0.02154114106385
R_3	-0.03004700660265		

Table 3.10: Multiple-Feedback Nominal Multiplier Coefficients

B_6	-0.93258023559817	B_5	-0.41809239985141
B_4	-0.10246763078235	B_3	-0.01032056324723
B_2	-0.00111897652411	B_1	0.00020433107546
R_3	-0.00291749958148	R_2	-0.02154114106385
R_1	-0.03004700660265	g	0.93570000000000

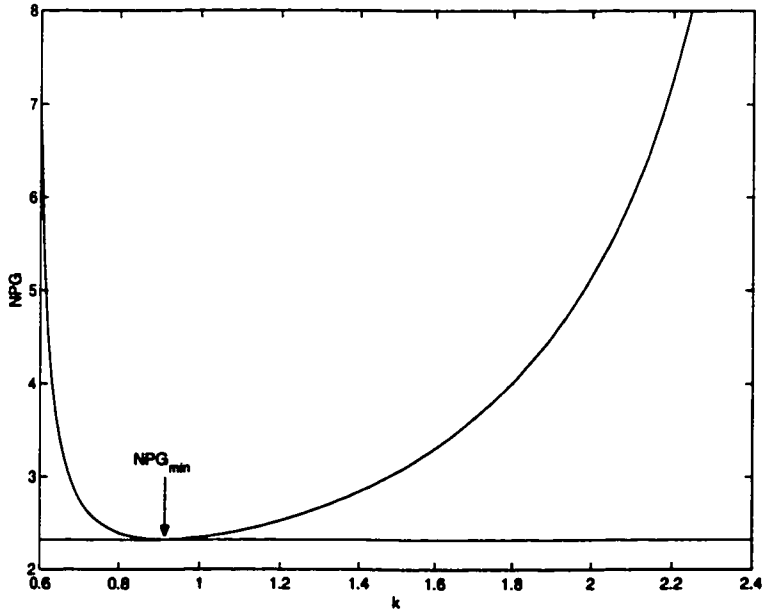

Figure 3.9: Noise Power Gain versus k for FF and MF Σ-Δ A/D Converters

Table 3.11: Maximum Stable DC Input Signal Amplitude m_{umax}

	COI	COR	CRI	FF	MF
Simulated Results	0.41	0.41	0.41	0.46	0.44
Predicted Results	0.42	0.42	0.42	0.42	0.42

Fig. 3.5, NPG_{min} corresponds to $m_{umax} = 0.4226 \approx 0.42$ in the case of the COI, COR, and CRI A/D converters, and to $m_{umax} = 0.4193 \approx 0.42$ in the case of the FF and MF converters. To verify the accuracy of these estimations for the maximum DC input signal, an empirical investigation was undertaken. Each of the five A/D converters was simulated with a DC input signal which was swept from a value of 0 to a value of 1 in increments of 0.01 to determine their maximum input signal level for stable converter operation. The results of these simulations are as shown in Table 3.11. These results show that the statistical estimation technique did not accurately estimate the maximum DC input signal level and led to a maximum error of 0.04 between the simulated and estimated results.

The achievable $SQNR$ as a function of the amplitude of a sinusoidal input signal was determined for each of the five Σ-Δ A/D converters by selecting the input signal frequency as 3 kHz. Repeated simulations reveal that the COR, COI, and CRI A/D converters features a $SQNR$ performance level of 61.124 dB and a dynamic range of 69.5 dB (as shown in Fig. 3.10 for FF, MF, and CRI A/D converters). From Fig. 3.10, the FF and MF A/D converters gave significantly poorer $SQNR$

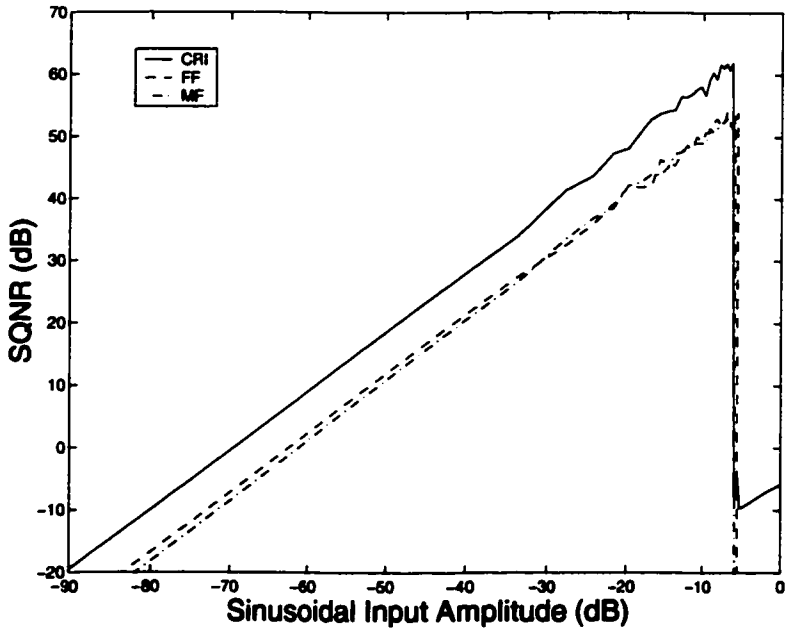

Figure 3.10: $SQNR$ versus Sinusoidal Input Signal Level

performance of 52.9 dB and 52.8 dB, respectively. The dynamic range of 62.4 dB and 61.2 dB for the FF and MF A/D converters was also significantly lower as compared to the COR, COI,

Table 3.12: COI Σ-Δ A/D Converter Scaled Capacitor Values

Capacitor	Value	Capacitor	Value
CB_1	−28.298395211164	CA_1	−13.59099104581705
CB_2	−122.151584192600	CA_2	−28.67968286343373
CB_3	−15.096768574766	CA_3	−46.03083238002003
CB_4	−32.306170732969	CA_4	−47.04890115108366
CB_5	−1	CA_5	−30.48179483135976
CB_6	−1.417975557543	CA_6	−15.08592999114161
CX_1	34.01671711982564	CF_1	498.973404865214
CX_2	1	CF_2	4.253926678031
CX_3	1	CF_3	4.253926678031
CX_4	1	CF_4	4.253926678031
CX_5	1	CF_5	4.253926678031
CX_6	1	CF_6	4.253926678031
CFG	34.01671711982564	CF_7	1

and CRI A/D converters and failed to satisfy the system specifications completely. This poorer $SQNR$ performance can be attributed to the noise transfer function zeros being located outside the unit-circle. However, the complementarity of the signal and noise transfer functions $STF(z)$ and $NTF(z)$ does not seem to have a direct impact on the achievable $SQNR$ or DR.

3.4.1 Investigation of the Effect of Capacitor Mismatches

This subsection is concerned with the simulation of the corresponding switched-capacitor hardware implementation of each of the five Σ-Δ A/D converters. First, the capacitors will be scaled for both minimum spread and minimum total capacitance. A Monte-Carlo analysis will then be performed to determine the $SQNR$ characteristic of each of the five A/D converters in the presence of capacitor mismatches.

The nominal capacitor values for the COI Σ-Δ A/D converter may be determined as given in Table 2.1, where the multiplier values are as given in Table 3.6. These capacitor values result in a capacitance spread of $C_{spread} = 490183.5$ and a total capacitance of 1531338.15 units. The nominal capacitor values were then scaled using the technique presented in (Gregorian et. al., [23]), resulting in the scaled capacitor values as given in Table 3.12. These new capacitor values lead to a reduction of the capacitor spread to $C_{spread} = 498.97$ and a reduction of the total capacitance to 975 units.

Similarly, the nominal capacitor values for the other four A/D converters were determined and scaled, resulting in the capacitor values given in Tables 3.14 to 3.16. The capacitor spread values and total capacitance for both the nominal and scaled capacitors are given in Table 3.17 for each

Table 3.13: CRI Σ-Δ A/D Converter Scaled Capacitor Values

Capacitor	Value	Capacitor	Value
CR_1	1	CA_1	−8.22169054385137
CR_2	1	CA_2	−16.54763749373107
CR_3	1.27544628443914	CA_3	−35.63872118651384
		CA_4	−33.13219621383988
		CA_5	−27.43447783210772
		CA_6	−12.61920413533742
CX_1	1	CF_1	8.87350094724358
CX_2	1	CF_2	4.25392667803142
CX_3	1.77857170152340	CF_3	11.81983402160172
CX_4	1	CF_4	4.25392667803142
CX_5	17.20340639147583	CF_5	77.43627414646043
CX_6	1	CF_6	4.25392667803143
CFG	1	CF_7	1

of the five A/D converters. It is easily observed that the COR A/D converter satisfied the design specifications with the smallest amount of capacitor spread and total capacitance. The COI A/D converter had the largest amount of spread and total capacitance. This is caused by the fact that the configuration has all of the B coefficients feedback to the same op-amp.

Monte-Carlo simulations of 1000 different samples of each of the five Σ-Δ A/D converters led to the determination of the actual $SQNR$s as shown in Fig. 3.11, and as summarized in Table 3.18, where the capacitor values were individually perturbed around their nominal values with a Gaussian distributed white random variable ϵ of zero mean and standard deviation of $\sigma = 0.00333$ [2]. Under capacitance perturbations, the COI A/D converter gave rise to more unstable samples and the highest amount of $SQNR$ variance among the stable samples than the FF, MF, COR, and CRI A/D converters. Since the noise transfer function zeros for the COI A/D converter are nominally forced to be on the unit-circle by numerical optimization, the zeros of $NTF(z)$ may move off the unit-circle significantly due to capacitor mismatches, affecting the achievable $SQNR$, and thus resulting in more $SQNR$ variance among the samples, and, ultimately, more unstable samples. The lowest amount of $SQNR$ variance was observed when the Σ-Δ A/D converter configuration proper guaranteed the location of the noise transfer function zeros on the unit-circle. Conclusion cannot be drawn concerning the number of unstable samples and the location of the noise transfer function zeros either on or off the unit-circle. Similarly, no direct impact can be observed between the complementarity of the signal and noise transfer functions and the stability of the Σ-Δ A/D

[2]The samples with substantially low $SQNR$ imply unstable Σ-Δ A/D converter operation and were discarded.

Table 3.14: COR Σ-Δ A/D Converter Scaled Capacitor Values

Capacitor	Value	Capacitor	Value
CB_1	−1.46678387304306	CA_1	−1.46678387304306
CB_2	−12.97399796104120	CA_2	−12.97399796104128
CB_3	−2.08198267851292	CA_3	−2.08198267851306
CB_4	−5.67533631781905	CA_4	−5.67533631781965
CB_5	−3.69115003623503	CA_5	−3.69115003624335
CB_6	−13.58583746209491	CA_6	−13.58583746210956
CX_1	1	CF_1	34.03920815734993
CX_2	2.73716752109054	CF_2	9.67731772479131
CX_3	1	CF_3	12.47315669015196
CX_4	8.14081390370671	CF_4	4.03111325572408
CX_5	1	CF_5	18.69488625077205
		CF_6	1.58306956670644
CR_1	1	CR_2	1
CR_3	1		

Table 3.15: FF Σ-Δ A/D Converter Scaled Capacitor Values

Capacitor	Value	Capacitor	Value
CR_1	−1.11398979509243	CA_1	−3.69033852569051
CR_2	−1	CA_2	−7.03796775824170
CR_3	−1	CA_3	−11.69153932402205
		CA_4	−5.00931566255049
		CA_5	−4.73353916965130
		CA_6	3.67696436403021
CX_1	20.36170764795855	CF_1	80.57386519017499
CX_2	1	CF_2	4.25397565345412
CX_3	1.61002009005616	CF_3	10.91292813509342
CX_4	1	CF_4	4.25392667803142
CX_5	1	CF_5	8.71545369831970
CX_6	1	CF_6	4.25392667803142
CFG	20.36170764795855	CF_7	1

Table 3.16: MF Σ-Δ A/D Converter Scaled Capacitor Values

Capacitor	Value	Capacitor	Value
CB_1	−1	CR_1	−1
CB_2	−143.304198800343	CR_2	−1
CB_3	−1.210686601624	CR_3	−1.77582015990610
CB_4	−1.212134792913	CG	1.85127000440464
CB_5	−1		
CB_6	1		
CX_1	1.791945980779	CF_1	9.813476006909
CX_2	1.418270727298	CF_2	10.791949724806
CX_3	1	CF_3	9.940177492839
CX_4	135.485910822408	CF_4	4.670248611563
CX_5	1.002441188223	CF_5	320.430712361000
		CF_6	1.072294065925

Table 3.17: Comparison of Capacitance Spread and Total Capacitance

	Nominal Capacitors		Scaled Capacitors	
	Total	Spread	Total	Spread
COI	1531338.15	490183.5	975.47	498.97
COR	2189.35	1619.21	176.33	34.04
CRI	4376.50	1619.21	272.74	77.44
FF	13887.64	4894.02	199.25	80.57
MF	7882.61	9060.20	651.77	320.43

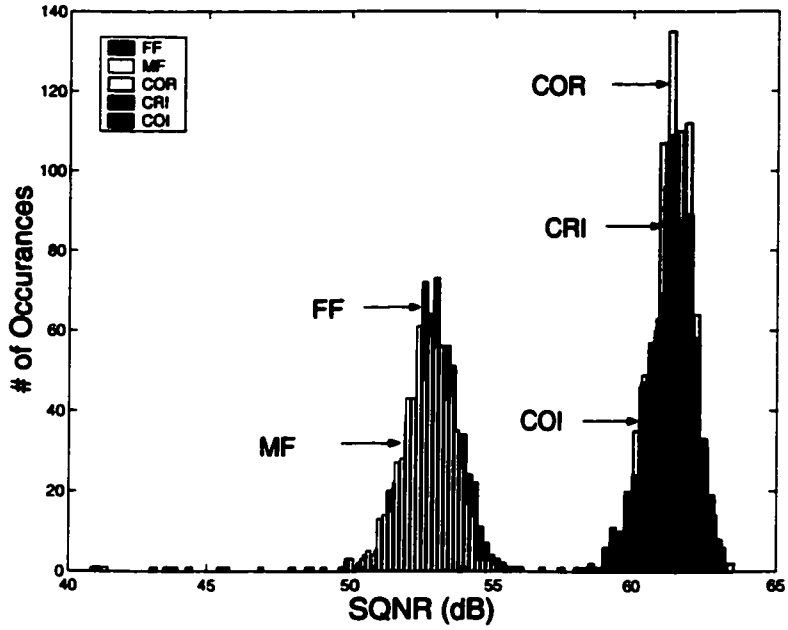

Figure 3.11: Monte-Carlo Simulation Results

Table 3.18: Monte-Carlo Simulation Results

$SQNR$ (ϵ_{max}=1%)	FF	MF	COR	COI	CRI
Nominal (dB)	52.927	52.321	61.124	61.124	61.124
Variance (dB)	0.820	0.757	0.565	1.175	0.591
Max. (dB)	55.853	55.307	63.599	63.072	63.188
Min. (dB)	50.005	50.081	57.455	50.320	56.069
Mean (dB)	52.880	52.690	61.388	61.180	61.404

converter.

Finally, the above Monte-Carlo simulations were repeated for several other standard deviations. The main results of these simulations are as summarized in Table 3.19. Both the MF and FF Σ-Δ A/D converters exhibited low sensitivity to capacitor mismatches compared to the COR, COI, and CRI A/D converters. These A/D converters did not give the best overall performance, but gave the most consistent performance in terms of the number of unstable samples. The COI A/D converter was more sensitive to capacitor mismatches than the other A/D converters, but gave very good performance relative to the other A/D converters with a tolerance level of 0.1%. The COR and CRI A/D converters were more insensitive to the capacitor mismatches than the COI A/D converter, but showed a consistent increase in the number of unstable samples as a function of capacitor mismatches. The main advantage of the complementarity of the signal and noise transfer functions $STF(z)$ and $NTF(z)$ is the reduction in the complexity of the design and optimization

Table 3.19: Percentage of Unstable Samples

ϵ_{max}	FF	MF	COR	COI	CRI
0.1	24.8	32.6	18.4	16.6	23.4
0.5	25.4	31.8	22.0	24.7	25.0
1.0	26.6	33.1	24.9	37.4	28.4
1.5	26.9	33.6	33.3	43.7	36.2
2.0	29.8	34.3	39.4	51.8	42.3

of the Σ-Δ A/D converter. However, in the design of feedforward and multiple-feedback bandpass Σ-Δ A/D converters, the complementarity of the transfer functions leads to a significant reduction in both capacitance spread and total capacitance (Fraser et. al., [24]).

3.5 A Novel Statistical Approach for the Estimation of Stability in Feedforward and Multiple-Feedback Oversampled Σ-Δ A/D Converter Configurations

This section presents a novel statistical approach (Fraser et. al., [25]) employing the Gram-Charlier series to model the quantizer input signal. This approach makes no recourse to the assumption that the quantizer input signal has a Gaussian distribution.

The Gram-Charlier series is well known for its application to the approximation of probability density functions based on the normal distribution and its derivatives. This series is defined as (Springer, [26])

$$f_N(z) = \sum_{j=0}^{N} C_j H_j(z)\phi(z), \tag{3.38}$$

where

$$z = \frac{x - \mu_x}{\sigma_x}, \tag{3.39}$$

where N represents the number of terms in the series expansion (controlling the precision). Moreover, $\phi(z)$ represents the characteristic function of z,

$$\phi(z) = \frac{1}{\sqrt{2\pi}} e^{-\frac{z^2}{2}}, \tag{3.40}$$

$H_n(z)$ represents the n-th Hermite polynomial,

$$H_0 = 1 \tag{3.41}$$

$$H_1 = z \tag{3.42}$$

$$H_2 = z^2 - 1 \tag{3.43}$$

$$H_n = zH_{n-1}(z) - (n-1)H_{n-2}(z), \tag{3.44}$$

and c_n represents the n-th Hermite coefficient,

$$C_n = \frac{1}{n!} \sum_{k=0}^{\lfloor \frac{n}{2} \rfloor} \left(\frac{-1}{2} \right)^k \frac{n! v_{n-2k}}{k!(n-2k)!}, \tag{3.45}$$

with v_n representing the n-th normalized central moment of x,

$$v_n = \frac{E\left[(x-\mu_x)^n\right]}{\sigma_x^n}. \tag{3.46}$$

From Section 3.3, the distribution of the quantizer input enters into the derivation of the statistical technique in Eqns. 3.23 and 3.30. Therefore, Eqn. 3.23 can be modified to include the Gram-Charlier series leading to a new expression for k (Fraser et. al. [25]):

$$k = \frac{2}{\sigma_{G_e}^2 \sqrt{2\pi}} e^{\frac{-m_e^2}{2\sigma_u^2}} \left[\sigma_{G_e} - m_e + C_1 \sqrt{\frac{\pi}{2}} erf\left(\frac{m_e}{\sqrt{2}\sigma_{G_e}} \right) e^{\frac{m_e^2}{2\sigma_{G_e}^2}} + \sum_{i=2}^{N} C_i \left[-m_e H_{i-1}(-m_e) + \sigma_{G_e} H_{i-2}(-m_e) \right] \right]. \tag{3.47}$$

A complete derivation of this expression for k can be found in Appendix A.2. In practical situations, it so happens that C_1 is approximately zero, yielding the simplified expression for k,

$$k = \frac{2}{\sigma_{G_e}^2 \sqrt{2\pi}} e^{\frac{-m_e^2}{2\sigma_u^2}} \left[\sigma_{G_e} - m_e + \sum_{i=2}^{N} C_i \left[-m_e H_{i-1}(-m_e) + \sigma_{G_e} H_{i-2}(-m_e) \right] \right]. \tag{3.48}$$

Similarly, Eqn. 3.30 can be modified to the following form (Fraser et. al., [25])

$$m_y = \frac{2}{\sqrt{2\pi}} \left[\sqrt{\frac{\pi}{2}} erf\left(\frac{m_e}{\sqrt{2}\sigma_u} \right) + C_1 \sigma_u e^{\frac{-m_e^2}{2\sigma_u^2}} + \sum_{i=2}^{N} C_i H_{i-1}(-m_e) e^{\frac{-m_e^2}{2\sigma_u^2}} \right]. \tag{3.49}$$

A complete derivation of this expression for m_y can be found in Appendix A.3. Again, in practical situations, it so happens that C_1 is approximately zero, leading to the simplified equation

$$m_y = erf\left(\frac{m_e}{\sqrt{2}\sigma_u} \right) + e^{\frac{-m_e^2}{2\sigma_u^2}} \frac{2}{\sqrt{2\pi}} \sum_{i=2}^{N} C_i H_{i-1}(-m_e). \tag{3.50}$$

As in the case of the existing statistical technique, m_y can be replaced by m_u. However, due to the complexity of Eqn. 3.50, it is very difficult to solve for m_e in terms of m_u analytically. The easiest approach to this problem is to solve for m_e through an iterative optimization technique, e.g. by using the interval halving optimization (Ravindran et. al., [27]). In this way, let

$$\alpha_i = \frac{m_u - erf\left(\frac{m_{ei}}{\sqrt{2}\sigma_u} \right)}{\frac{2}{\sqrt{2\pi}} \sum_{i=2}^{N} C_i H_{i-1}(-m_e)} = e^{\frac{-m_{ei}^2}{2\sigma_u^2}}. \tag{3.51}$$

Then

$$m_{ei} = \sqrt{-2\sigma_u^2 ln(\alpha_i)}. \tag{3.52}$$

From Eqn. 3.52, it is observed that $\alpha_{min} = \alpha_i \approx 0$ and $\alpha_{max} = \alpha_i \approx 1$, making it possible to calculate m_{e_a} and m_{e_b}. Then, the interval length L can be defined in accordance with $L = m_{e_b} - m_{e_a}$. In this way, one can proceed to calculate $m_{e_0} = (m_{e_b} + m_{e_a})/2$, $m_{e_1} = m_{e_a} + L/4$, and $m_{e_2} = m_{e_b} - L/4$, leading to the determination of α_0, α_1, and α_2 in Eqn. 3.51. In this process, if α_0 is greater than α_1, then set $m_{e_b} = m_{e_0}$ and $m_{e_0} = m_{e_1}$. Otherwise, if α_0 is greater than α_2, then set $m_{e_a} = m_{e_0}$ and $m_{e_0} = m_{e_2}$, and else, if α_0 is less than α_2, then set $m_{e_a} = m_{e_1}$ and $m_{e_b} = m_{e_2}$. Subsequently re-calculate the interval length L, m_{e_1} and m_{e_2}, and repeat the process. Once the interval length L has become sufficiently small, one can terminate the process by setting $m_e = m_{e_0}$.

Having determined m_e, one can invoke its value in Eqn. 3.48 to obtain a corresponding value for k. Moreover, having determined k, one can invoke its value in Eqn. 3.21 to obtain σ_N^2. Finally, having determined σ_N^2, one can invoke its value in Eqn. 3.16 to obtain NPG. In this way, a value for NPG can be obtained for a corresponding value of m_u, and a graphical representation of NPG versus m_u can be obtained.

3.6 Demonstration of the Accuracy of the Proposed Statistical Approach

This section is concerned with an investigation of the improvements achieved by using the proposed statistical approach over the hitherto statistical technique. The starting point in this investigation is an actual (nonlinear) Matlab simulation of the 6-th order COI Σ-Δ A/D converter in Section 3.4 in order to determine the relationships between k and m_u on the one hand, and between NPG and m_u on the other. Recall that the COI A/D converter was designed with an $NPG_{min} = 2.3139$ and was unstable with a DC input amplitude of 0.41. These relationships will then be obtained by employing the hitherto statistical technique and the proposed statistical approach. The results obtained using the two statistical techniques will then be compared to the Matlab simulation results.

Fig. 3.12 shows the relationship between k and m_u with particulars as indicated in the following:

Curve A: Obtained through Matlab simulation,

Curve B: Obtained by employing Eqn. 3.33 of the hitherto statistical technique, and

Curves C and D: Obtained by employing Eqn. 3.48 [3] of the proposed statistical approach for $N = 6$ and $N = 20$, respectively.

The moments of the quantizer input signal, which are required in the Gram-Charlier series, were obtained through (nonlinear) Matlab simulation of the A/D converter. A Matlab simulation is required as no analytic technique for the estimation of the moments exists at present for higher-order Σ-Δ A/D converters. For the case of the first and second-order Σ-Δ A/D converters, the moments of

[3] Using the optimization technique outlined in the previous section.

the quantizer input signal may be approximated very accurately as detailed in Appendices B.2 and B.3. As is evident from Fig. 3.12, the result obtained from the hitherto statistical technique differs substantially from the Matlab simulation result, whereas, the result obtained from the proposed statistical approach more closely approximates the Matlab simulation result. It is also evident that a more accurate result may be obtained in the proposed statistical approach by increasing the number of terms N in the Gram-Charlier series approximation. Choosing $15 < N < 30$ is usually sufficient for an accurate approximation of the quantizer input signal distribution.

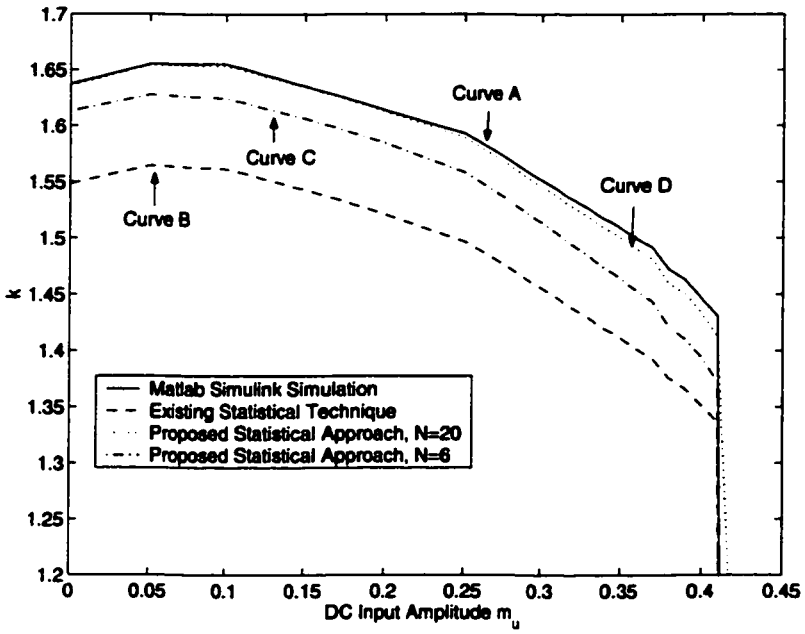

Figure 3.12: Comparison of k versus m_u Curves

Fig. 3.13 shows the relationship between NPG and m_u with particulars as indicated in the following:

Curve A: Obtained through Matlab simulation,

Curve B: Obtained by employing Eqn. 3.35 of the hitherto statistical technique, and

Curves C and D: Obtained by employing Eqn. 3.48 of the proposed approach using Eqns. 3.21 and 3.16 as described in the previous section for $N = 6$ and $N = 20$, respectively.

From Fig. 3.13, the difference between the result obtained through the hitherto statistical technique and the result obtained using Matlab simulation leads to a mean squared error of 0.4070. Figure 3.14 shows a more detailed plot of the NPG versus m_u curve. The most important error is at the instability point $m_u = 0.41$, where the Matlab simulation result falls below NPG_{min}, whereas the result obtained through the hitherto statistical technique maintains its value. The estimation of the noise power gain from the proposed statistical approach (for $N = 20$) differs from the Matlab simulation result by a mean squared error of 0.0857, indicating an improvement of 80% as compared to the hitherto statistical technique. Furthermore, the proposed statistical approach successfully

predicts the instability point found at $m_u = 0.41$. Investigations into other feedforward and multiple-feedback A/D converters have resulted in similar improvements.

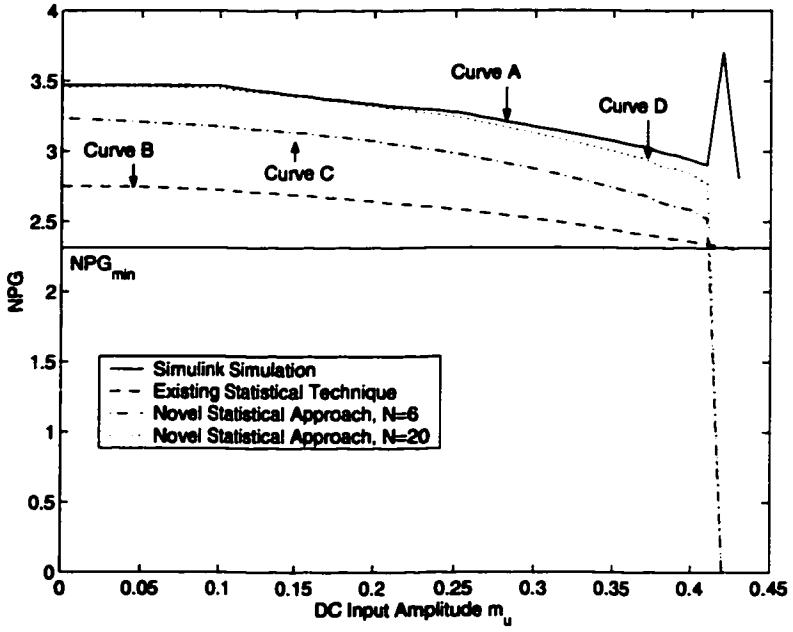

Figure 3.13: Comparison of NPG versus m_u Curves

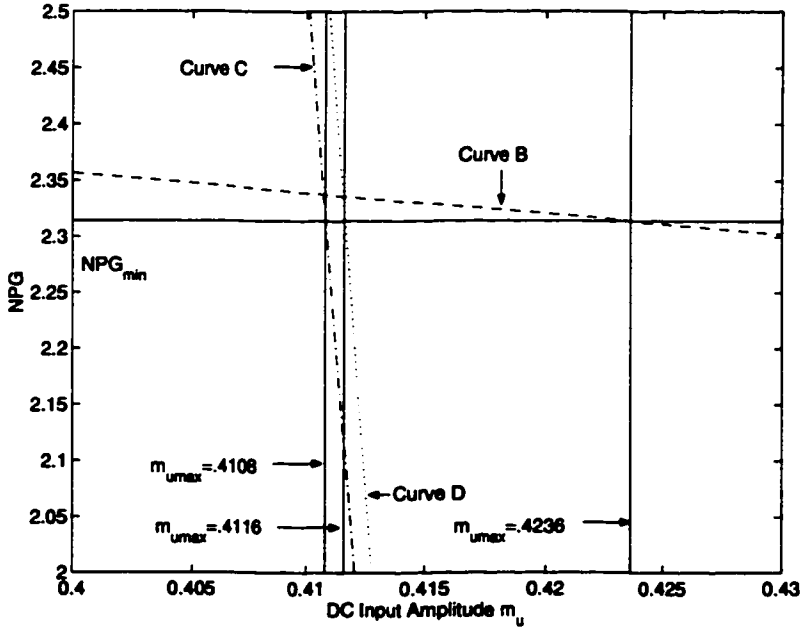

Figure 3.14: Detailed Comparison of NPG versus m_u Curves

3.7 Concluding Remarks

This chapter has presented a detailed step-by-step procedure for the design and realization of five feedforward and multiple-feedback Σ-Δ A/D converter configurations. An empirical investigation and Monte-Carlo analysis of the feedforward and multiple-feedback oversampled Σ-Δ A/D converters for corresponding switched-capacitor (SC) hardware implementations has been performed. This investigation has included the determination of the impact of the complementarity of the signal and noise transfer functions and the relative position of the noise transfer function zeros with respect to unit-circle on the achievable $SQNR$ and on the stability of the Σ-Δ A/D converters. It has been shown that A/D converters having noise transfer function zeros on the unit-circle exhibit superior performance in terms of the achievable $SQNR$, regardless of whether the noise transfer function zeros are located on the unit-circle by the A/D converter configuration proper or by numerical optimization. However, it has been shown that if the noise transfer function zeros are located on the unit-circle by numerical optimization, then the Σ-Δ A/D converter exhibits a high level of stability at low capacitor mismatches, but that the A/D converter becomes highly prone to instability as the capacitor mismatches are increased. The A/D converters which guarantee the location of the noise transfer function zeros on the line $Re(z) = 1$ have shown low sensitivity to capacitor mismatches in terms of the number of unstable samples produced as a function of capacitor mismatches. It has been observed that the main advantage of the complementarity of the signal and noise transfer functions is the reduction in the complexity of the design and optimization of the Σ-Δ A/D converter.

A hitherto statistical approach for the estimation the maximum DC input signal for stable converter operation has been reviewed and extended to the case of arbitrary quantizer input signal distributions. The proposed statistical approach employs Gram-Charlier series to model the distribution of the quantizer input signal. A typical application example has been given demonstrating that the proposed statistical approach leads to an 80% increase in the accuracy of estimating the noise power gain as compared to the hitherto statistical technique. This in turn gave rise to an improved accuracy in the estimation of the maximum DC input signal amplitude for stable A/D converter operation.

Chapter 4

A Novel Class of Highly Stable High-Resolution Σ-Δ A/D Converters

4.1 Introduction

The previous two chapters dealt with the characterization, design, and investigation of five widely used hitherto feedforward and multiple-feedback Σ-Δ A/D converter configurations. The present chapter is concerned with the development of novel Σ-Δ A/D converter configurations capable of realizing magnitude-squared and magnitude complementary signal and noise transfer functions (in addition to being capable of realizing complementary signal and noise transfer functions). The resulting Σ-Δ A/D converters embody three important practical advantages as compared to the hitherto feedforward and multiple-feedback A/D converters, including a) their noise transfer function can be obtained without any recourse to numerical optimization, simplifying the design process, b) their noise transfer function is guaranteed to be bounded below 1, resulting in a highly stable A/D converter operation, and c) in the signal band, where the magnitude of the signal transfer function is 1, the magnitude of their noise transfer function is automatically 0 resulting in high $SQNR$ in an actual (nonlinear) converter operation.

Section 4.2 presents a method for obtaining magnitude-squared complementary or magnitude complementary signal and noise transfer functions $STF(z)$ and $NTF(z)$. Section 4.3 presents five novel Σ-Δ A/D converter configurations capable of realizing magnitude-squared and magnitude complementary signal and noise transfer functions. A systematic procedure is given in Section 4.4 for the design of the proposed magnitude-squared and magnitude complementary Σ-Δ A/D converters. Section 4.5 presents the practical advantages of the proposed Σ-Δ A/D converter configurations. Finally, the main conclusions of the chapter are given in Section 4.6.

4.2 Magnitude-Squared Complementary and Magnitude Complementary Transfer Functions

Let us consider a rational transfer function $H(z)$ of order N, where N is odd for lowpass (or highpass) $H(z)$, and where N is even for bandpass (or bandstop) $H(z)$. Moreover, let $H(z)$ satisfy a relationship of the form (Nowrouzian et. al., [28]), (Nowrouzian et. al., [29])

$$4H(z)H(z^{-1}) = \frac{1}{1 - \left[\frac{P(z)}{Q(z)}\right]^2} \tag{4.1}$$

where $P(z)$ is an antisymmetric polynomial, and $Q(z)$ is a symmetric polynomial in z. In addition, let z_{1i_1} (for $i_1 = 1, 2, \cdots, n_1$) denote those roots of

$$P(z) + Q(z) = 0, \tag{4.2}$$

which are inside the unit circle, and let z_{2i_2} (for $i_2 = 1, 2, \cdots, n_2 = N - n_1$) denote those roots which are outside the unit circle. Then, form the polynomials $P_1(z)$, $Q_1(z)$, and $P_2(z)$, $Q_2(z)$ in accordance with

$$P_1(z) + Q_1(z) = \prod_{i_1=1}^{n_1} (z - z_{1i_1}) \tag{4.3}$$

and

$$P_2(z) + Q_2(z) = \prod_{i_2=1}^{n_2} (z - z_{2i_2}^{-1}) \tag{4.4}$$

where $P_1(z)$, $P_2(z)$ are antisymmetric polynomials, and $Q_1(z)$, $Q_2(z)$ are symmetric polynomials in z. Finally, let $H_1(z)$ and $H_2(z)$ be all-pass transfer functions formed in accordance with (Nowrouzian et. al., [28]), (Nowrouzian et. al., [29])

$$H_1(z) = \frac{1 - \frac{Z_1(z)}{R}}{1 + \frac{Z_1(z)}{R}}, \quad H_2(z) = \frac{1 - \frac{Z_2(z)}{R}}{1 + \frac{Z_2(z)}{R}} \tag{4.5}$$

where

$$\frac{Z_1(z)}{R} = \frac{\prod_{i_1=1}^{n_1}(z - z_{i_1 1}) - z^{n_1} \prod_{i_1=1}^{n_1}(z^{-1} - z_{i_1 1})}{\prod_{i_1=1}^{n_1}(z - z_{i_1 1}) + z^{n_1} \prod_{i_1=1}^{n_1}(z^{-1} - z_{i_1 1})} \tag{4.6}$$

$$\frac{Z_2(z)}{R} = \frac{\prod_{i_2=1}^{n_2}(z - z_{i_2 2}^{-1}) + z^{n_2} \prod_{i_2=1}^{n_2}(z^{-1} - z_{i_2 2}^{-1})}{\prod_{i_2=1}^{n_2}(z - z_{i_2 2}^{-1}) - z^{n_2} \prod_{i_2=1}^{n_2}(z^{-1} - z_{i_2 2}^{-1})}. \tag{4.7}$$

Subsequently, a pair of magnitude-squared complementary transfer functions $H_A(z)$ and $H_B(z)$ may be formed in accordance with

$$H_A(z) = \frac{1}{2}[H_1(z) - H_2(z)] \tag{4.8}$$

$$H_B(z) = \frac{1}{2}[H_1(z) + H_2(z)]. \tag{4.9}$$

Moreover, a pair of magnitude complementary transfer functions may be formed in accordance with

$$\tilde{H}_A(z) = H_A(z)^2, \tag{4.10}$$

$$\tilde{H}_B(z) = H_B(z)^2. \tag{4.11}$$

Example:

As an example, consider a 3-rd order highpass elliptic transfer function $H(z)$ defined in accordance with

$$H(z) = \frac{0.746482 - 2.236346z^{-1} + 2.236346z^{-2} - 0.746482z^{-3}}{1 - 2.424510z^{-1} + 1.995130z^{-2} - 0.546015z^{-3}} \tag{4.12}$$

Then, by solving Eqn. 4.1 for $Q(z)$ and $P(z)$ it may be shown that

$$Q(z) = 1.492964 - 4.472691z^{-1} + 4.472691z^{-2} - 1.492964z^{-3} \tag{4.13}$$

$$P(z) = 0.105927 - 0.093624z^{-1} - 0.093624z^{-2} + 0.105927z^{-3} \tag{4.14}$$

$$\tag{4.15}$$

Having found $P(z)$ and $Q(z)$, the roots of $P(z) + Q(z) = 0$ may then be determined and the all-pass transfer functions $H_1(z)$ and $H_2(z)$ may then be determined to be

$$H_1(z) = \frac{-0.368273 + 1.162690z^{-1} - 1.212406z^{-2} + 0.424523z^{-3}}{2 - 5.071994z^{-1} + 4.348849z^{-2} - 1.250723z^{-3}} \tag{4.16}$$

$$H_2(z) = \frac{-0.424523 + 1.212406z^{-1} - 1.162690z^{-2} + 0.368273z^{-3}}{2 - 5.071994z^{-1} + 4.348849z^{-2} - 1.250723z^{-3}} \tag{4.17}$$

The magnitude-squared complementary transfer functions are then formed in accordance with Eqns. 4.8 and 4.9 resulting in

$$H_A(z) = \frac{0.056249 - 0.049716z^{-1} - 0.049716z^{-2} + 0.056249z^{-3}}{1 - 2.535997z^{-1} + 2.174424z^{-2} - 0.625362z^{-3}} \tag{4.18}$$

$$H_B(z) = \frac{0.792796 - 2.375095z^{-1} + 2.375095z^{-2} - 0.792796z^{-3}}{1 - 2.535997z^{-1} + 2.174424z^{-2} - 0.625362z^{-3}}. \tag{4.19}$$

A plot of the magnitude-frequency responses of $H_A(z)$ and $H_B(z)$ are shown in Fig. 4.1. One may note from the figure that the two responses intersect at a magnitude of $\frac{\sqrt{2}}{2}$. Furthermore, by invoking Eqns. 4.18 and 4.19 in Eqns. 4.10 and 4.11, respectively, one may obtain the magnitude complementary transfer functions $\tilde{H}_A(z)$ and $\tilde{H}_B(z)$ having magnitude-frequency responses as shown in Fig. 4.2. In this case, the two transfer functions intersect at a magnitude of $\frac{1}{2}$.

In this way, the signal transfer and noise transfer functions may be obtained as

$$STF(z) = H_A(z) \quad (or \quad \tilde{H}_A(z)), \tag{4.20}$$

$$NTF(z) = H_B(z) \quad (or \quad \tilde{H}_B(z)). \tag{4.21}$$

The resulting signal and noise transfer functions may be decomposed into $N(z)$, $D(z)$, and $S(z)$ in accordance with Eqns. 2.1 (with $G(z) = 1$) and 2.2.

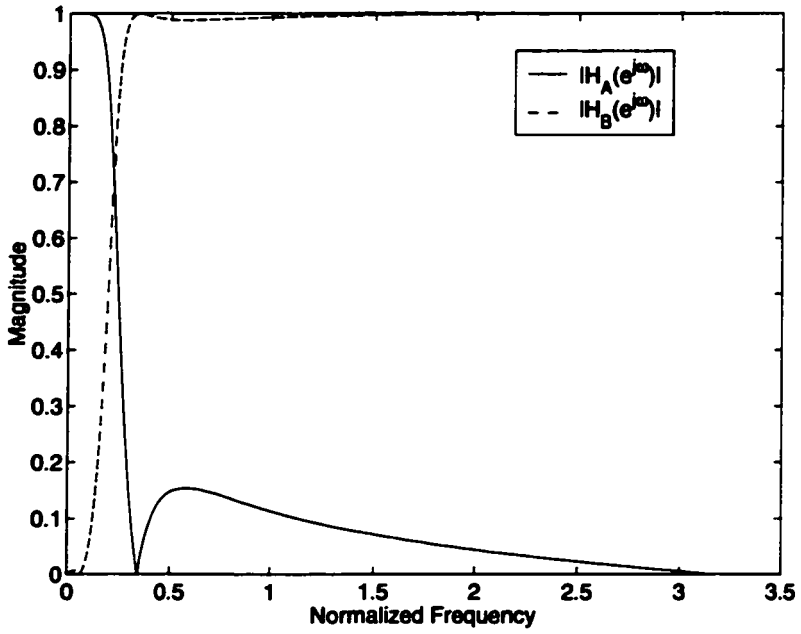

Figure 4.1: Magnitude-Frequency Plot of $H_A(z)$ and $H_B(z)$

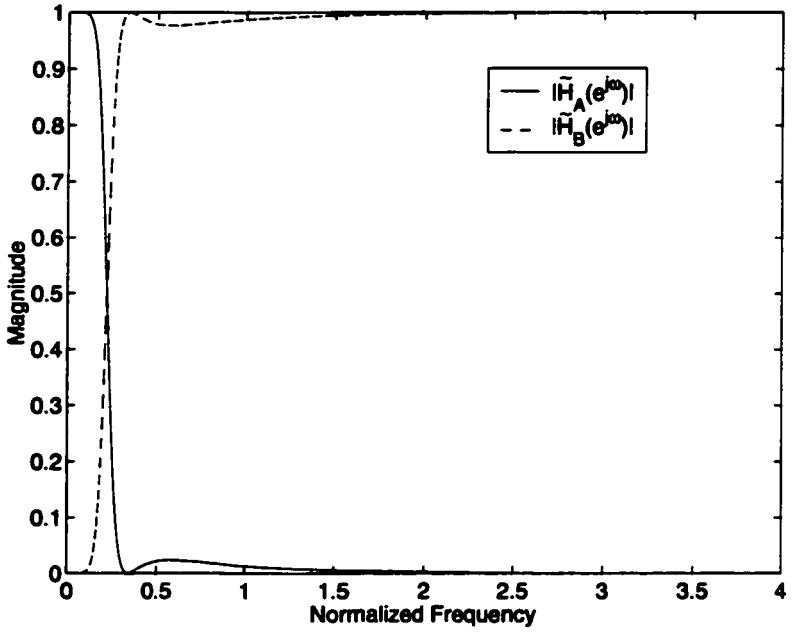

Figure 4.2: Magnitude-Frequency Plot of $\tilde{H}_A(z)$ and $\tilde{H}_B(z)$

As before, it is expedient to recast the polynomial $D(z)$ in the form

$$D(z) = \mathcal{Z}'\mathcal{D}, \tag{4.22}$$

and the polynomials $N(z)$ and $S(z)$ in the forms

$$N(z) = \mathcal{Z}'\mathcal{N}, \tag{4.23}$$

$$S(z) = \mathcal{Z}'\mathcal{S}, \tag{4.24}$$

where $\mathcal{Z}' = [z^0, z^{-1}, z^{-2}, \cdots, z^{-N}]$, where $\mathcal{D}$, $\mathcal{N}$, and $\mathcal{S}$ are column vectors of length $(N+1)$ whose entries depend on the system parameters of the Σ-Δ A/D converter, and where N is the order of the A/D converter.

In the hitherto feedforward and multiple-feedback Σ-Δ A/D converters, the configuration proper imposes two restricting conditions on the signal and noise transfer functions, namely 1) the z^0 coefficient of $S(z)$ must be zero and 2) the z^0 coefficient of $N(z)$ must be unity. However, magnitude-squared or magnitude complementary signal and noise transfer functions require that the z^0 coefficient of $S(z)$ be non-zero and that the z^0 coefficient of $N(z)$ be unconstrained.

In this thesis, five novel Σ-Δ A/D converter configurations are proposed which do not make any recourse to the above problem. This is achieved through suitable modifications of the hitherto cascade-of-integrators (COI), cascade-of-resonators (COR), cascade-of-resonators/integrators (CRI), feedforward (FF), and multiple-feedback (MF) Σ-Δ A/D converter configurations.

4.3 Proposed Σ-Δ A/D Converter Configurations

4.3.1 Modified Cascade-of-Integrators Σ-Δ A/D Converter Configuration

The modified cascade-of-integrators (MCOI) Σ-Δ A/D converter configuration is as shown in Fig. 4.3 (Fraser et. al., [30]). The modification includes the addition of $(N+1)$ multipliers in the feedforward path and the addition of 1 multiplier after the quantizer.

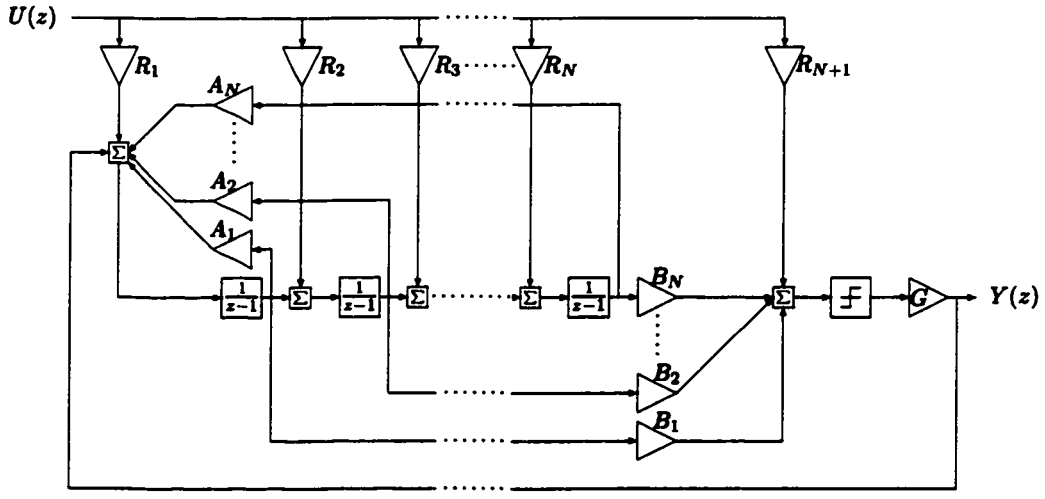

Figure 4.3: Modified Cascade-of-Integrators Σ-Δ A/D Converter Configuration

As before, it is necessary to be able to determine the multiplier values of the configuration given a

signal and noise transfer function. Through a detailed analysis of this A/D converter configuration, the G multiplier coefficient corresponds directly to the z^0 coefficient of $N(z)$ as is evident from

$$N(z) = \frac{G}{z^N}\left[(z-1)^N - \sum_{i=1}^{N} A_i(z-1)^{N-i}\right]. \tag{4.25}$$

Next, to determine the multiplier coefficients A_{1-N}, B_{1-N}, and $R_{1-(N+1)}$, it is convenient to let

$$\mathcal{A} = [1\ A_1\ A_2 \cdots A_N],$$
$$\mathcal{B} = [1\ B_1\ B_2 \cdots B_N],$$
$$\mathcal{R} = [R_1\ R_2 \cdots R_{N+1}].$$

Then, it can be shown that

$$\mathcal{N} = \mathcal{C}_{MCOI1}\mathcal{A}G, \tag{4.26}$$
$$\mathcal{D} = \mathcal{C}_{MCOI2}\mathcal{B}, \tag{4.27}$$
$$\mathcal{S} = \mathcal{C}_{MCOI3}\mathcal{R}G, \tag{4.28}$$

where $\mathcal{C}_{MCOI1}$ is a lower triangular matrix of order $(N+1)$ whose elements are independent of the A multiplier coefficients, $\mathcal{C}_{MCOI2}$ is a lower triangular matrix of order $(N+1)$ whose elements depend solely on the A and G multiplier coefficients, and $\mathcal{C}_{MCOI3}$ is a matrix of order $(N+1)$ whose elements are solely dependent on the A and B multiplier coefficients. For example, by considering the case of $N = 3$, one has

$$\mathcal{C}_{MCOI1} = \begin{bmatrix} 1 & 0 & 0 & 0 \\ -3 & -1 & 0 & 0 \\ 3 & 2 & -1 & 0 \\ -1 & -1 & 1 & -1 \end{bmatrix} \tag{4.29}$$

$$\mathcal{C}_{MCOI2} = \begin{bmatrix} 1 & 0 & 0 & 0 \\ -3 - A_1 & -G & 0 & 0 \\ 3 + 2A_1 - A_2 & 2G & -G & 0 \\ -1 - A_1 + A_2 - A_3 & -G & G & -G \end{bmatrix} \tag{4.30}$$

$$C_{MCOI3} = \left[\begin{array}{ccc|c} 0 & 0 & 0 & \\ & & & \\ B_1 & B_2 & B_3 & \\ & & & \\ 2B_1+B_2 & B_3-B_2(2+A_1) & -B_3(2-A_1) & \\ & +B_1A_2 & +B_1A_3 & C_{\cdot 1} \\ & & & \\ B_1-B_2 & -B_3(1+A_1) & B_3(1-A_2+A_1) & \\ +B_3 & +B_2(1+A_1) & +B_2A_3+B_1A_3 & \\ & +B_1(A_3-A_2) & & \end{array}\right] \tag{4.31}$$

where $C_{\cdot 1}$ represents the first column of the matrix C_{MCOI2}.

In this way, once $\mathcal{N}$, $\mathcal{D}$, and $\mathcal{S}$ have been obtained, the coefficient G may be obtained from $\mathcal{N}$, and the multiplier coefficients $\mathcal{A}$, $\mathcal{B}$, and $\mathcal{R}$ may be obtained through the inversion of Eqns. 4.26, 4.27, and 4.28, respectively.

Also, as before, the SC hardware implementation may be obtained by first sectioning the configuration into its primary components then substituting these components in terms of their corresponding SC hardware counterparts shown in Fig. 2.4. In doing so, for a 6-th order MCOI converter configuration, one arrives at the corresponding SC hardware implementation shown in Fig. 4.5. It is convenient to factor out the CR_{N+1} and G coefficients to obtain the equivalent system shown in Fig. 4.4, where $M = CR_{N+1}$. The nominal capacitor values are given in Table 4.1.

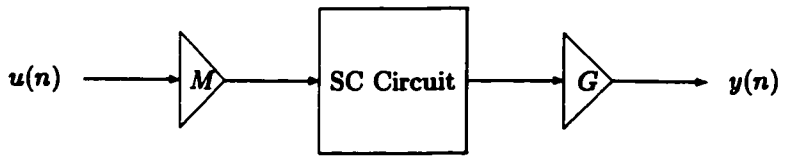

Figure 4.4: Equivalent SC system

4.3.2 Modified Cascade-of-Resonators Σ-Δ A/D Converter Configuration

The modified cascade-of-resonators (MCOR) configuration is as shown in Fig. 4.6 (Fraser et. al., [31]). The modification includes the addition of 1 feedforward multiplier and the addition of 1 multiplier after the quantizer.

Through a detailed analysis of this A/D converter configuration it can be shown that

$$N(z) = G \prod_{k=1}^{\lfloor \frac{N}{2} \rfloor} \left[1 + (-2 - R_k)z^{-1} + z^{-2}\right]. \tag{4.32}$$

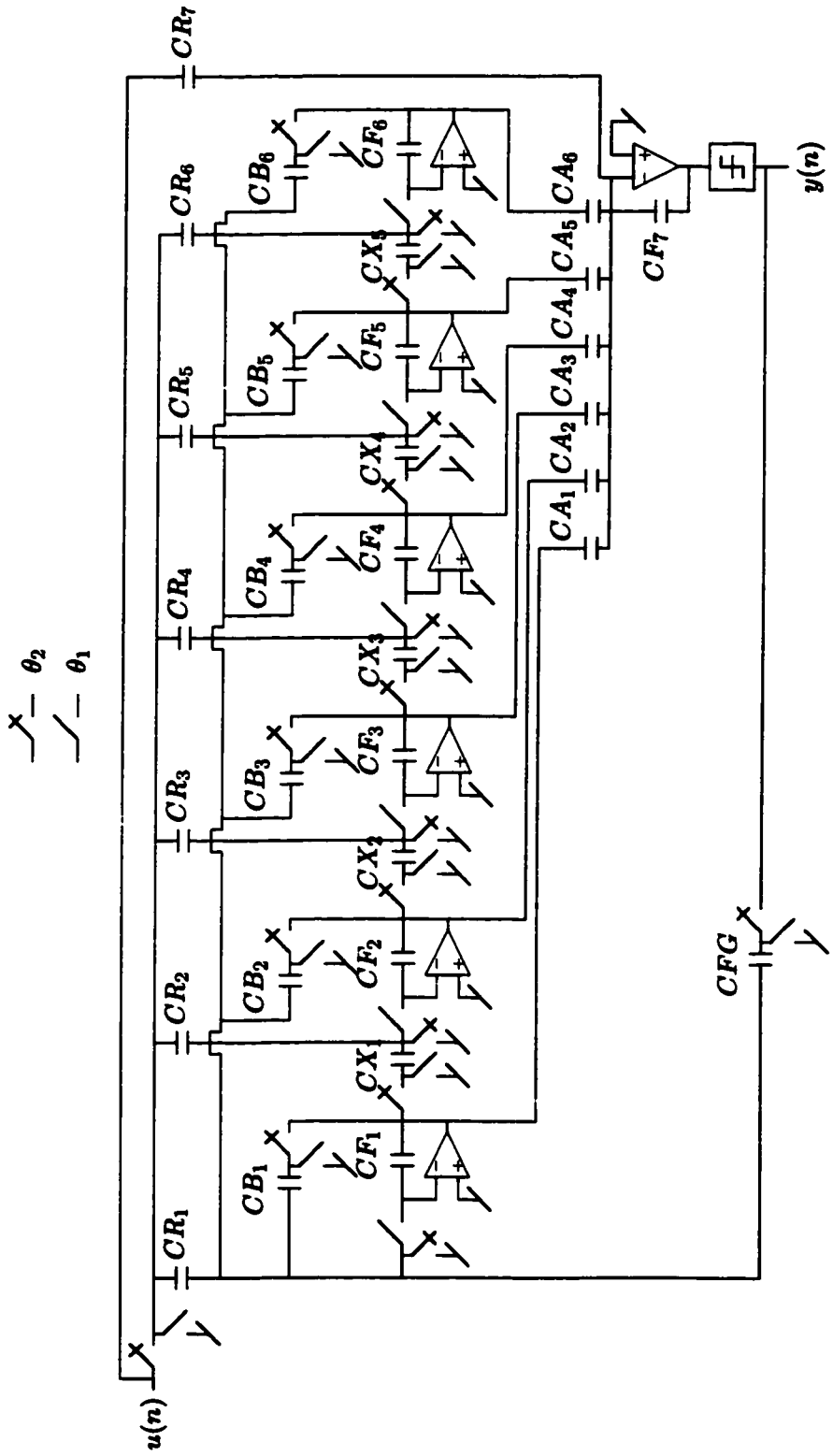

Figure 4.5: Modified Cascade-of-Integrators SC Hardware Implementation

Table 4.1: Modified Cascade-of-Integrators Nominal Capacitor Values

CR_1	R_1/R_{N+1}	CA_1	$-A_1$	CB_1	B_1
CR_2	R_2/R_{N+1}	CA_2	$-A_2$	CB_2	B_2
$\vdots$	$\vdots$	$\vdots$	$\vdots$	$\vdots$	$\vdots$
CR_{N+1}	1	CA_N	$-A_N$	CB_N	B_N
CF_1	1	CX_1	1		
CF_2	1	CX_2	1		
$\vdots$	$\vdots$	$\vdots$	$\vdots$	$\vdots$	$\vdots$
CF_{N+1}	-1	CX_{N-1}	1	CFG	G

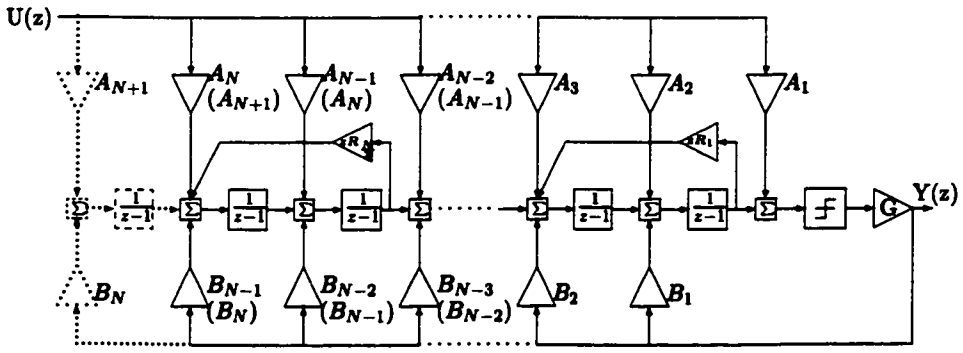

Figure 4.6: Modified Cascade-of-Resonators Σ-Δ A/D Converter Configuration

The above equations reveal that the A/D converter configuration automatically places the zeros of $NTF(z)$ on the unit-circle. Evidently, the zeros of $NTF(z)$ depend on the values of multiplier coefficients R_k (for $k = 1, 2, \ldots, \frac{N}{2}$) only.

Given the signal and noise transfer functions, the coefficient G may be obtained as the z^0 coefficient of $N(z)$ (c.f. Eqn. 4.32), and the coefficients $R_{1-\lfloor N/2 \rfloor}$ may be obtained from Eqn. 2.26 using the zero frequencies f_0 of $N(z)$. Further analysis of the MCOR Σ-Δ A/D converter configuration reveals that the A_{1-N} and B_{1-N} coefficients may be obtained as discussed in the following.

First, let $\mathcal{A}^T = [A_1, A_2, \cdots, A_{N+1}]$ and $\mathcal{B}^T = [1, B_1, \cdots, B_N]$. Then it can be shown that

$$\mathcal{S} = \mathcal{C}_{1MCOR}\mathcal{A}, \tag{4.33}$$

and

$$\mathcal{D} = \mathcal{C}_{2MCOR}\mathcal{B}, \tag{4.34}$$

where $\mathcal{C}_{1MCOR}$ and $\mathcal{C}_{2MCOR}$ are lower triangular matrices of order $(N+1)$ having elements as being independent of the multiplier coefficients A_k and B_k, respectively[1]. As an example, consider the case when $N = 3$. Then,

$$\mathcal{C}_{1MCOR} = \begin{bmatrix} 1 & 0 & 0 & 0 \\ -(R_1+3) & 1 & 0 & 0 \\ (R_1+3) & -2 & 1 & 0 \\ -1 & 1 & -1 & 1 \end{bmatrix} \tag{4.35}$$

$$\mathcal{C}_{2MCOR} = \begin{bmatrix} 1 & 0 & 0 & 0 \\ -(R_1+3) & -G & 0 & 0 \\ (R_1+3) & 2G & -G & 0 \\ -1 & -G & G & -G \end{bmatrix} \tag{4.36}$$

$$\tag{4.37}$$

In this way, once $\mathcal{N}$, $\mathcal{D}$, and $\mathcal{S}$ have been obtained, the coefficient G and $\mathcal{R}$ may be obtained from $\mathcal{N}$, and the multiplier coefficients, $\mathcal{A}$, and $\mathcal{B}$ may be obtained through the inversion of Eqns. 4.33, 4.34, respectively.

The corresponding SC hardware implementation can once again be obtained by decomposing the converter configuration into its primary components and then replacing those components by their SC capacitor hardware counterparts. As a result, the MCOR SC hardware implementation is as shown in Fig. 4.7 for the case of a 6-th order converter. Moreover, it is convenient to factor out the G coefficient to obtain the equivalent system as shown in Fig. 4.4, where $M = 1$. The nominal capacitor values are given in Table 4.2.

[1]The elements depend solely on the multiplier coefficients R_k and G.

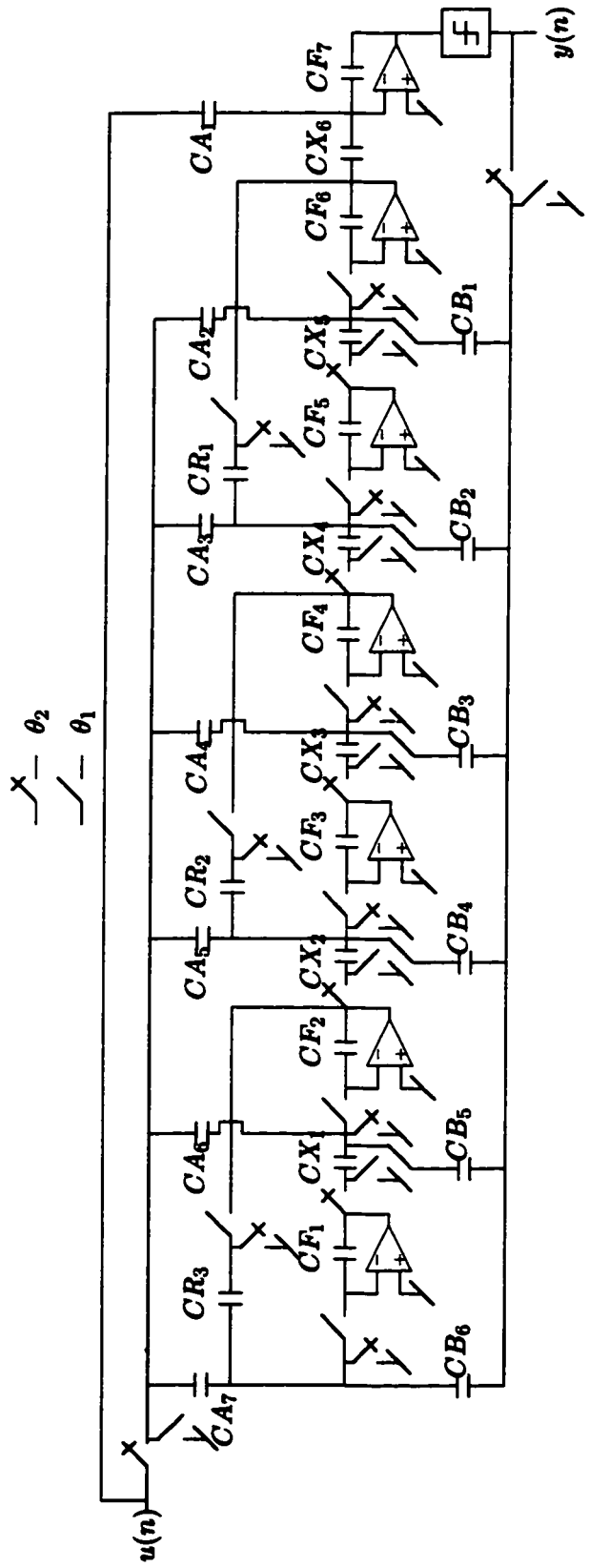

Figure 4.7: Modified Cascade-of-Resonators SC Hardware Implementation

Table 4.2: Modified Cascade-of-Resonators Nominal Capacitor Values

CA_1	A_1	CB_1	B_1G	CF_1	1
CA_2	A_2	CB_2	B_2G	CF_2	1
$\vdots$	$\vdots$	$\vdots$	$\vdots$	$\vdots$	$\vdots$
CA_{N+1}	A_{N+1}	CB_N	B_NG	CF_{N+1}	1
CX_1	1	CR_1	$-R_1$		
CX_2	1	CR_2	$-R_2$		
$\vdots$	$\vdots$	$\vdots$	$\vdots$		
CX_N	1	$CR_{\lfloor \frac{N}{2} \rfloor}$	$-R_{\lfloor \frac{N}{2} \rfloor}$		

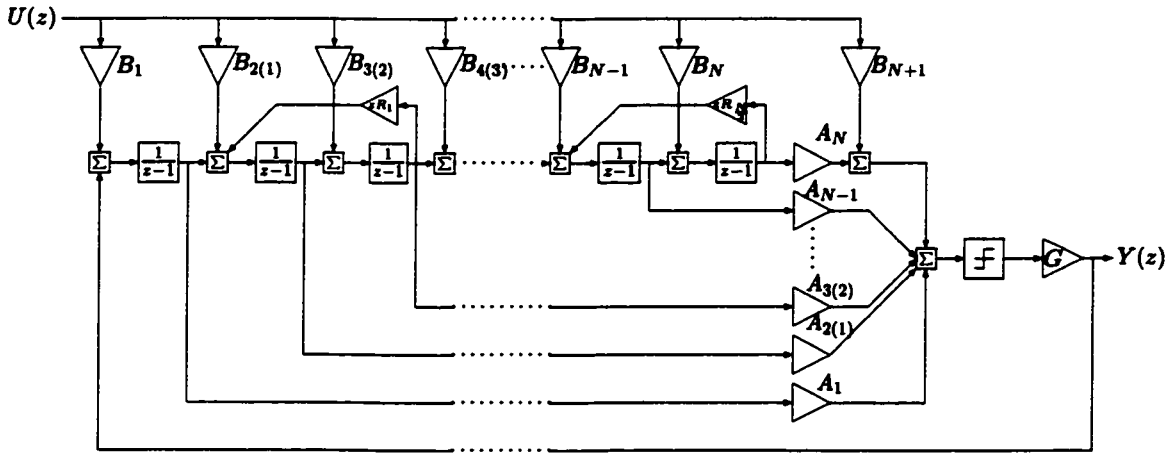

Figure 4.8: Modified Cascade-of-Resonators/Integrators Σ-Δ A/D Converter Configuration

4.3.3 Modified Cascade-of-Resonators/Integrators Σ-Δ A/D Converter Configuration

The modified cascade-of-resonators/integrators (MCRI) is as shown in Fig. 4.8. The modification of the CRI A/D converter includes the addition of $(N+1)$ multiplier coefficients in the feedforward path and the addition of 1 multiplier after the quantizer.

Having obtained the signal and noise transfer function, the multiplier coefficients G, $R_{1-\lfloor N/2 \rfloor}$, A_{1-N}, and $B_{1-(N+1)}$ may be determined as discussed in the following.

First, an analysis of this A/D converter reveals that,

$$N(z) = G \prod_{k=1}^{\frac{N}{2}} \left[1 + (-2 - R_k)z^{-1} + z^{-2}\right]. \tag{4.38}$$

Evidently, the G multiplier corresponds directly to the z^0 coefficient of $N(z)$, and the multipliers $R_{1-\lfloor N/2 \rfloor}$ may be determined from the zero frequencies f_0 of the noise transfer function in accordance

with Eqn. 2.26. Next, it is convenient to let

$$\mathcal{A} = [1\ A_1\ A_2 \cdots A_N], \tag{4.39}$$

$$\mathcal{B} = [1\ B_1\ B_2 \cdots B_{N+1}], \tag{4.40}$$

Then, it can be shown that

$$\mathcal{D} = \mathcal{C}_{MCRI1}\mathcal{A}, \tag{4.41}$$

$$\mathcal{S} = \mathcal{C}_{MCRI2}\mathcal{B}G, \tag{4.42}$$

where $\mathcal{C}_{MCRI1}$ is a lower triangular matrix of order $(N+1)$ whose elements are independent of the A multiplier coefficients, and $\mathcal{C}_{MCRI2}$ is a matrix of order $(N+1)$ whose elements depend solely on the A and R multiplier coefficients. As an example, by considering the case of $N = 3$, one has

$$\mathcal{C}_{CRI1} = \begin{bmatrix} 1 & 0 & 0 & 0 \\ -(3+R_1) & -G & 0 & 0 \\ 3+R_1 & R_1G & -G & 0 \\ -1 & -G & G & -G \end{bmatrix} \tag{4.43}$$

and

$$\mathcal{C}_{CRI2} = \begin{bmatrix} 0 & 0 & 0 & 1 \\ A_1 & A_2 & A_3 + A_2R_1 & -(3+R_1) \\ -A_1(2+R_1) + A_2 & -2A_2 + A_3 & -A_2R_1 - 2A_3 & 3+R_1 \\ A_1 - A_2 + A_3 & A_2 - A_3 & A_3 & -1 \end{bmatrix}. \tag{4.44}$$

In this way, once $\mathcal{N}$, $\mathcal{D}$, and $\mathcal{S}$ have been obtained, the coefficient G and $\mathcal{R}$ may be obtained from $\mathcal{N}$, and the multiplier coefficients $\mathcal{A}$ and $\mathcal{B}$ may be obtained through the inversion of Eqns. 4.41 and 4.42, respectively.

The corresponding SC hardware implementation is as shown in Fig. 4.9 for the case of a 6-th order MCRI A/D converter and was obtained by replacing the primary blocks of the MCRI configuration by their SC hardware counterparts. It is convenient to factor out the CB_{N+1} and G coefficients to obtain the equivalent system as shown in Fig. 4.4, where $M = CB_{N+1}$. The nominal capacitor values are given in Table 4.3.

4.3.4 Modified Feedforward Σ-Δ A/D Converter Configuration

The next configuration is the modified feedforward Σ-Δ A/D converter as shown in Fig. 4.10. The modification includes the addition of $(N+1)$ feedforward multipliers and the addition of 1 multiplier after the quantizer.

The numerator $N(z)$ of the noise transfer function can be expressed in terms of the G and $R_{1-\lfloor N/2 \rfloor}$ multiplier coefficients in accordance with

$$N(z) = G \prod_{k=1}^{\frac{N}{2}} \left[1 - 2z^{-1} + (1 - R_k)z^{-2}\right], \tag{4.45}$$

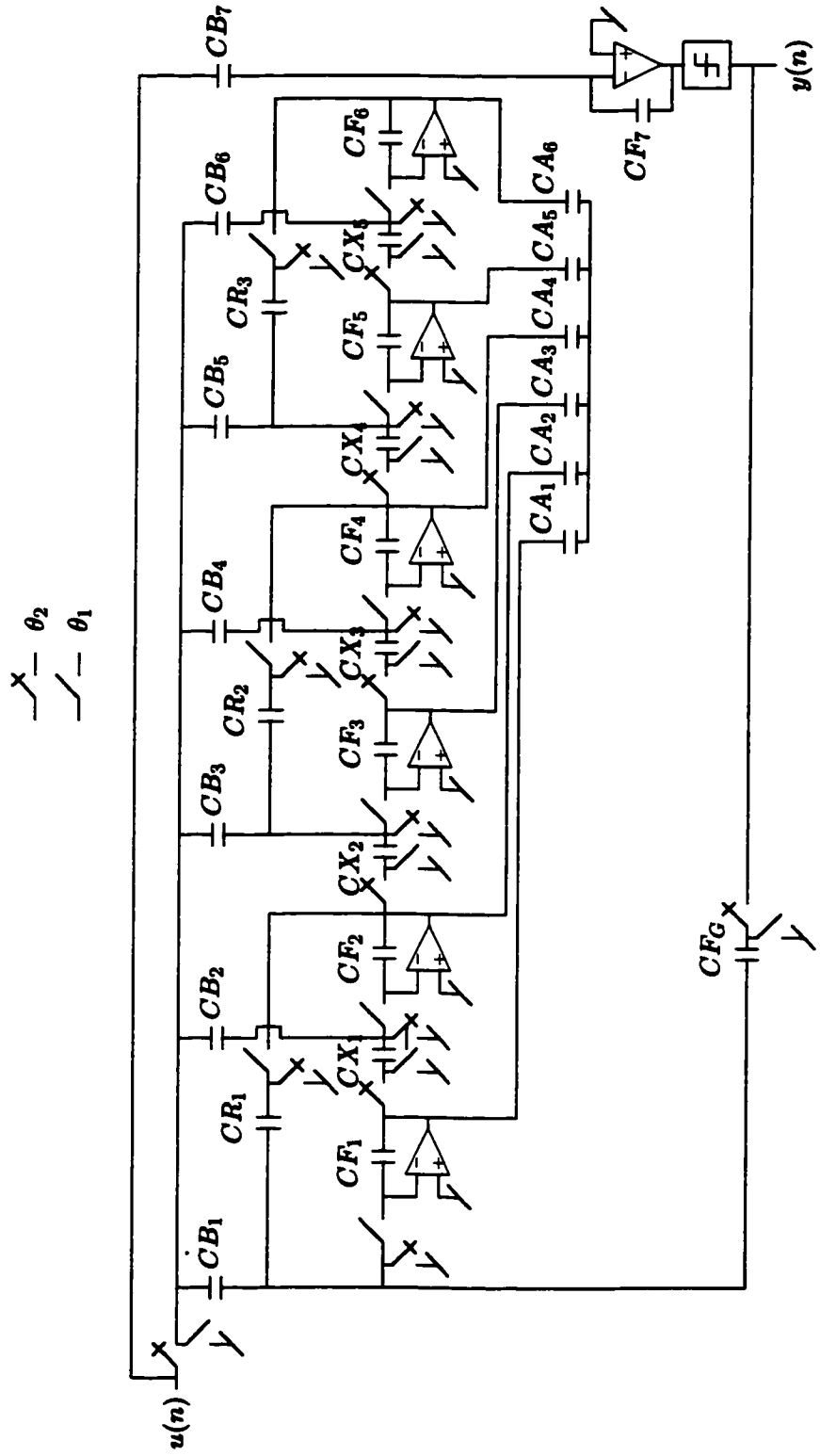

Figure 4.9: Modified Cascade-of-Resonators/Integrators SC Hardware Implementation

Table 4.3: Modified Cascade-of-Resonators/Integrators Nominal Capacitor Values

CB_1	B_1/B_{N+1}	CA_1	A_1	CF_1	1
CB_2	B_2/B_{N+1}	CA_2	A_2	CF_2	1
$\vdots$	$\vdots$	$\vdots$	$\vdots$	$\vdots$	$\vdots$
CB_{N+1}	B_{N+1}/B_{N+1}	CA_N	A_N	CF_{N+1}	-1
CX_1	1	CR_1	$-R_1$		
CX_2	1	CR_2	$-R_2$		
$\vdots$	$\vdots$	$\vdots$	$\vdots$		
CX_{N-1}	1	$CR_{\lfloor \frac{N}{2} \rfloor}$	$-R_{\lfloor \frac{N}{2} \rfloor}$	CFG	G

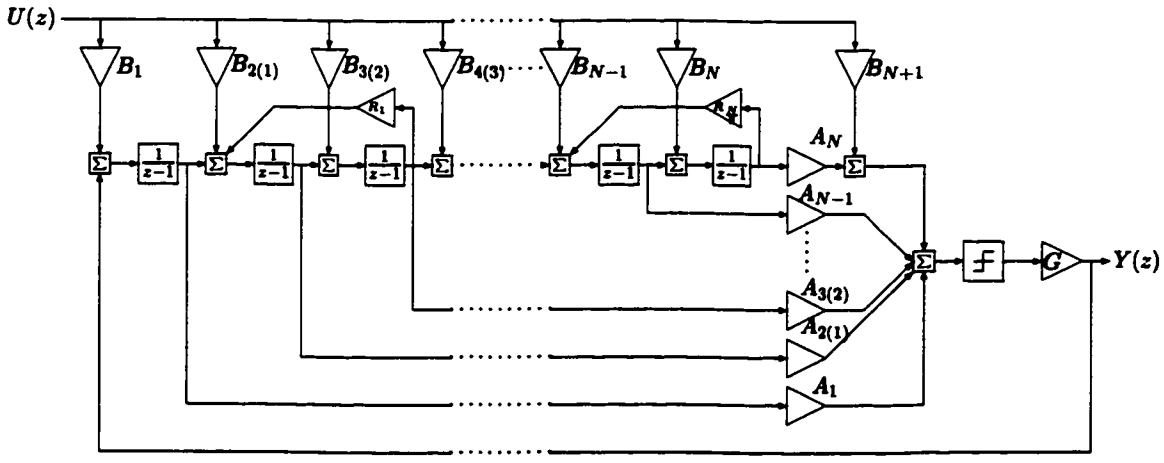

Figure 4.10: Modified Feedforward Σ-Δ A/D Converter Configuration

for even orders N. Evidently, the parameter G corresponds directly to the z^0 coefficient of $N(z)$, and the $R_{1-\lfloor N/2 \rfloor}$ multiplier coefficients may be expressed in terms of the angles of the zeros θ_k of $NTF(z)$ in accordance with

$$R_k = tan^2(\theta_k). \tag{4.46}$$

Then, the multiplier coefficients A_{1-N} and $B_{1-(N+1)}$ may be determined as discussed in the following.

First, is convenient to let

$$\mathcal{A} = [1\ A_1\ A_2 \cdots A_N], \tag{4.47}$$

$$\mathcal{B} = [B_1\ B_2 \cdots B_{N+1}], \tag{4.48}$$

Then, it may be shown that

$$\mathcal{D} = \mathcal{C}_{MFF1}\mathcal{A}^T, \tag{4.49}$$

$$\mathcal{S} = \mathcal{C}_{MFF2}\mathcal{B}^T G, \tag{4.50}$$

where $\mathcal{C}_{MFF1}$ is a lower triangular matrix of order $(N+1)$ whose elements are independent of the A multiplier coefficients, and $\mathcal{C}_{MFF2}$ is a matrix of order $(N+1)$ whose elements depend solely on the A and R multiplier coefficients. As an example, consider the case $N = 3$. Then,

$$\mathcal{C}_{MFF1} = \begin{bmatrix} 1 & 0 & 0 & 0 \\ -3 & -G & 0 & 0 \\ 3 - R_1 & 2G & -G & 0 \\ -1 + R_1 & G(R_1 - 1) & G & -G \end{bmatrix} \tag{4.51}$$

and

$$\mathcal{C}_{MFF2} = \begin{bmatrix} 0 & 0 & 0 & 1 \\ A_1 & A_2 & A_3 & -3 \\ A_2 - 2A_1 & A_3 - 2A_2 & -2A_3 + A_2R_1 & 3 - R_1 \\ A_3 - A_2 + A_1(1 - R_1) & -A_3 + A_2 & A_3 - A_2R_1 & R_1 - 1 \end{bmatrix}. \tag{4.52}$$

In this way, once the vectors $\mathcal{N}$, $\mathcal{D}$, and $\mathcal{S}$ have been obtained, the coefficient G and $\mathcal{R}$ may be obtained from $\mathcal{N}$, and the multiplier coefficients, $\mathcal{A}$ and $\mathcal{B}$ may be obtained through the inversion of Eqns. 4.49 and 4.50, respectively.

The corresponding SC hardware implementation can once again be obtained by decomposing the converter configuration into its primary components and then replacing those components by their SC capacitor hardware counterparts. The resulting SC hardware implementation is as shown in Fig. 4.11 for the case of a 6-th order MFF Σ-Δ A/D converter. It is convenient to factor out the B_{N+1} and G coefficients to obtain the equivalent system as shown in Fig. 4.4, where $M = CB_{N+1}$. The capacitor values are given in Table 4.4.

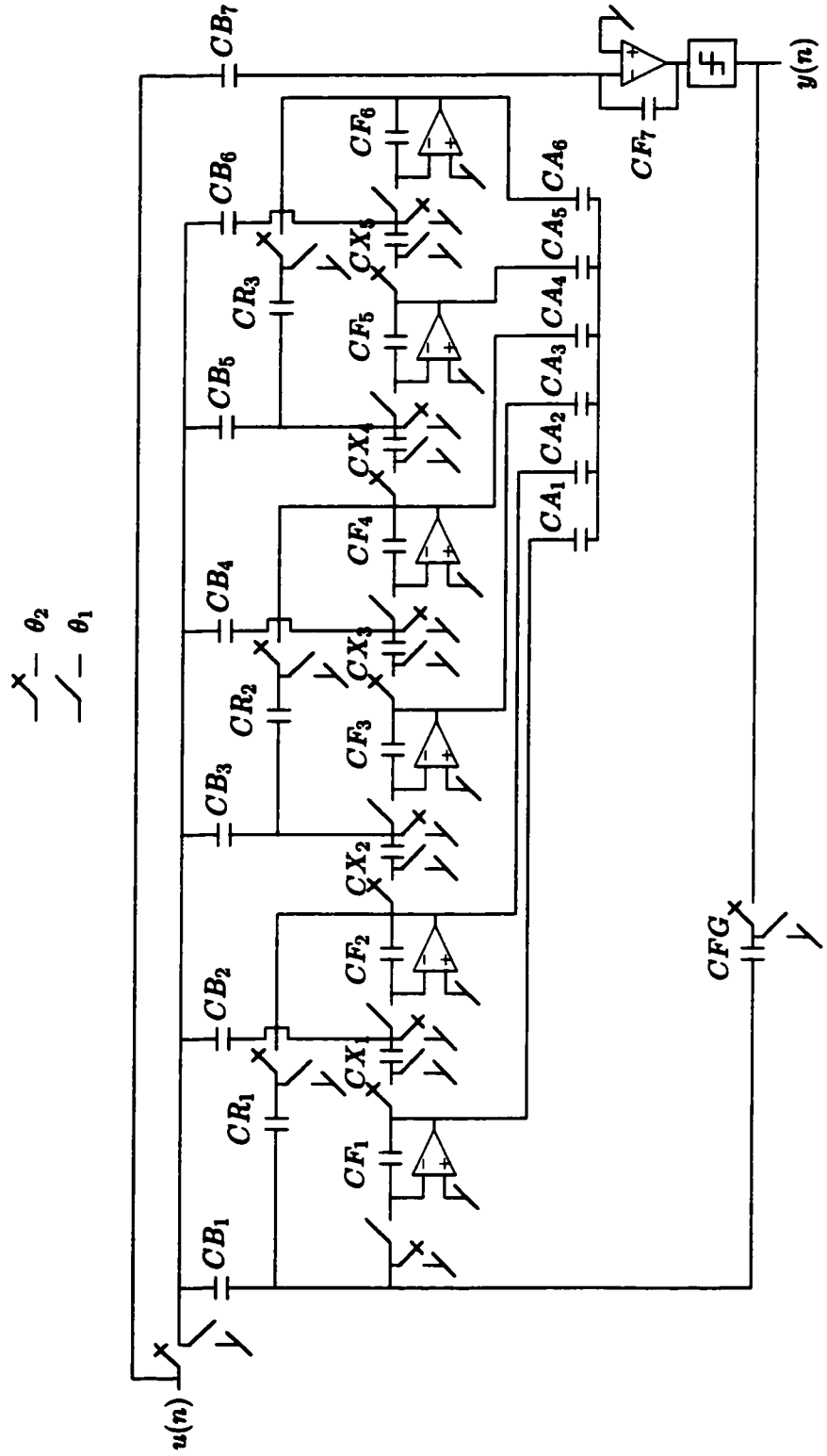

Figure 4.11: Modified Feedforward SC Hardware Implementation

Table 4.4: Modified Feedforward Nominal Capacitor Values

CB_1	B_1	CA_1	A_1	CF_1	1
CB_2	B_2	CA_2	A_2	CF_2	1
$\vdots$	$\vdots$	$\vdots$	$\vdots$	$\vdots$	$\vdots$
CB_{N+1}	B_{N+1}	CA_N	A_N	CF_{N+1}	1
CX_1	1	CR_1	$-R_1$		
CX_2	1	CR_2	$-R_2$		
$\vdots$	$\vdots$	$\vdots$	$\vdots$		
CX_{N-1}	1	$CR_{\lfloor \frac{N}{2} \rfloor}$	$-R_{\lfloor \frac{N}{2} \rfloor}$	CFG	G

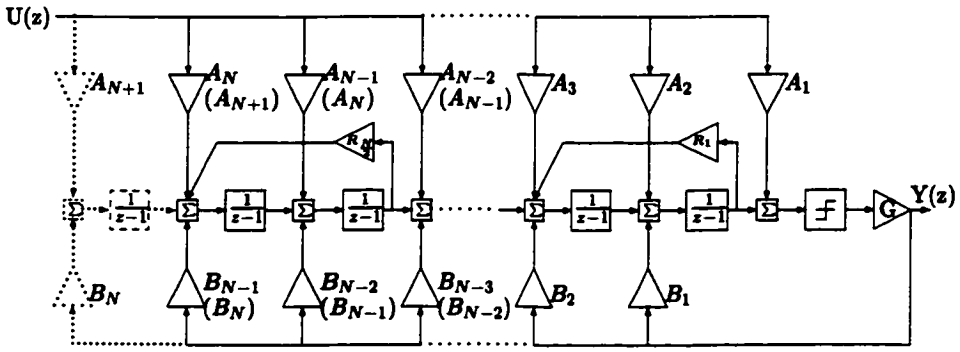

Figure 4.12: Modified Multiple-Feedback Σ-Δ A/D Converter Configuration

4.3.5 Modified Multiple-Feedback Σ-Δ A/D Converter Configuration

The modified multiple-feedback (MMF) Σ-Δ A/D converter configuration is as shown in Fig. 4.12 (Fraser et. al., [32]). The modification includes the addition of N feedforward multipliers and the addition of 1 multiplier after the quantizer. Given a signal and noise transfer function, the constituent parameters of the MMF Σ-Δ A/D converter configuration can be determined as discussed in the following.

First, through a detailed analysis of the A/D converter configuration, the numerator of the noise transfer function can be expressed in terms of the G and R multiplier coefficients in accordance with

$$N(z) = G \prod_{k=1}^{\lfloor \frac{N}{2} \rfloor} \left[1 - 2z^{-1} + (1 - R_k)z^{-2}\right]. \tag{4.53}$$

The above equation reveals that the A/D converter configuration automatically places the zeros of $NTF(z)$ on the real line $Re(z) = 1$. Then, the G coefficient may determined as the z^0 coefficient of $N(z)$, and the R coefficients may be obtained from the angles of the zeros of the noise transfer function in accordance with Eqn. 4.46. Moreover, it may be shown that if $\mathcal{A}^T = [A_1, A_2, \cdots, A_N, A_{N+1}]$

and $\mathcal{B}^T = [1, B_1, \cdots, B_N]$, then

$$\mathcal{S} = \mathcal{C}_{1MMF}\mathcal{A}, \tag{4.54}$$

$$\text{and} \quad \mathcal{D} = \mathcal{C}_{2MMF}\mathcal{B}, \tag{4.55}$$

where $\mathcal{C}_{1MMF}$ and $\mathcal{C}_{2MMF}$ are lower triangular matrices of order $(N+1)$ having elements as being independent of the multiplier coefficients A_k and B_k, respectively[2]. As an example, by considering the case of $N = 3$, one has

$$\mathcal{C}_{MMF1} = \begin{bmatrix} 1 & 0 & 0 & 0 \\ -3 & 1 & 0 & 0 \\ 3 - R_1 & -2 & 1 & 0 \\ -1 + R_1 & 1 & -1 & 1 \end{bmatrix} \tag{4.56}$$

and

$$\mathcal{C}_{MMF2} = \begin{bmatrix} 1 & 0 & 0 & 0 \\ -3 & -G & 0 & 0 \\ 3 - R_1 & 2G & -G & 0 \\ R_1 - 1 & -G & G & -G \end{bmatrix}. \tag{4.57}$$

In this way, once the vectors $\mathcal{N}$, $\mathcal{D}$, and $\mathcal{S}$ have been obtained, the coefficient G and $\mathcal{R}$ may be obtained from $\mathcal{N}$, and the multiplier coefficients $\mathcal{A}$ and $\mathcal{B}$ may be obtained through the inversion of Eqns. 4.54 and 4.55, respectively.

Applying the basic building blocks from Fig. 2.4 to a 6-th order MMF A/D converter, one arrives at the SC hardware implementation shown in Fig. 4.13. Moreover, it is convenient to factor out the G multiplier coefficient to obtain the equivalent system as shown in Fig. 4.4, where $M = 1$. The nominal capacitor values are given in Table 4.5.

Using the above relationships for the various multiplier coefficients, one may proceed to a systematic design of magnitude-squared complementary and magnitude complementary Σ-Δ A/D converters as discussed in the following design procedure.

4.4 Design Procedure

This section presents a systematic procedure for the design of the magnitude-squared and magnitude complementary oversampled Σ-Δ A/D converters starting from a set of high-level system specifications. In the case of lowpass Σ-Δ A/D converters, these specifications include, the sampling frequency f_s, the signal bandwidth BW, the desired $SQNR$, and the order N. These specifications can be extended to the case of bandpass Σ-Δ A/D converters by including the corresponding center frequency associated with the input signal passband.

[2]The elements depend solely on the multiplier coefficients R_k and G.

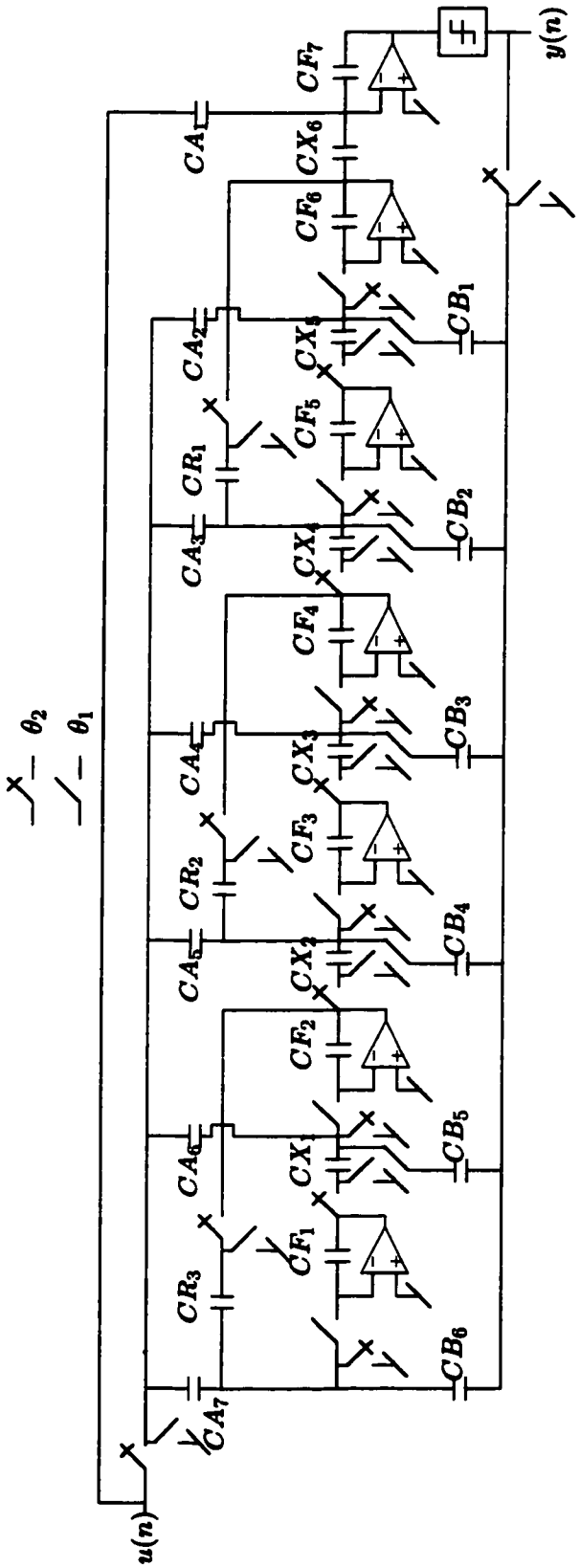

Figure 4.13: Modified Multiple-Feedback SC Hardware Implementation

Table 4.5: Modified Multiple-Feedback Nominal Capacitor Values

CA_1	A_1	CB_1	B_1G	CF_1	1
CA_2	A_2	CB_2	B_2G	CF_2	1
$\vdots$	$\vdots$	$\vdots$	$\vdots$	$\vdots$	$\vdots$
CA_{N+1}	A_{N+1}	CB_N	B_NG	CF_{N+1}	1
CX_1	1	CR_1	$-R_1$		
CX_2	1	CR_2	$-R_2$		
$\vdots$	$\vdots$	$\vdots$	$\vdots$		
CX_N	1	$CR_{\lfloor \frac{N}{2} \rfloor}$	$-R_{\lfloor \frac{N}{2} \rfloor}$		

4.4.1 Design of Magnitude-squared Complementary Σ-Δ A/D Converters

The design of the magnitude-squared complementary Σ-Δ A/D converter proceeds in a step-by-step manner as discussed in the following.

Step 1) Choose $NTF(z)$ to be an odd N-th order highpass transfer function or an even $2N$-th order bandstop classical transfer function [3].

Step 2) Set the stopband loss A_a of $NTF(z)$ to $SQNR_{min}$.

Step 3) Set the passband ripple A_p of $NTF(z)$ to be as large as possible. Note that as A_p increases, the achievable $SQNR$ increases but the stability margin decreases. It is important to have A_p as large as possible while still maintaining a stable converter operation.

Step 4) Set the cutoff frequency W_n of $NTF(z)$ to BW.

Step 5) Calculate $STF(z)$ as detailed in Section 4.2. The constituent multiplier coefficients may be determined as detailed in Sections 4.3.1 to 4.3.5.

Step 6) Simulate the nonlinear magnitude-squared complementary converter and test for stability. If unstable, then lower A_p and go to Step 5.

4.4.2 Design of Magnitude Complementary Σ-Δ A/D Converters

The design of magnitude complementary Σ-Δ A/D converters proceeds similarly in a step-by-step manner as discussed in the following.

Step 1) Choose $H(z)$ to be an odd N-th order highpass filter or an even $2N$-th order bandstop classical transfer function.

Step 2) Set the stopband loss A_a of $H(z)$ to $SQNR_{min}/2$.

Step 3) Set the passband ripple A_p of $H(z)$ to be as large as possible. Note that as before, as A_p increases, the achievable $SQNR$ increases but stability margin decreases.

Step 4) Set the cutoff frequency W_n of $H(z)$ to BW.

[3] Butterworth, (inverse) Chebyschev, or elliptic.

Step 5) Calculate the magnitude complementary $NTF(z)$ and $STF(z)$ as detailed in Section 4.2. The constituent multiplier coefficients may be determined as detailed in Sections 4.3.1 to 4.3.5.
Step 6) Simulate magnitude complementary converter and test for stability. If unstable, then lower A_p and go to Step 5.

4.5 Advantages of the Proposed Σ-Δ A/D Converters

The resulting Σ-Δ A/D converters embody three important practical advantages as compared to the hitherto feedforward and multiple-feedback A/D converters, including a) their noise transfer function can be obtained without any recourse to numerical optimization, simplifying the design process, b) their noise transfer function is guaranteed to be bounded below 1, resulting in a highly stable A/D converter operation, and c) in the signal band, where the magnitude of the signal transfer function is 1, the magnitude of their noise transfer function is automatically 0 resulting in high $SQNR$ in an actual (nonlinear) converter operation.

Subsequently, the next chapter presents a detailed empirical investigation of the proposed Σ-Δ A/D converter configurations to determine the significance of magnitude-squared complementary signal and noise transfer functions on a) their achievable $SQNR$ and DR performance, and b) their stability performance in the presence of capacitor mismatches in corresponding SC hardware implementations.

4.6 Concluding Remarks

This chapter has introduced five novel feedforward and multiple-feedback Σ-Δ A/D converter configurations for the realization of magnitude-squared and magnitude complementary signal and noise transfer functions (in addition to complementary signal and noise transfer functions). The resulting Σ-Δ A/D converters embody three important practical advantages as compared to the hitherto feedforward and multiple-feedback A/D converters, including a) their noise transfer function can be obtained without any recourse to numerical optimization, simplifying the design process, b) their noise transfer function is guaranteed to be bounded below 1, resulting in a highly stable A/D converter operation, and c) in the signal band, where the magnitude of the signal transfer function is 1, the magnitude of their noise transfer function is automatically 0 resulting in high $SQNR$ in an actual (nonlinear) converter operation.

Chapter 5

Design, Investigation, and Analysis of the Proposed Σ-Δ A/D Converter Configurations

The previous chapter was concerned with the realization of five modified Σ-Δ A/D converter configurations capable of realizing magnitude-squared and magnitude complementary signal and noise transfer functions. This chapter presents an empirical investigation and analysis of the MCOR, MCOI, MCRI, and the MFF, MMF Σ-Δ A/D converters satisfying a set of high-level system specifications. This investigation includes the determination of the impact of magnitude-squared complementary signal and noise transfer functions on the achievable $SQNR$, DR, and the stability of the Σ-Δ A/D converters in a corresponding SC hardware implementation.

Section 5.1 presents the design, investigation, and analysis of the MCOI, MCOR, and MCRI Σ-Δ A/D converter configurations. Section 5.2 presents a similar investigation for the MFF and MMF A/D converter configurations. Then, Section 5.3 compares the results obtained for MCOI, MCOR, MCRI, MFF, and MMF Σ-Δ A/D converters to those obtained for the corresponding COI, COR, CRI, FF, and MF A/D converters in Section 3.4. Finally, the main conclusions of the chapter are presented in Section 5.4.

5.1 Design and Simulation of the MCOI, MCOR, and MCRI Σ-Δ A/D Converter Configurations

The design specifications for the MCOI, MCOR, and MCRI Σ-Δ A/D converters are given in Table 5.1. These design specifications are very similar to those given in Table 3.2 for the A/D converter design in Section 3.4.

The noise and signal transfer functions $NTF(z)$ and $STF(z)$ were determined using the design

Table 5.1: Σ-Δ A/D Converter Design Specifications

Sampling Frequency	640 kHz
Passband Edge Frequency	20 kHz
Desired $SQNR$	56 dB
Order	5

Table 5.2: MCOI, MCOR and MCRI Σ-Δ A/D Converter Noise and Signal Transfer Function Coefficients

a_1	−4.94731925395907	a_2	9.84254945217749
a_3	−9.84254945217749	a_4	4.94731925395907
a_5	−1	G	0.65636818432169
b_1	−4.11722967144513	b_2	6.88281044847699
b_3	−5.81956791049806	b_4	2.48256347017200
b_5	−0.42576340605744		
c_0	0.07110405988635	c_1	−0.19176810930984
c_2	0.12207051474767	c_3	0.12207051474767
c_4	−0.19176810930984	c_5	0.07110405988635

procedure outlined in the previous chapter, leading to

$$NTF(z) = G\frac{1 + a_1z^{-1} + a_2z^{-2} + a_3z^{-3} + a_4z^{-4} + a_5z^{-5}}{1 + b_1z^{-1} + b_2z^{-2} + b_3z^{-3} + b_4z^{-4} + b_5z^{-5}}, \tag{5.1}$$

$$STF(z) = \frac{c_0 + c_1z^{-1} + c_2z^{-2} + c_3z^{-3} + c_4z^{-4} + c_5z^{-5}}{1 + b_1z^{-1} + b_2z^{-2} + b_3z^{-3} + b_4z^{-4} + b_5z^{-5}}, \tag{5.2}$$

where the coefficients a_1 through a_5, b_1 through b_5, and c_1 through c_5 are shown for the MCOI, MCOR, MCRI Σ-Δ A/D converters in Table 5.2. A magnitude-frequency plot of the resulting noise and signal transfer functions is as shown in Fig. 5.1 for the MCOI, MCOR, and MCRI A/D converters. It is important to notice that the noise transfer function is bounded from above by unity gain.

Next, the nominal multiplier values were determined for each of the five magnitude-squared complementary A/D converters as tabulated in Tables 5.3 to 5.5. Then, the achievable $SQNR$ as a function of the amplitude of a 3 kHz sinusoidal input signal was determined. By sweeping the sinusoidal input signal amplitude from −90 dB to 0 dB, the $SQNR$ plot was obtained as shown in Fig. 5.2. As is evident from the plot, the same achievable peak-signal-to-quantization-noise ratio ($PSQNR$) of 56.5 dB and the same DR of 70.7 dB was observed for the three A/D converters.

The capacitor values were then determined and scaled for both maximum dynamic range and minimum capacitance spread and total capacitance, leading to the capacitor values given in Tables 5.6 to 5.8. An inspection of the values in these tables reveals that the MCOI Σ-Δ A/D converter

Table 5.3: MCOI Σ-Δ A/D Converter Nominal Multiplier Values

R_1	−0.02015398572478	R_2	4.74676139057003
R_3	−25.00099446810740	R_4	45.92088354320634
R_5	80.46955965472353	R_6	0.10832953452768
A_1	−0.05268074604093	A_2	−0.05327243634120
A_3	−0.00118338060054	A_4	−0.00059169030027
A_5	0		
B_1	−1.26467065641181	B_2	−0.54941621938598
B_3	−0.18937850528210	B_4	−0.03404890587307
B_5	−0.00428559871662	G	0.65636818432169

Table 5.4: MCOR Σ-Δ A/D Converter Nominal Multiplier Values

A_1	0.10832953452768	A_2	0.24377533680415
A_3	0.08595661541496	A_4	0.06207186806802
A_5	0.00751711911847	A_6	0.00428559871662
B_1	−1.26467065641180	B_2	−0.50332395418071
B_3	−0.12494206401594	B_4	−0.01570472981218
B_5	−0.00428559871662	G	0.65636818432169
R_1	−0.01623468399972	R_2	−0.03644606204120

Table 5.5: MCRI Σ-Δ A/D Converter Nominal Multiplier Values

B_1	−0.99999999999945	B_2	4.24998538281488
B_3	−22.94908556211249	B_4	47.22728141561618
B_5	80.46955965373127	B_6	0.10832953452768
A_1	−1.26467065641180	A_2	−0.48279242571014
A_3	−0.11416843577696	A_4	−0.02286084820574
A_5	−0.00168381687860	G	0.65636818432169
R_1	−0.03644606204120	R_2	−0.01623468399972

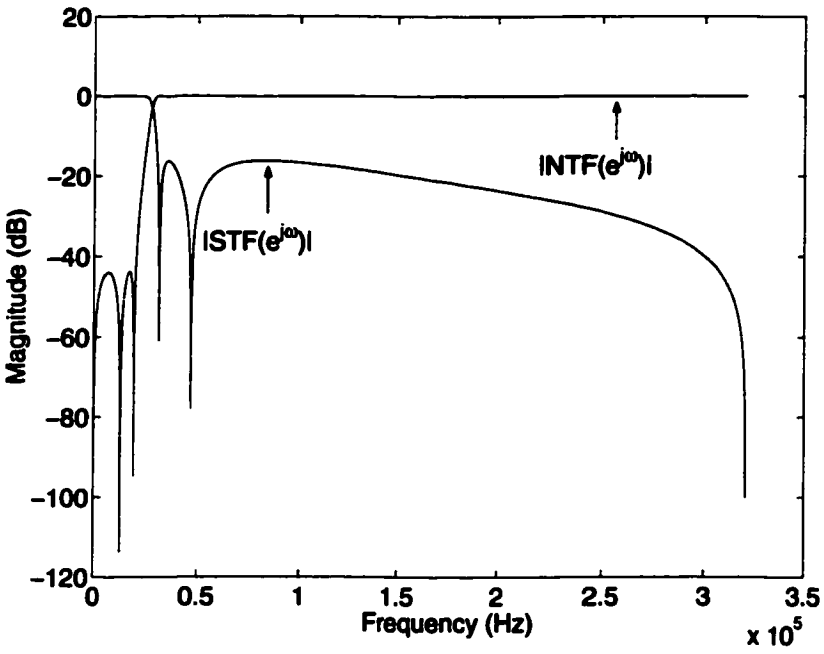

Figure 5.1: Magnitude-Frequency Plot of $NTF(z)$ and $STF(z)$ for the MCOI, MCOR, and MCRI Σ-Δ A/D Converters

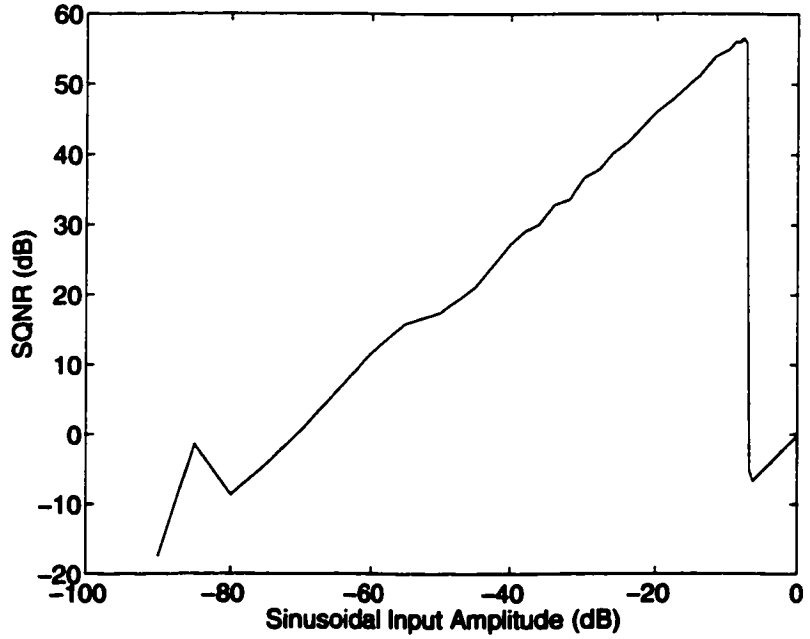

Figure 5.2: $SQNR$ versus Sinusoidal Input Signal Level for MCOI, MCOR, and MCRI

Table 5.6: MCOI Σ-Δ A/D Converter Scaled Capacitor Values

Capacitor	Value	Capacitor	Value
CR_1	−1.30918078968271	CF_1	46.66814671183060
CR_2	6.60717065373864	CF_2	5.08217949946317
CR_3	−6.84739540310877	CF_3	3.56291121334064
CR_4	3.52998905210302	CF_4	2.82458728638623
CR_5	2.18997797821535	CF_5	3.97960529465630
CR_6	1	CF_6	−1
CA_1	−2.45851278512665	CB_1	−8.38711198816223
CA_2	−12.63493795433773	CB_2	−18.51767578981508
CA_3	−1	CB_3	−22.74158261258900
CA_4	−1.41229364319179	CB_4	−11.54910050741024
CA_5	0	CB_5	−5.78490862268652
CX_1	1		
CX_2	1		
CX_3	1		
CX_4	1	CG	4.61884167940045

Table 5.7: MCOR Σ-Δ A/D Converter Scaled Capacitor Values

Capacitor	Value	Capacitor	Value
CA_1	1	CB_1	−3.40514177273324
CA_2	1	CB_2	−20.23374543515793
CA_3	5.26454044940471	CB_3	−1.32117814810544
CA_4	1	CB_4	−1.37128131530488
CA_5	1	CB_5	−1
CA_6	1.52353514976254		
CF_1	6.99932202577311	CX_1	2.61916927665205
CF_2	8.75958573648249	CX_2	1.06081629986459
CF_3	5.64722620574069	CX_3	21.46896758558008
CF_4	53.78499843047843	CX_4	3.60238590632573
CF_5	4.12558210728489	CX_5	9.28385017162211
CF_6	−9.23109292733515		
CR_1	1		
CR_2	1.69953134125228		

Table 5.8: MCRI Σ-Δ A/D Converter Scaled Capacitor Values

Capacitor	Value	Capacitor	Value
CA_1	−5.87736201648536	CB_1	−14.06389454551282
CA_2	−14.13319815524053	CB_2	10.78648513173512
CA_3	−11.39347098869816	CB_3	−7.23666565615489
CA_4	−7.75420609981015	CB_4	19.89377628814851
CA_5	−2.27289753990933	CB_5	2.18997797818835
		CB_6	1
CF_1	7.08039486375152	CX_1	1.27774558754309
CF_2	8.04858231159930	CX_2	1
CF_3	3.40902353897281	CX_3	4.55387557524139
CF_4	15.47804697153920	CX_4	1
CF_5	3.97960529465630		
CF_6	−1		
CR_1	1	CG_1	1
CR_2	1		

has a total capacitance of 177.706 units and a spread of 46.668, the MCOR A/D converter has a total capacitance of 167.40 units and a spread of 53.785, and the MCRI A/D converter has a total capacitance of 146.43 units and a spread of 19.894.

Monte-Carlo simulations of 1000 different samples of each of the three Σ-Δ A/D converters led to the determination of the actual $SQNRs$ as shown in Fig. 5.3 and summarized in Table 5.9, where the capacitor values were individually perturbed around their nominal values with a Gaussian distributed white random variable ϵ of zero mean and of $\sigma = 0.00333$ standard deviation[1]. Under capacitance perturbations, the MCOI A/D converter gave rise to slightly fewer unstable samples and the highest amount of $SQNR$ variance among the stable samples than the MCOR, and MCRI A/D converters. Since the noise transfer function zeros for the MCOI A/D converter are nominally forced to be on the unit-circle, the zeros of $NTF(z)$ may move off the unit-circle significantly due to capacitor tolerances, affecting the achievable $SQNR$, and thus resulting in more $SQNR$ variance among the samples. The lowest amount of $SQNR$ variance was observed when the Σ-Δ A/D converter configuration proper guaranteed the location of the noise transfer function zeros on the unit-circle.

Finally, the above Monte-Carlo simulations were repeated for several other standard deviations. The main results of these simulations are as shown in Table 5.10. As ϵ_{max} increased, the MCOI and MCRI A/D converters produced more unstable samples whereas the MCOR A/D converter showed

[1]The samples with substantially low $SQNR$ imply unstable Σ-Δ A/D converter operation and were discarded.

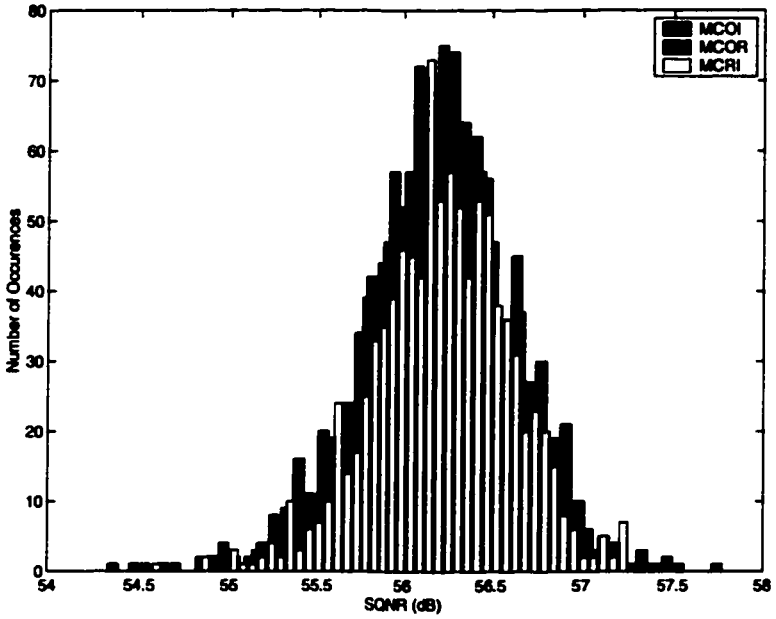

Figure 5.3: MCOI, MCOR, and MCRI Σ-Δ A/D Converters Monte-Carlo Simulation Results

Table 5.9: Monte-Carlo Simulation Results

$SQNR$ (ϵ_{max}=1.0%)	MCOI	MCOR	MCRI
Nominal (dB)	56.099	56.099	56.099
Variance (dB)	0.190881	0.15481	0.15293
Max. (dB)	57.781	57.568	57.257
Min. (dB)	54.322	54.439	54.571
Mean (dB)	56.192	56.204	56.216

less sensitivity to ϵ_{max}.

5.2 Design and Simulation of the MFF and MMF Σ-Δ A/D Converter Configurations

The MFF and MMF converters are well suited for the implementation of Butterworth and Chebyshev type I noise transfer functions because they guarantee the noise transfer function zeros to remain at $z = 1$ (by appropriately setting the R_k multiplier coefficients to 0). However, by not moving the noise transfer function zeros in-band, achieving a high $SQNR$ with a low oversampling ratio (i.e. an oversampling ratio of 16) becomes very difficult. In order to facilitate a 20 kHz signal bandwidth as called for by the previous system specifications, it was determined (through many simulations) that the required oversampling ratio must be doubled from 16 to 32 to achieve the desired $SQNR$ and DR performance. The updated system design specifications are as shown in Table 5.11. This result

Table 5.10: Percentage of Unstable Samples

ϵ_{max} (%)	MCOI	MCOR	MCRI
0.1	1.7	2.2	1.9
0.5	2.3	1.7	2.1
1.0	2.1	3.0	3.2
1.5	3.3	2.2	2.4
2.0	4.2	2.6	4.6

agrees reasonably well with the result given in (Welland et. al., [33]), where it was concluded that an 11 dB increase in $SQNR$ can be obtained by placing the noise transfer function zeros in-band as opposed to leaving them at DC.

Table 5.11: MFF and MMF Σ-Δ A/D Converter Design Specifications

Sampling Frequency	1.28 MHz
Passband Edge Frequency	20 kHz
Desired $SQNR$	55 dB
Order	5
Filter type	Chebyshev Type I

The noise and signal transfer functions $NTF(z)$ and $STF(z)$ were determined by using the design procedure outlined in the previous chapter, [2] leading to

$$NTF(z) = G\frac{1 + a_1 z^{-1} + a_2 z^{-2} + a_3 z^{-3} + a_4 z^{-4} + a_5 z^{-5}}{1 + b_1 z^{-1} + b_2 z^{-2} + b_3 z^{-3} + b_4 z^{-4} + b_5 z^{-5}}, \tag{5.3}$$

$$STF(z) = \frac{c_0 + c_1 z^{-1} + c_2 z^{-2} + c_3 z^{-3} + c_4 z^{-4} + c_5 z^{-5}}{1 + b_1 z^{-1} + b_2 z^{-2} + b_3 z^{-3} + b_4 z^{-4} + b_5 z^{-5}}, \tag{5.4}$$

where the coefficients a_1 through a_6, b_1 through b_6, and c_1 through c_6 are shown for the MFF and MMF A/D converters in Table 5.12. The resulting magnitude-frequency plots for $NTF(z)$ and $STF(z)$ are shown in Fig. 5.4

Next, the multiplier values were found as given in Tables 5.13 and 5.14. Then, the achievable $SQNR$ as a function of the amplitude of a 3 kHz sinusoidal input signal was determined for the MFF and MMF Σ-Δ A/D converters. By sweeping the sinusoidal input signal amplitude from -90 dB to 0 dB, the $SQNR$ plot shown in Fig. 5.5 was obtained. The MFF A/D converter had a $PSQNR$ of 64.2 dB and a DR of 79.8 dB. The MMF A/D converter had a $PSQNR$ of 63.8 dB and a DR of 77.9 dB. The slight difference between the $PSQNR$ for the MFF and MMF A/D converters arises

[2]Note that only the cutoff frequency w_n and the passband ripple A_p must be set in the design of Chebyshev noise transfer functions $NTF(z)$

Table 5.12: MFF and MMF Σ-Δ A/D Converter Noise and Signal Transfer Function Coefficients

a_1	−5	a_2	10
a_3	−10	a_4	5
a_5	−1	G	0.69622426102791
b_1	−4.28513808220955	b_2	7.38058688599618
b_3	−6.37692775131968	b_4	2.75936840127495
b_5	−0.47720493933595		
c_0	0.08673685668687	c_1	−0.24806972533326
c_2	0.16167512584936	c_3	0.16167512584936
c_4	−0.24806972533326	c_5	0.08673685668687

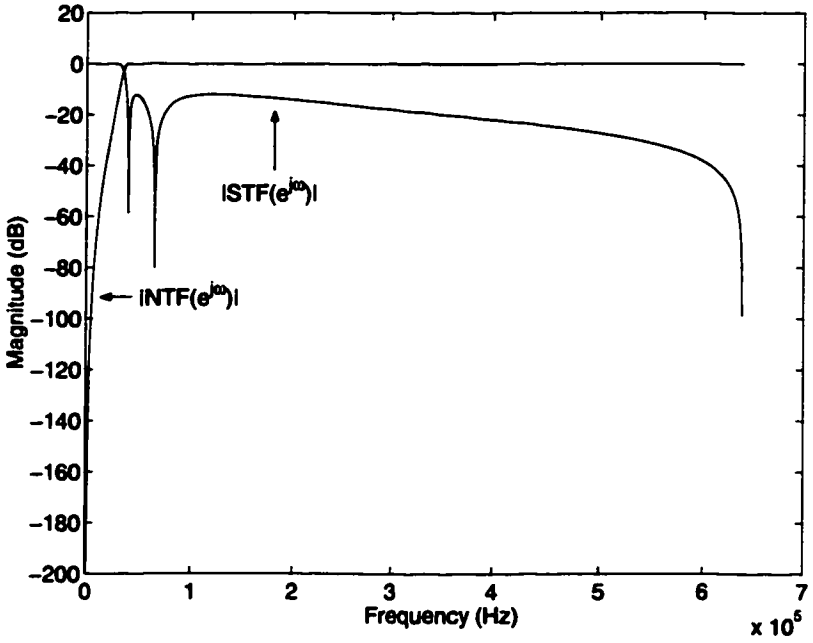

Figure 5.4: Magnitude-Frequency Plot of $NTF(z)$ and $STF(z)$ for MFF and MMF Σ-Δ A/D Converter Configurations

Table 5.13: MFF Σ-Δ A/D Converter Nominal Multiplier Values

B_1	−0.999999999999	B_2	7.318972000369
B_3	−30.443161819708	B_4	18.448700452976
B_5	427.322394607792	B_6	0.124581778519
A_1	−1.02676961692633	A_2	−0.34476614877450
A_3	−0.07756755464369	A_4	−0.00965382587501
A_5	−0.00098318091493	G	0.69622426102791
R_1	0	R_2	0

Table 5.14: MMF Σ-Δ A/D Converter Nominal Multiplier Values

A_1	0.12458177851892	A_2	0.26660168065255
A_3	0.05280596130161	A_4	0.03684260905929
A_5	0.00245795228732	A_6	0.00098318091493
B_1	−1.02676961692633	B_2	−0.34476614877450
B_3	−0.07756755464369	B_4	−0.00965382587501
B_5	−0.00098318091493	G	0.69622426102791
R_1	0	R_2	0

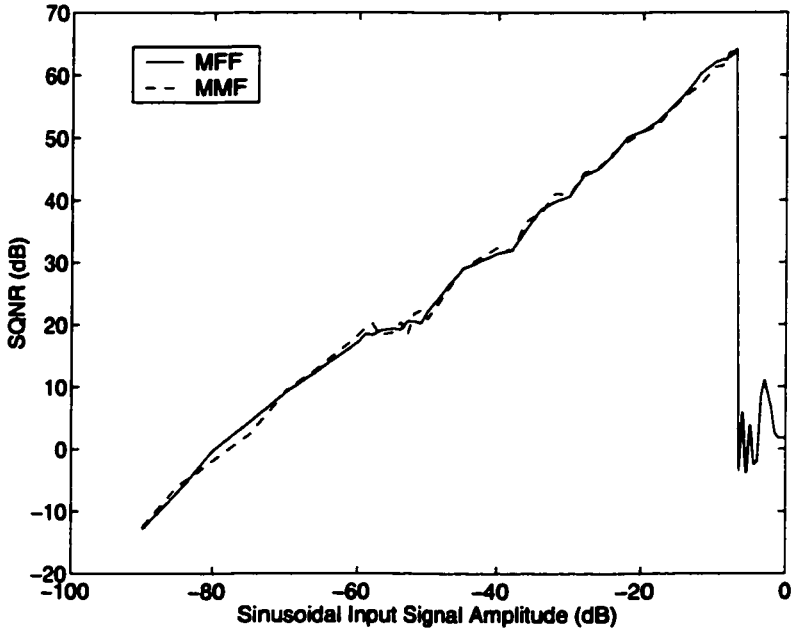

Figure 5.5: $SQNR$ versus Sinusoidal Input Signal Level for MFF and MMF Σ-Δ A/D Converters

from the Matlab based matrix inversion that is required to calculate the corresponding two sets of coefficient values.

By making use of the scheme in 4.4 to factor out the common pre and post multiplier values, the capacitor values for the SC hardware implementations of the MFF and MMF A/D converters can be determined. In the case of the MFF A/D converter, M was appropriately set to B_6 whereas in the case of the MMF A/D converter, M was set to A_1. By employing the capacitor scaling technique in (Gregorian et. al., [23]), the scaled capacitor values are obtained as given in Tables 5.15 and 5.16 for the MFF and MMF A/D converters, respectively. The resulting MFF A/D converter has a capacitance spread of 14.908 and a total capacitance of 118.1908 units, while the resulting MMF A/D converter has a capacitance spread of 11.529 and a total capacitance of 64.5800 units.

Monte-Carlo simulations of 1000 different samples of the MFF and MMF Σ-Δ A/D converters

Table 5.15: MFF Σ-Δ A/D Converter Scaled Capacitor Values

Capacitor	Value	Capacitor	Value
CA_1	−6.96486990897411	CB_1	−11.52912427538410
CA_2	−14.90835128905212	CB_2	8.66075113038160
CA_3	−13.23686380227860	CB_3	−5.65106404931460
CA_4	−8.64071063006752	CB_4	1
CA_5	−4.91777256301217	CB_5	3.83222612195165
		CB_6	1
CF_1	9.74295837509670	CX_1	1
CF_2	6.37477704331629	CX_2	1
CF_3	3.94638998209865	CX_3	1.15237478550747
CF_4	6.04419889530963	CX_4	1
CF_5	5.58836803681210		
CF_6	−1		
CR_1	0	CG_1	1
CR_2	0		

Table 5.16: MMF Σ-Δ A/D Converter Scaled Capacitor Values

Capacitor	Value	Capacitor	Value
CA_1	1.02110405297256	CB_1	−1
CA_2	2.99354778092600	CB_2	−1
CA_3	1.76585344150512	CB_3	−1.23863758261587
CA_4	6.78282873302369	CB_4	−1.00808839243507
CA_5	2.95916322923003	CB_5	−1
CA_6	11.52912427536204		
CF_1	9.74018952510051	CX_1	1
CF_2	6.53935628866278	CX_2	1
CF_3	5.58547355575507	CX_3	1.01454480064048
CF_4	3.00276420077574	CX_4	1.00826069657033
CF_5	1.36995984626725	CX_5	1
CF_6	−1.02110405297256		
CR_1	0		
CR_2	0		

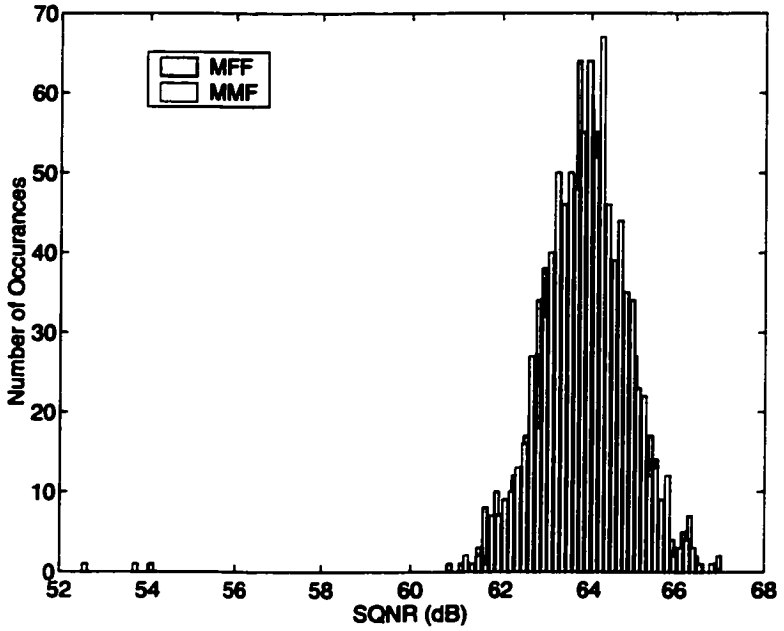

Figure 5.6: MFF and MMF Σ-Δ A/D Converters Monte-Carlo Simulation Results

led to the determination of the actual $SQNRs$ as shown in Fig. 5.6 and summarized in Table 5.17, where the capacitor values were individually perturbed around their nominal values with a Gaussian distributed white random variable ϵ of zero mean and of $\sigma = 0.00333$ standard deviation[3]. Under capacitance perturbations, the MMF Σ-Δ A/D converter gave rise to more unstable samples and the highest amount of $SQNR$ variance among the stable samples than the MFF A/D converters. However, by eliminating the Monte-Carlo samples resulting in $SQNR < 60$ dB, one finds that the MMF A/D converter produced 8% unstable samples with a variance of 0.8712 dB, while the MFF A/D converter produced 6% unstable samples with a very similar variance of 0.9644 dB. One would expect the variances to be similar since both configurations guarantee the location of the noise transfer function zeros.

Finally, the above Monte-Carlo simulations were repeated for several other standard deviations. The main results of these simulations are as shown in Table 5.18. The MMF Σ-Δ A/D converter shows less sensitivity to ϵ_{max} as compared to the MFF A/D converter as ϵ_{max} is increased.

By comparing the above simulation results, one can observe that converters which guarantee the noise transfer function zeros on the unit-circle provide the least amount of $SQNR$ variance. Furthermore, the MCOR and MMF A/D converters show the least amount of sensitivity to ϵ_{max} as compared to the MFF, MCOI, and MCRI A/D converters. The MCRI, and MFF converters show very similar sensitivity to ϵ_{max}. The MFF and MMF converters resulted in the highest number of unstable samples. Since the noise transfer function zeros are constrained to lie at DC, any shift in the pole locations will result in a reduction of signal bandwidth resulting in lower $SQNR$ values.

[3]The samples with substantially low $SQNR$ imply unstable Σ-Δ A/D converter operation and were discarded.

Table 5.17: Monte-Carlo Simulation Results

$SQNR$ (ϵ_{max}=1%)	MFF	MMF
Nominal (dB)	64.1560	64.4820
Variance (dB)	1.0680	1.1250
Max. (dB)	67.0627	66.9272
Min. (dB)	54.0004	52.4945
Mean (dB)	63.9104	63.9207

Table 5.18: Percentage of Unstable Samples

ϵ_{max}	MFF	MMF
0.1	7.5	5.0
0.5	6.5	6.9
1.0	5.9	7.8
1.5	7.9	6.1
2.0	10	7.8

5.3 Comparison of the Modified Σ-Δ A/D Converters to the Hitherto A/D Converters

This section is concerned with a comparison of the key performance features of the five modified Σ-Δ A/D converters presented in Chapter 5 and the corresponding hitherto A/D converters discussed in Chapter 3. This comparison is based on the achievable $SQNR$, DR, stability performance under capacitor mismatches, total capacitance, and capacitance spread.

Achievable *SQNR*: The COI, COR, and CRI Σ-Δ A/D converters gave the highest $SQNR$ performance levels followed by the MCOI, MCOR, and MCRI A/D converters. All six of these converters have their constituent noise transfer function zeros on the unit-circle. The FF and MF Σ-Δ A/D converters gave slightly lower $SQNR$ performance levels compared to the other converters as a result of their constituent noise transfer function zeros being on the real line $Re(z) = 1$. The MMF and MFF Σ-Δ A/D converters gave a high level of $SQNR$ but for an oversampling ratio of 32.

Dynamic Range: The COI, COR, CRI, MCOI, MCOR, and MCRI Σ-Δ A/D converters featured identical DR performance. The FF and MF A/D converters gave slightly lower DR performance while the MFF and MMF A/D converters gave a larger DR performance level due to the higher oversampling ratio. One can attribute the location of the noise transfer function zeros to the dynamic range performance.

Stability: The MCOI, MCOR, MCRI, MFF, and MMF Σ-Δ A/D converters gave substantially higher stability performance in the presence of capacitor mismatch as compared to the hitherto A/D

Table 5.19: Comparison of Σ-Δ A/D Converter Configurations

Configuration	$PSQNR$	DR	% Unstable	Variance	Total Cap	Cap Spread
COI	61.1	70.0	37.4	1.18	975.0	499.0
COR	61.1	70.0	24.9	0.57	176.3	34.0
CRI	61.1	70.0	28.4	0.59	272.7	77.4
FF	52.9	65.0	26.6	0.82	199.3	80.6
MF	52.9	64.0	33.1	0.76	651.8	320.4
MCOI	56.5	70.7	2.1	0.19	177.7	46.7
MCOR	56.5	70.7	3.0	0.15	167.4	53.8
MCRI	56.5	70.7	3.2	0.15	146.4	19.9
MFF ($OSR = 32$)	64.2	79.8	5.9	1.06	118.2	14.9
MMF ($OSR = 32$)	63.8	77.9	7.8	1.13	64.6	11.5

converter configurations. One can attribute this increase in stability to the choice of magnitude-squared complementary signal and noise transfer functions.

Variance of *SQNR*: The MCOI, MCOR, MCRI, MFF, and MMF Σ-Δ A/D converters gave substantially less $SQNR$ variance than the other converters. In particular, converter configurations which guarantee the noise transfer function zeros on the unit-circle gave less variance than configurations which did not.

Total capacitance and capacitance spread: The COR Σ-Δ A/D converter featured the lowest capacitance spread and total capacitance among the hitherto Σ-Δ A/D converters. The distribution of the feedforward and feedback paths of this A/D converter lends itself very well to capacitor scaling. The MF Σ-Δ A/D converter features a similar topology to that of the COR A/D converter, but led to a much larger capacitor spread and total capacitance due to the very small R coefficients. The MCOR Σ-Δ A/D converter featured higher capacitance spread and total capacitance as a result of the noise transfer function having slightly smaller R coefficients than found in the COR design. The MMF, on the other hand, offered the lowest amount of capacitor spread and total capacitance among the COR, MCOR, and MMF Σ-Δ A/D converters due to the absence of the CR capacitors (as a result of the noise transfer function zeros being located at DC).

The CRI Σ-Δ A/D converter featured almost identical spread to that of the FF Σ-Δ A/D converter configurations. However, the CRI A/D converter configuration resulted in much higher total capacitance as compared to the FF A/D converter. The MCRI Σ-Δ A/D converter featured much smaller spread and total capacitance as compared to the CRI Σ-Δ A/D converter. This can be attributed to the elimination of the small CR_3 capacitor associated with the CRI Σ-Δ A/D converter. Furthermore, the MFF Σ-Δ A/D converter gave rise to a very small spread and total capacitance. This can also be attributed to the elimination of the CR capacitors.

The COI Σ-Δ A/D converter gave rise to the largest amount of capacitor spread and total capacitance as compared to the other Σ-Δ A/D converters. This can be attributed to the fact that all of the feedforward capacitors sum at the same op-amp and all of the feedback capacitors sum at the same op-amp. The MCOI Σ- Δ A/D converter substantially improved the capacitor spread and total capacitance due to the substantially increased nominal B multiplier coefficients. Thus, when scaling for minimum capacitance, the CF_1 value remains reasonably small.

5.4 Concluding Remarks

This chapter has been concerned with the an empirical investigation of the proposed Σ-Δ A/D converter configurations. It was demonstrated that the proposed Σ-Δ A/D converter configurations not only give rise to an achievable $SQNR$ and DR comparable to that obtained by the existing Σ-Δ A/D converter configurations, but also give rise to very high stability performance in the presence of capacitor mismatches in a corresponding SC hardware implementation.

A comparison of the key performance features of the five modified Σ-Δ A/D converters presented in Chapter 5 and the corresponding hitherto A/D converters discussed in Chapter 3 was presented. This comparison was based on the achievable $SQNR$, DR, stability performance under capacitor mismatches, total capacitance, and capacitance spread.

Chapter 6

Conclusion

This thesis has been concerned with the design and analysis of ten different feedforward and multiple-feedback Σ-Δ A/D configurations.

Chapter 2 was concerned with the characterization of five practical existing feedforward and multiple-feedback Σ-Δ A/D converter configurations. These configurations were characterized in terms of two important features, namely, a) the location of their noise transfer function zeros with respect to the unit circle in the complex z-plane, and b) the relationship between their signal and noise transfer functions.

Chapter 3 presented a design procedure for the above feedforward and multiple-feedback Σ-Δ A/D converter configurations. This design procedure was based on a set of high-level system design specifications and proceeded in a step-by-step manner. Each of the five feedforward and multiple-feedback A/D converters were then designed and simulated to determine, a) the effect of the noise transfer function zeros on their achievable $SQNR$ and DR, and b) the effect of capacitor mismatches on their $SQNR$ and DR in a corresponding SC hardware implementation. The effect of capacitor mismatch was investigated through Monte-Carlo analysis. It has been shown that A/D converters having noise transfer function zeros on the unit-circle exhibit superior performance in terms of the achievable $SQNR$, regardless of whether the noise transfer function zeros are located on the unit-circle by the A/D converter configuration proper or by numerical optimization. However, it is has been shown that if the noise transfer function zeros are located on the unit-circle by numerical optimization, then the Σ-Δ A/D converter exhibits a high level of stability at low capacitor tolerances, but that the A/D converter becomes highly prone to instability as the capacitor mismatches are increased. The A/D converters which guarantee the location of the noise transfer function zeros on the line $Re(z) = 1$ have shown low sensitivity to capacitor mismatches in terms of the number of unstable samples produced as a function of capacitor tolerances. It has been observed that the main advantage of the complementarity of the signal and noise transfer functions is the reduction in the complexity of the design and optimization of the Σ-Δ A/D converter. A hitherto statistical approach for the estimation of the maximum DC input signal level for stable A/D converter operation was discussed. The main limiting assumption of the hitherto statistical approach was that the quantizer

input was Gaussian distributed. A proposed statistical approach was then developed for arbitrary quantizer input signal distributions by employing the Gram-Charlier series. A typical application example was been given demonstrating that the proposed statistical approach leads to an 80% increase in the accuracy of estimating the noise power gain as compared to the hitherto statistical technique. This in turn gave rise to an improved accuracy in the estimation of the maximum DC input signal amplitude for stable A/D converter operation.

Chapter 4 was concerned with the development of a novel class of Σ-Δ A/D converters based on magnitude-squared or magnitude complementary signal and noise transfer functions. In particular, five different configurations were introduced which were capable of realizing magnitude-squared and magnitude complementary signal and noise transfer functions (in addition to being capable of realizing complementary signal and noise transfer functions).

Chapter 5 was concerned with an investigation and comparison of the proposed Σ-Δ A/D converters to the corresponding existing A/D converters. It was shown that the proposed A/D converters exhibit a high degree of stability in the presence of capacitor mismatches in a corresponding SC hardware implementation as compared to the existing converters. It was further shown that the achievable $SQNR$ and DR remain very similar to that achieved by the feedforward and multiple feedback converters.

6.1 Original Contributions

The following lists the original contributions presented in this thesis.

6.1.1 Chapter 2

- Procedure to determine the constituent multiplier coefficients for a set of N-th order Σ-Δ A/D converter configurations.
- General equations for the numerator of the signal and noise transfer function $S(z)$ and $N(z)$ and for the denominator of the signal and noise transfer function $D(z)$ for a set of Σ-Δ A/D converter configurations.

6.1.2 Chapter 3

- Statistical approach based on Gram-Charlier series expansion to estimate the maximum DC input signal amplitude for a set of feedforward and multiple-feedback Σ-Δ A/D converter configurations.
- A procedure to determine the statistical moments of the quantizer input signal for first- and second-order Σ-Δ A/D converter configurations with DC input signals without recourse to nonlinear simulations.

6.1.3 Chapter 4

- The application of magnitude-squared and magnitude complementary signal and noise transfer functions to Σ-Δ A/D converters.
- The development of five novel Σ-Δ A/D converter configurations and their corresponding switched-capacitor hardware implementations.
- A design procedure for magnitude-squared and magnitude complementary Σ-Δ A/D converters.

6.1.4 Chapter 5

- An empirical investigation of the novel Σ-Δ A/D converter configurations.

6.2 Future Work

In Section 3.5 a novel approach was presented for the estimation of the maximum DC input signal for higher order feedforward and multiple-feedback Σ-Δ A/D converter configurations. In this approach, knowledge of the higher-order moments of the quantizer input signal are required to model its corresponding distribution. A procedure to determine the quantizer input signal moments was presented for first- and second-order Σ-Δ A/D converters. Future work may focus on developing techniques to determine these moments for higher-order Σ-Δ A/D converters without recourse to non-linear simulations.

In Section Chapter 4, five modified feedforward and multiple-feedback Σ-Δ A/D converter configurations were presented which were capable of realizing magnitude-squared and magnitude complementary signal and noise transfer functions. Future work may focus on developing other configurations for this purpose which may perform better in a corresponding SC hardware implementation.

Switched-capacitor hardware implementations rely on three key components, namely a) capacitors, b) transistors, and c) operational amplifiers. Each one of these devices contributes noise to the circuit and ultimately to the degradation of signal-to-quantization-noise ratio and dynamic range of the resulting Σ-Δ A/D converter. Moreover, these circuit nonidealities become more problematic as the power supply of the circuit is reduced for low-voltage low-power applications. Future work may focus on characterizing these noise sources and determining their effect on $SQNR$ and dynamic range.

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Appendix A

Appendix

A.1 Important Properties of Hermite Polynomials

Property 1.

$$\int_a^b x^2 e^{\frac{-x^2}{2\sigma_x^2}} dx = a\sigma_x e^{\frac{-a^2}{2\sigma_x^2}} - b\sigma_x e^{\frac{-b^2}{2\sigma_x^2}} + \sigma_x\sqrt{\frac{\pi}{2}}\left[erf\left(\frac{b}{\sqrt{(2)}\sigma_x}\right) - erf\left(\frac{a}{\sqrt{2}\sigma_x}\right)\right] \tag{A.1}$$

Property 2.

$$\int x e^{\frac{-x^2}{2\sigma_x^2}} H_k(x)dx = -x\sigma_x H_{k-1}(x)e^{\frac{-x^2}{2\sigma_x^2}} - \sigma_x^2 H_{k-2}(x)e^{\frac{-x^2}{2\sigma_x^2}} \tag{A.2}$$

Property 3.

$$e^{\frac{-x^2}{2}} H_N(x) = (-1)^N \frac{d^N}{dx^N} e^{\frac{-x^2}{2}} \tag{A.3}$$

Property 4.

$$e^{\frac{-x^2}{2}} H_{N-1}(x) = (-1)^{N-1} \frac{d^{N-1}}{dx^{N-1}} e^{\frac{-x^2}{2}} \tag{A.4}$$

Property 5.

$$\frac{d}{dx} H_{N-1}(x)e^{\frac{-x^2}{2}} = (-1)^{N-1} \frac{d^N}{dx^N} e^{\frac{-x^2}{2}} \tag{A.5}$$

Property 6.

$$e^{\frac{-x^2}{2}} H_N(x) = -\frac{d}{dx} H_{N-1}(x)e^{\frac{-x^2}{2}} \tag{A.6}$$

Property 7.

$$\int e^{\frac{-x^2}{2}} H_N(x)dx = -H_{N-1}(x)e^{\frac{-x^2}{2}} \tag{A.7}$$

Property 8.

$$\int_a^b e^{\frac{-x^2}{2\sigma_x^2}} dx = \sigma_x\sqrt{\frac{\pi}{2}}\left[erf\left(\frac{b}{\sqrt{2}\sigma_x}\right) - erf\left(\frac{a}{\sqrt{2}\sigma_x}\right)\right] \tag{A.8}$$

Property 9.

$$C_1 \int x e^{\frac{-x^2}{2\sigma_x^2}} dx = C_1 \left[-\sigma_x^2 e^{\frac{-b^2}{2\sigma_x^2}} + \sigma_x^2 e^{\frac{-a^2}{2\sigma_x^2}} \right] \tag{A.9}$$

Property 10.

$$C_N \int_a^b e^{\frac{-x^2}{2\sigma_x^2}} H_N(x) dx = C_N \sigma_x \left[-H_{N-1}(b) e^{\frac{-b^2}{2\sigma_x^2}} + H_{N-1}(a) e^{\frac{-a^2}{2\sigma_x^2}} \right] \tag{A.10}$$

A.2 Derivation of k Using Gram-Charlier Series

Starting from the general expression for k, namely

$$k = \frac{Cov\{x, y(n)\}}{\sigma_x^2}, \tag{A.11}$$

an expression for k can be obtained in terms of the Gram-Charlier series as

$$k = \frac{1}{\sigma_x^2} \int_{-\infty}^{\infty} x y(n) \frac{1}{\sigma_x \sqrt{2\pi}} e^{\frac{-x^2}{2\sigma_x^2}} G(x) dx, \tag{A.12}$$

where $G(x) = \sum_{j=0}^{N} C_j H_j(x)$. Then, noting that $y(n) = -1$ when $-\infty < x < 0$, and that $y(n) = 1$ when $-m_e < x < \infty$, one obtains

$$k = \frac{1}{\sigma_x^2} \left[-\int_{-\infty}^{-m_e} x \frac{1}{\sigma_x \sqrt{2\pi}} e^{\frac{-x^2}{2\sigma_x^2}} f_N(x) dx + \int_{-m_e}^{\infty} x \frac{1}{\sigma_x \sqrt{2\pi}} e^{\frac{-x^2}{2\sigma_x^2}} f_N(x) dx \right]. \tag{A.13}$$

Then, by factoring out $\frac{1}{\sigma_x \sqrt{2\pi}}$, one can write

$$k = \frac{1}{\sigma_x^3 \sqrt{2\pi}} \left[-\int_{-\infty}^{-m_e} x e^{\frac{-x^2}{2\sigma_x^2}} f_N(x) dx + \int_{-m_e}^{\infty} x e^{\frac{-x^2}{2\sigma_x^2}} f_N(x) dx \right]. \tag{A.14}$$

Using the fact that $C_0 H_0(x) = 1$, $C_1 H_1(x) = C_1 x$, and from Eqn. A.2,

$$k = \frac{1}{\sigma_x^3 \sqrt{2\pi}} \left[-\left(-\sigma_x^2 e^{\frac{-x^2}{2\sigma_x^2}} \right)_{-\infty}^{-m_e} - C_1 \int_{-\infty}^{-m_e} x^2 e^{\frac{-x^2}{2\sigma_x^2}} dx \right. \tag{A.15}$$

$$- \sum_{i=2}^{N} C_i \left(-x \sigma_x H_{i-1}(x) e^{\frac{-x^2}{2\sigma_x^2}} - \sigma_x^2 H_{i-2}(x) e^{\frac{-x^2}{2\sigma_x^2}} \right)_{-\infty}^{-m_e} \tag{A.16}$$

$$+ \left(-\sigma_x^2 e^{\frac{-x^2}{2\sigma_x^2}} \right)_{-m_e}^{\infty} + C_1 \int_{-m_e}^{\infty} x^2 e^{\frac{-x^2}{2\sigma_x^2}} dx \tag{A.17}$$

$$\left. + \sum_{i=2}^{N} C_i \left(-x \sigma_x H_{i-1}(x) e^{\frac{-x^2}{2\sigma_x^2}} - \sigma_x^2 H_{i-2}(x) e^{\frac{-x^2}{2\sigma_x^2}} \right)_{-m_e}^{\infty} \right] \tag{A.18}$$

Then, by invoking Property A.1 into the above equation, one obtains,

$$k = \frac{1}{\sigma_x^3 \sqrt{2\pi}} \left[2\sigma_x^2 e^{\frac{-m_e^2}{2\sigma_x^2}} - \left[m_e \sigma_x e^{\frac{-m_e^2}{2\sigma_x^2}} + C_1 \sigma_x \sqrt{\frac{\pi}{2}} \left(erf\left(\frac{-m_e}{\sqrt{2}\sigma_x} \right) + 1 \right) \right] \right. \tag{A.19}$$

$$- \sum_{i=2}^{N} C_i \left[m_e \sigma_x H_{i-1}(-m_e) e^{\frac{-m_e^2}{2\sigma_x^2}} - \sigma_x^2 H_{i-2}(-m_e) e^{\frac{-m_e^2}{2\sigma_x^2}} \right] \tag{A.20}$$

$$+ \left[-m_e \sigma_x e^{\frac{-m_e^2}{2\sigma_x^2}} + C_1 \sigma_x \sqrt{\frac{\pi}{2}} \left(1 - erf\left(\frac{-m_e}{\sqrt{2}\sigma_x} \right) \right) \right] \tag{A.21}$$

$$\left. \sum_{i=2}^{N} C_i \left[-m_e \sigma_x H_{i-1}(-m_e) e^{\frac{-m_e^2}{2\sigma_x^2}} + \sigma_x^2 H_{i-2}(-m_e) e^{\frac{-m_e^2}{2\sigma_x^2}} \right] \right]. \tag{A.22}$$

By collecting terms, one obtains the following expression for k

$$k = \frac{2}{\sigma_x^2\sqrt{2\pi}}\left[\sigma_x e^{\frac{-m_e^2}{2\sigma_x^2}} - m_e e^{\frac{-m_e^2}{2\sigma_x^2}} + C_1\sqrt{\frac{\pi}{2}}erf\left(\frac{m_e}{\sqrt{2}\sigma_x}\right)\right. \tag{A.23}$$

$$\left. + \sum_{i=2}^{N}\left[-m_e H_{i-1}(-m_e)e^{\frac{-m_e^2}{2\sigma_x^2}} + \sigma_x H_{i-2}(-m_e)e^{\frac{-m_e^2}{2\sigma_x^2}}\right]\right]. \tag{A.24}$$

A further simplification yields the final result

$$k = \frac{2}{\sigma_x^2\sqrt{2\pi}}e^{\frac{-m_e^2}{2\sigma_x^2}}\left[\sigma_x - m_e + C_1\sqrt{\frac{\pi}{2}}erf\left(\frac{m_e}{\sqrt{2}\sigma_x}\right)e^{\frac{m_e^2}{2\sigma_x^2}} + \sum_{i=2}^{N} C_i\left[-m_e H_{i-1}(-m_e) + \sigma_x H_{i-2}(-m_e)\right]\right]. \tag{A.25}$$

A.3 Derivation of m_y Using Gram-Charlier Series

Starting from the general expression for m_y

$$m_y = P(x > -m_e) - P(x < -m_e), \tag{A.26}$$

one may determine m_y in terms of the Gram-Charlier series as

$$m_y = \int_{-m_e}^{\infty}\frac{1}{\sqrt{2\pi}\sigma_x}e^{\frac{-e^2}{2\sigma_x^2}}f_N(x)dx - \int_{-\infty}^{-m_e}\frac{1}{\sqrt{2\pi}\sigma_x}e^{\frac{-e^2}{2\sigma_x^2}}f_N(x), \tag{A.27}$$

where $G(x) = \sum_{j=0}^{N} C_j H_j(x)$. Factoring out $\frac{1}{\sqrt{2\pi}\sigma_x}$ yields,

$$m_y = \frac{1}{\sqrt{2\pi}\sigma_x}\left[\int_{-m_e}^{\infty} e^{\frac{-e^2}{2\sigma_x^2}}f_N(x)dx - \int_{-\infty}^{-m_e} e^{\frac{-e^2}{2\sigma_x^2}}f_N(x)dx\right]. \tag{A.28}$$

Then, by invoking Properties A.8, A.9, and A.10 in Eqn. A.28 one obtains the expression

$$m_y = \frac{1}{\sqrt{2\pi}\sigma_x}\left[\sigma_x\sqrt{\frac{\pi}{2}}\left[1 - erf\left(\frac{-m_e}{\sqrt{2}\sigma_x}\right)\right] + C_1\left[\sigma_x^2 e^{\frac{-m_e^2}{2\sigma_x^2}}\right]\right. \tag{A.29}$$

$$+ \sigma_x\sum_{i=2}^{N}\left[H_{N-1}(-m_e)e^{\frac{-m_e^2}{2\sigma_x^2}}\right] - \sigma_x\sqrt{\frac{\pi}{2}}\left[erf\left(\frac{-m_e}{\sqrt{2}\sigma_x}\right) + 1\right] - C_1\left[-\sigma_x^2 e^{\frac{-m_e^2}{2\sigma_x^2}}\right] \tag{A.30}$$

$$\left. -\sigma_x\sum_{i=2}^{N}\left[-H_{N-1}(-m_e)e^{\frac{-m_e^2}{2\sigma_x^2}}\right]\right] \tag{A.31}$$

A further simplification yields the final result

$$m_y = \frac{2}{\sqrt{2\pi}}\left[\sqrt{\frac{\pi}{2}}erf\left(\frac{m_e}{\sqrt{2}\sigma_x}\right) + C_1\sigma_x e^{\frac{-m_e^2}{2\sigma_x^2}} + \sum_{i=2}^{N} C_i H_{i-1}(-m_e)e^{\frac{-m_e^2}{2\sigma_x^2}}\right]. \tag{A.32}$$

Appendix B

Appendix

B.1 Calculation of Minimum Oversampling Ratio

Consider a DC input signal $u(n) = \frac{p}{q}$. It is known that the output of the quantizer will consist of a stream of $+1$'s and -1's in proportion to the input amplitude. Let α represent the proportion of $+1$'s, then $1-\alpha$ represents the proportion of -1's. The input signal amplitude can then be written as,

$$\alpha(1) + (1-\alpha)(-1) = \frac{p}{q} \qquad then, \tag{B.1}$$

$$2\alpha - 1 = \frac{p}{q}. \tag{B.2}$$

From Eqn. B.2 one can write,

$$2q\alpha = p + q \qquad and \qquad 2q(1-\alpha) = q - p \tag{B.3}$$

From the above equation it can be noted that both $2q\alpha$ and $2q(1-\alpha)$ are integer values which represent the number of $+1$'s and -1's in one cycle of the quantizer output stream. Therefore, the cycle has a length of $2q$ samples and the $q-p$ -1's are interleaved among the $+1$'s as regularly as possible, resulting in smaller cycles within $2q$ samples. Consequently,

$$\frac{2q}{q-p} \tag{B.4}$$

is the average length of the smaller cycles yielding a period

$$\frac{1}{F_{tone}} = \frac{2q}{(q-p)F_s} \tag{B.5}$$

where F_s is the sampling frequency. Rearranging Eqn. (B.5) gives

$$F_{tone} = (1 - \frac{p}{q})\frac{F_s}{2}. \tag{B.6}$$

B.2 Estimation of Quantizer Input Signal Distribution for First-Order Σ-Δ A/D Converter Configuration

Consider the first-order Σ-Δ A/D converter configuration as shown in Fig. 1.13. One may decompose this system into an equivalent system with two inputs as shown in Fig. B.1. Here $u(n)$ is a DC input

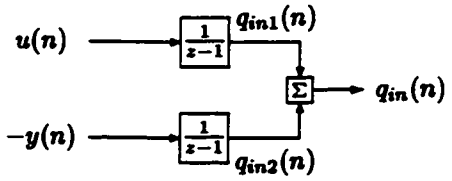

Figure B.1: Decomposed First-Order Σ-Δ A/D Converter Configuration

signal represented by $u(n) = \frac{p}{q}$ and $y(n)$ is simply the quantizer output stream of $+1$ and -1 values. Since, the system $H(z) = \frac{1}{z-1}$ is simply an accumulator, $q_{in1}(n) = n\frac{p}{q}$ and $q_{in2}(n) = \sum_{i=0}^{n} -y(i)$. If one could determine the first $2q$ samples of $y(n)$, then the quantizer input signal $q_{in}(n)$ could be estimated. Since the mean of the output $y(n)$ must be equal to the mean of the input signal $\frac{p}{q}$, the output $y(n)$ can be easily determined using the following procedure.

Procedure:

$y(1) = 1$

for $i = 2 : 2q$

  if $E\{y(n)\} > \frac{p}{q}$ *then*

    $y(i) = -1$

  else

    $y(i) = 1$

  end

end

As an example, let $\frac{p}{q} = \frac{23}{100}$. Then $2q = 200$ samples of $y(n)$ may be obtained using the above procedure. Once $y(n)$ has been obtained, $q_{in1}(n)$ and $q_{in2}(n)$ can be generated and combined to form $q_{in}(n)$. The distribution of $q_{in}(n)$ was then determined and is shown in Fig. B.2. A simulation was then conducted and the actual $q_{in}(n)$ was determined leading to the distribution shown in Fig. B.3. Next, the moments of the estimated $q_{in}(n)$ were calculated and compared to the actual moments of the $q_{in}(n)$ (determined through simulation). The results are as shown in Table B.1. The estimated and actual moments of the quantizer input signal $q_{in}(n)$ agree very well thus verifying the correctness of the moment estimation technique.

B.3 Estimation of Quantizer Input Signal Distribution for 2-nd Order Σ-Δ A/D Converter Configuration

The 2-nd order Σ-Δ A/D converter may be decomposed into the system shown in Fig. B.4. Here, $u(n)$ is a DC input signal represented by $u(n) = \frac{p}{q}$, and $y(n)$ is simply the quantizer output stream of $+1$ and -1 values. An analysis of the unit-impulse response of the system $H_1(z) = \frac{Q_{in1}(z)}{U(z)}$ reveals that $h_1(n) = n$. This result implies that $q_{in1}(1) = 1$ and $q_{in1}(n) = \begin{pmatrix} n \\ 2 \end{pmatrix}$. Furthermore, an

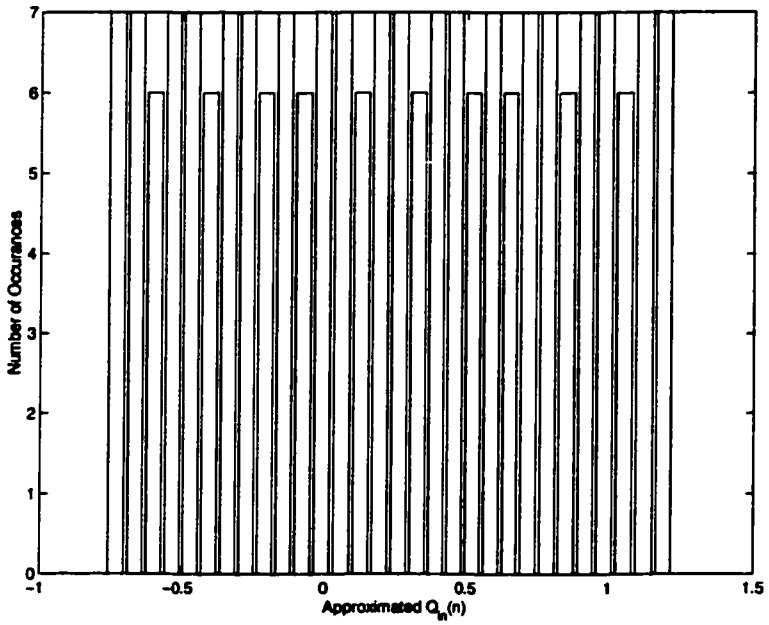

Figure B.2: Estimated First-Order Σ-Δ A/D Converter Quantizer Input Signal Distribution

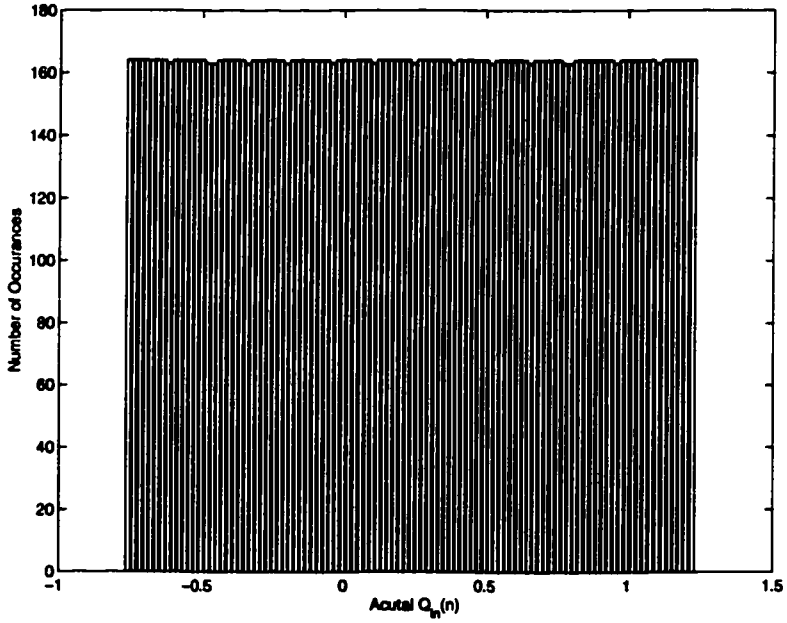

Figure B.3: Actual First-Order Σ-Δ A/D Converter Quantizer Input Signal Distribution

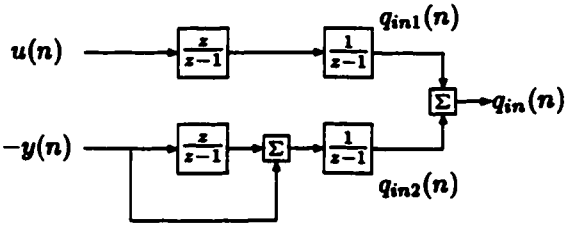

Figure B.4: Decomposed 2-nd Order Σ-Δ A/D Converter Configuration

Table B.1: Actual and Estimated First-Order Σ-Δ A/D Converter Quantizer Input Signal Moments

Moment	Actual $Q_{in}(n)$	Estimated $Q_{in}(n)$
Mean	0.23494659749757	0.22500000000000
Variance	0.33333823109576	0.33500000000000
3	1.088653087316250e-006	-6.588479761759913e-017
4	0.19998646816484	0.19998333362500
5	-2.912090907281327e-006	9.107298248878238e-019
6	0.14283795922983	0.14283214431545
7	-6.357723224730307e-006	4.793501750047224e-017
8	0.11108302236725	0.11107778186090
9	-8.676749033897683e-006	7.357511562483933e-017
10	0.09087102165545	0.09086743299146

analysis of the unit-impulse response of the system $H_2(z) = \frac{Q_{in2}(z)}{Y(z)}$ reveals that $h_2(n) = -n - 1$. This result implies that $q_{in2}(n) = \sum_{i=}^{n} \pm (i+1)$. If one could determine the first $4q$ samples of $y(n)$, then the quantizer input signal $q_{in}(n)$ could be estimated. Since the mean of the output $y(n)$ must be equal to the mean of the input signal $\frac{p}{q}$, the output $y(n)$ can be easily determined using a procedure identical to that outlined in the previous subsection with the exception that the procedure must be run for $4q$ samples. As an example, let $\frac{p}{q} = \frac{7}{8}$. Then $4q = 32$ samples of $y(n)$ may be obtained using the above procedure. Once $y(n)$ has been obtained, $q_{in1}(n)$ and $q_{in2}(n)$ can be generated and combined to form $q_{in}(n)$. The distribution of $q_{in}(n)$ was then determined and is shown in Fig. B.5. A simulation was then conducted and the actual $q_{in}(n)$ was determined leading to the distribution shown in Fig. B.6. Next, the moments of the estimated $q_{in}(n)$ were calculated and compared to the actual moments of the $q_{in}(n)$ determined through simulation. The results are as shown in Table B.2.

The estimated and actual moments of the quantizer input signal $q_{in}(n)$ agree very well thus verifying the correctness of the moment estimation technique.

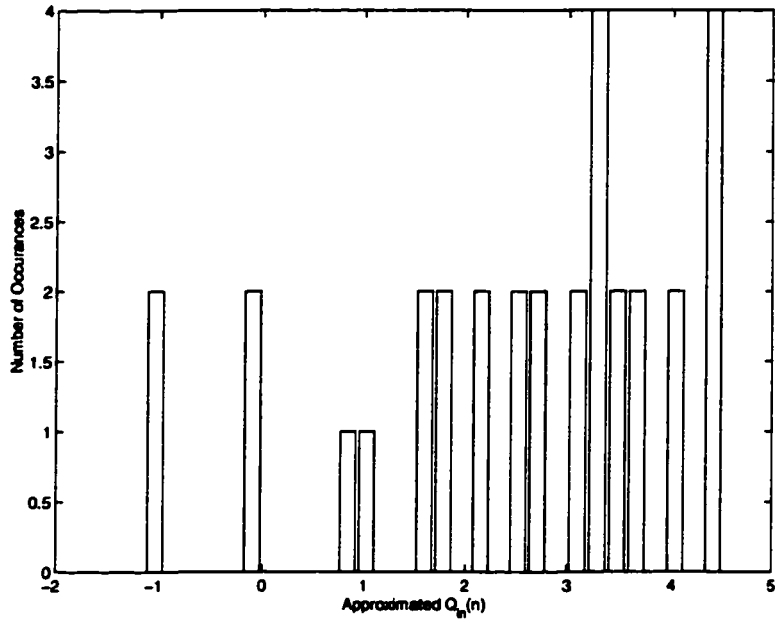

Figure B.5: Estimated 2-nd Order Σ-Δ A/D Converter Quantizer Input Signal Distribution

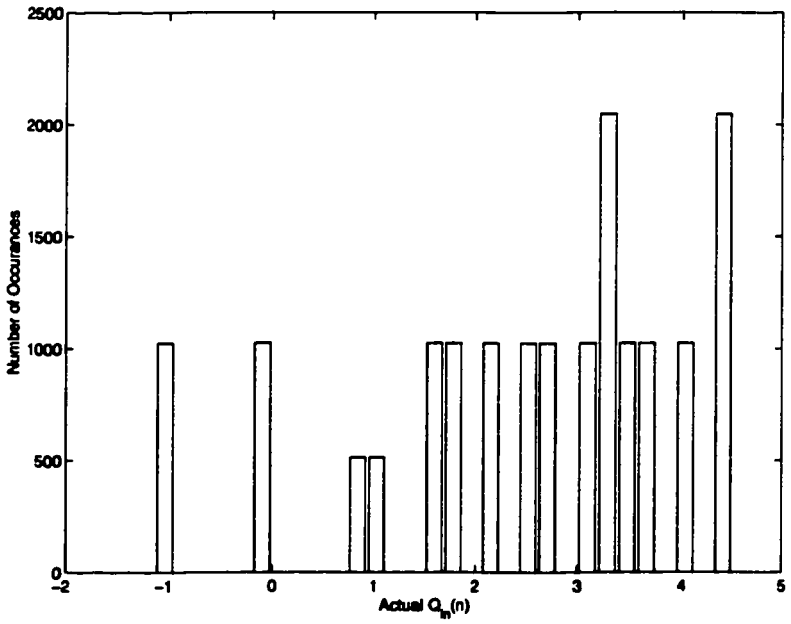

Figure B.6: Actual 2-nd Order Σ-Δ A/D Converter Quantizer Input Signal Distribution

Table B.2: Actual and Estimated 2-nd Order Σ-Δ A/D Converter Quantizer Input Signal Moments

Moment	Actual $Q_{in}(n)$	Estimated $Q_{in}(n)$
Mean	2.56234360695758	2.56250000000000
Variance	2.31680700717122	2.39112903225806
3	-3.08764217571444	-3.08789062500000
4	16.15646712164779	16.15675354003906
5	-43.16980298888438	-43.17832946777344
6	1.680128184791371e+002	1.680463095307350e+002
7	-5.523298488147996e+002	-5.525032440125942e+002
8	2.019997630257215e+003	2.020698650136823e+003
9	-7.086740033699986e+003	-7.089725682546850e+003
10	2.565241444105976e+004	2.566432110141348e+004